

Compal confidential

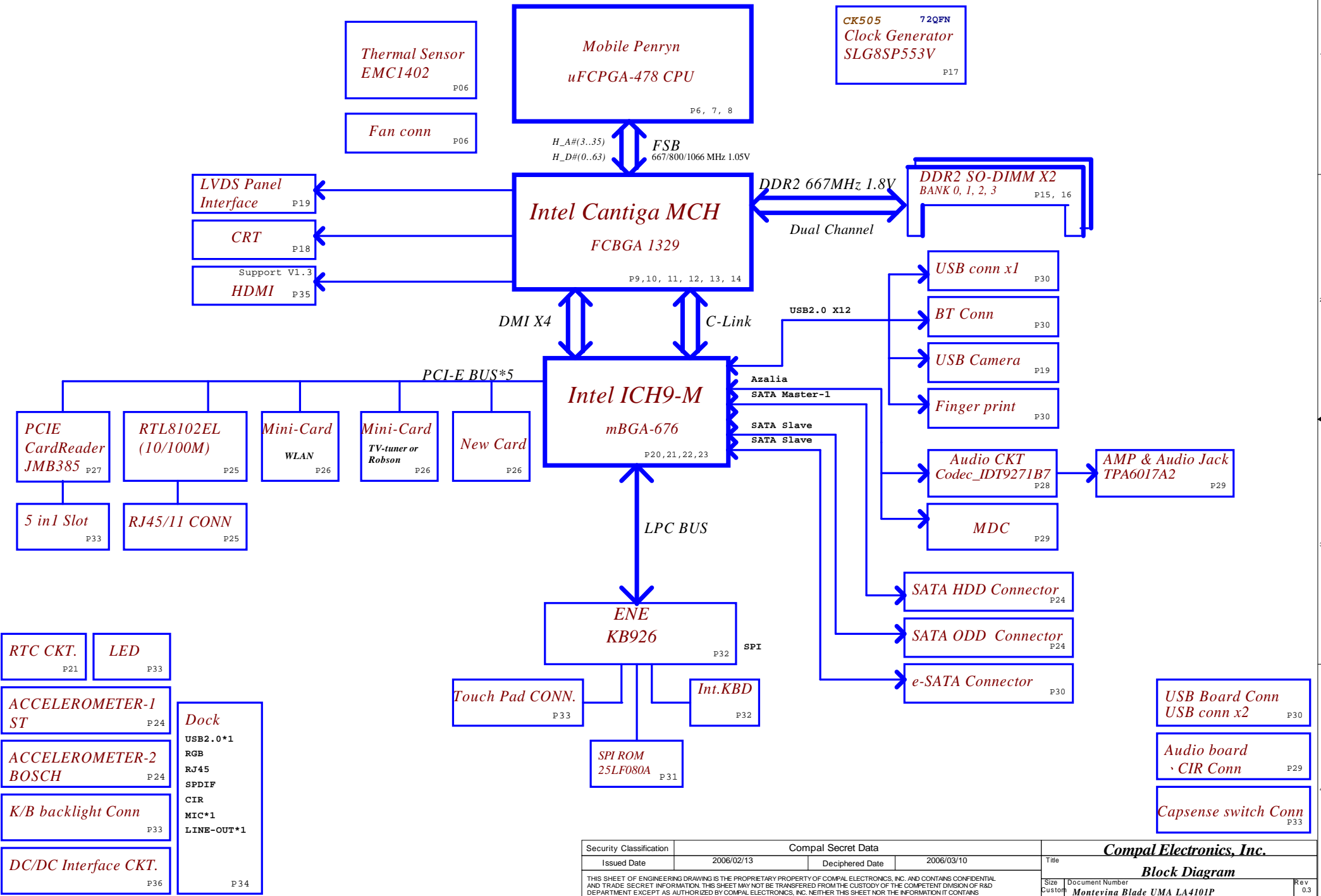
Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M core logic

2008-01-01

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Issued Date	2007/08/28	Deciphered Date	2006/03/10	Cover Sheet		
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Montevina Consumer 14" UMA



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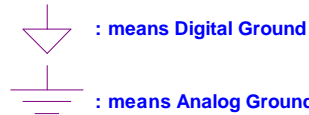
Block Diagram

Voltage Rails

O MEANS ON X MEANS OFF

power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
State				
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
DOCK@ :	means just reserve for Docking
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Dock
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	TV /WWAN/Robeson
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	Card reader
PCIe-6	New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

43154432L01 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/Multi@/2MiniC@
 43154432L02 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/2MiniC@
 43154432L03 : Main@/DEBUG@/DOCK@/NewC@/FP@/2MiniC@
 43154432L04 : OPP@/DEBUG@
 43154432L05 : OPP@/DEBUG@

I2C / SMBUS ADDRESSING

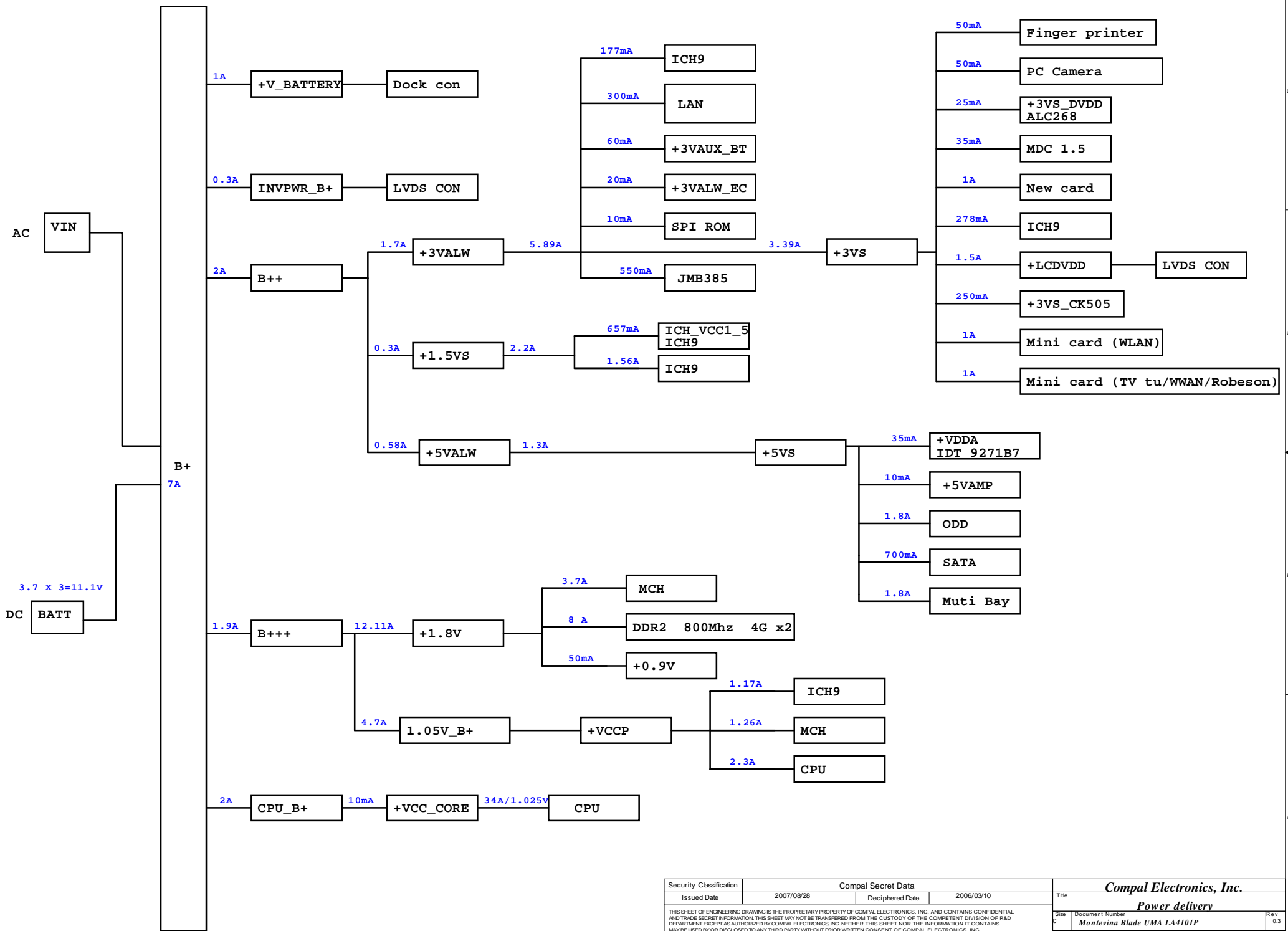
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

43154432L01 : UMA GM PA FF (SI-1)
 43154432L02 : UMA GM PR FF (SI-1)
 43154432L03 : UMA GL PR FF-
 43154432L04 : UMA GM OPP (SI-1)
 43154432L05 : UMA GL OPP

Cantiga GM45 B0(QR32) : SA00001P930
 ICH9M A2 ES2 Base : SA00002AN10

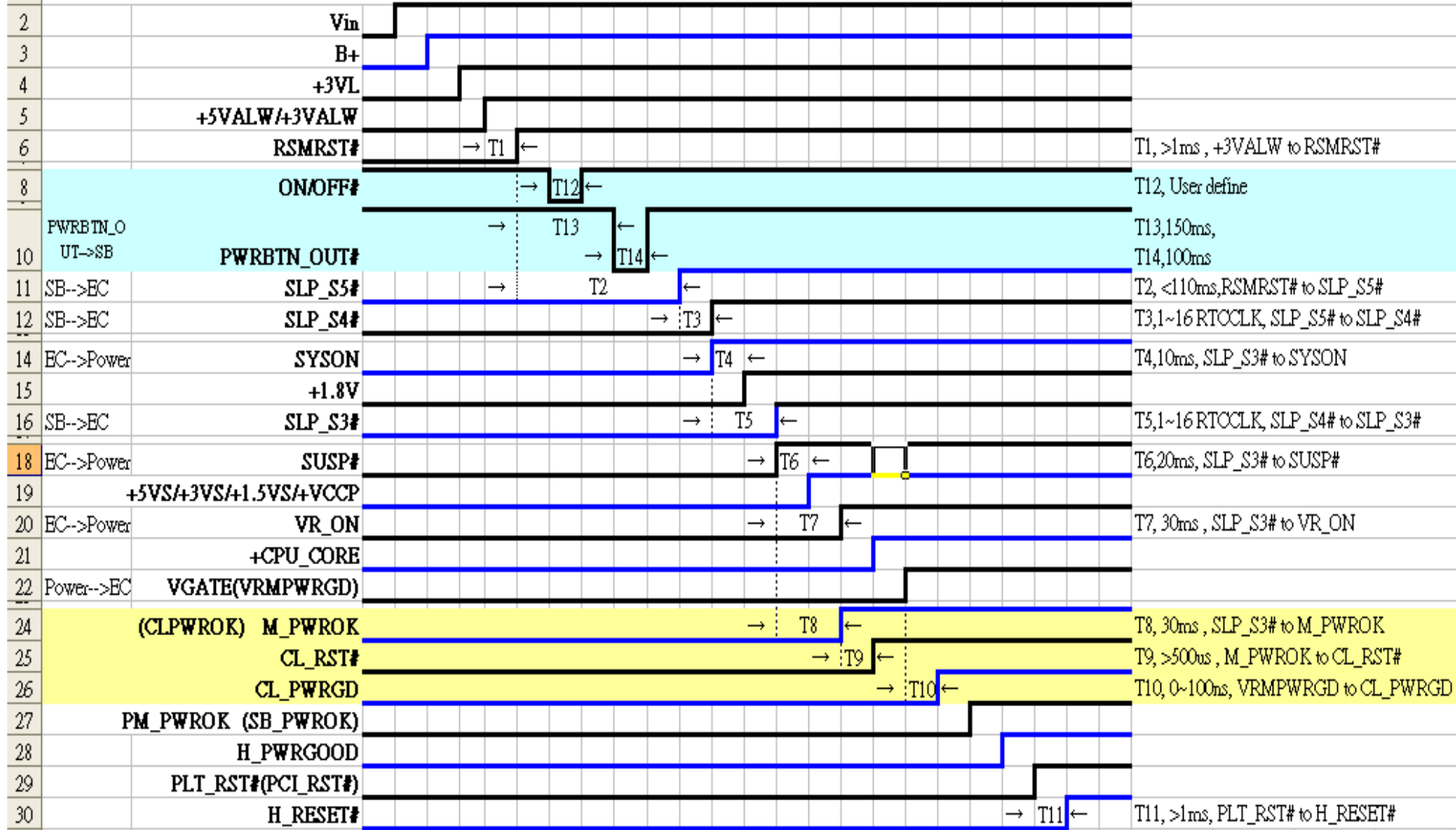
DA600007100 --->Main
 DAZ03V00100 --->OPP

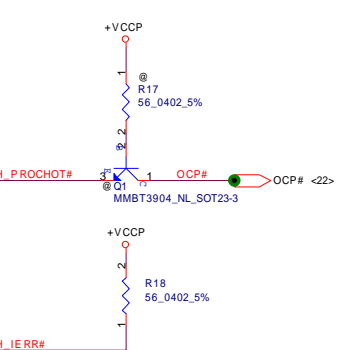
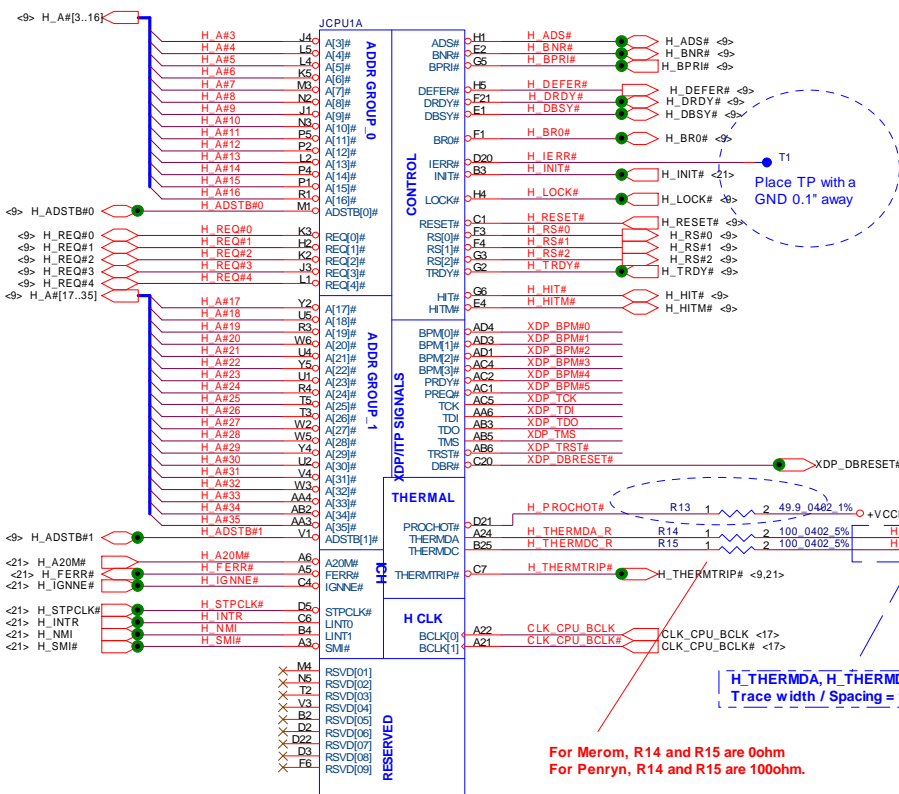
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JAL50 power sequence AC mode

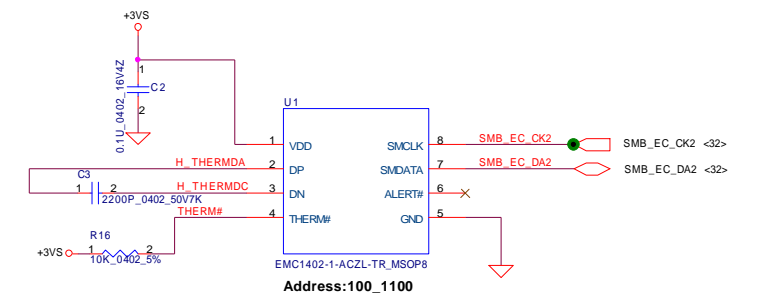
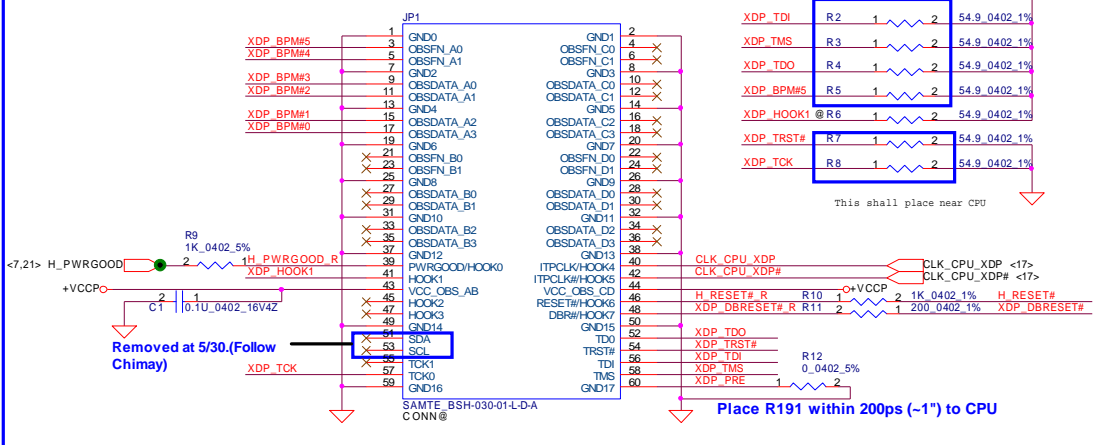
96.09.03.



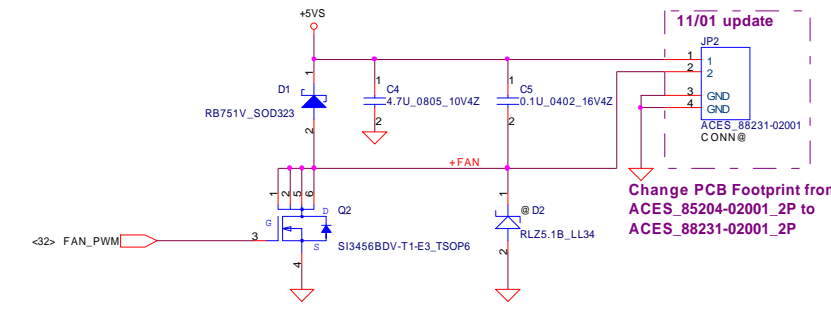


For Merom, R14 and R15 are 0ohm
For Penryn, R14 and R15 are 100ohm.

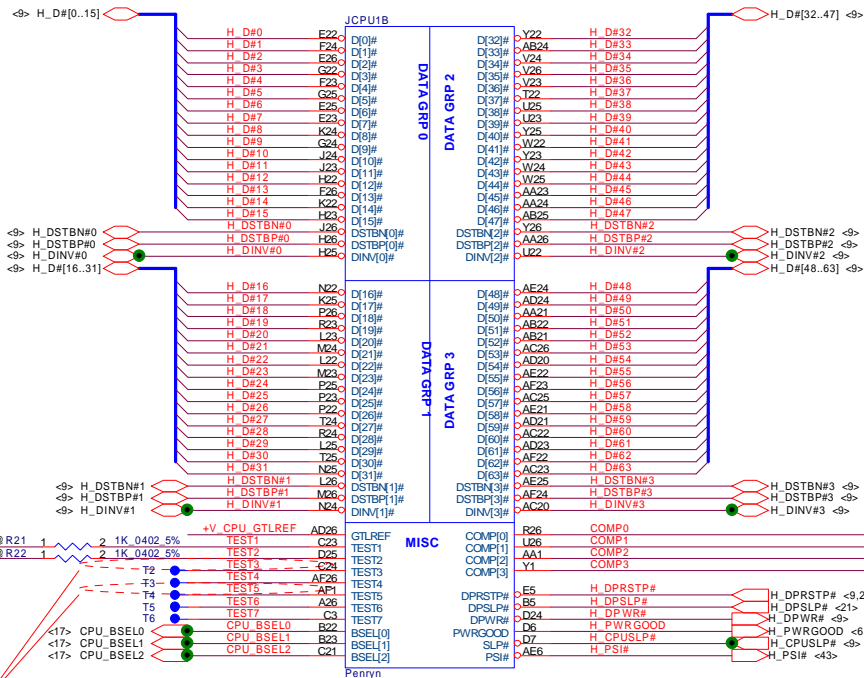
ITP-XDP Connector



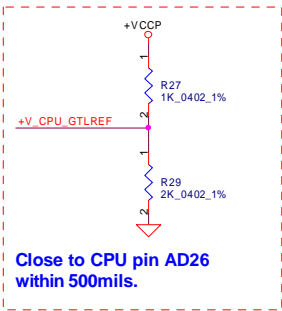
PWM Fan Control circuit



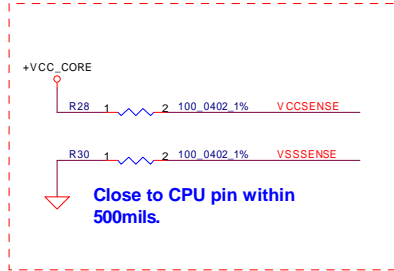
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Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

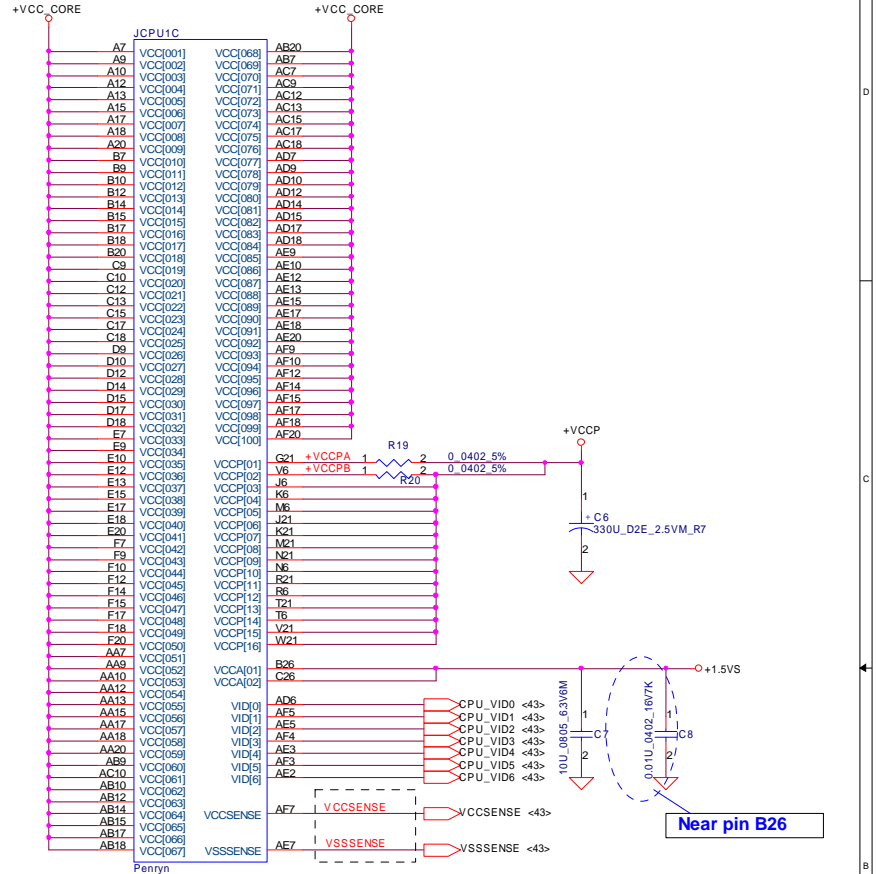


Length match within 25 mils. The trace width/space/other is 20/7/25.



* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

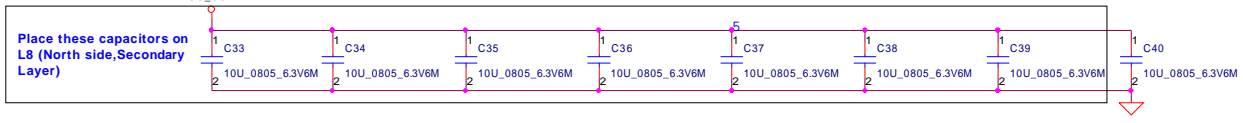
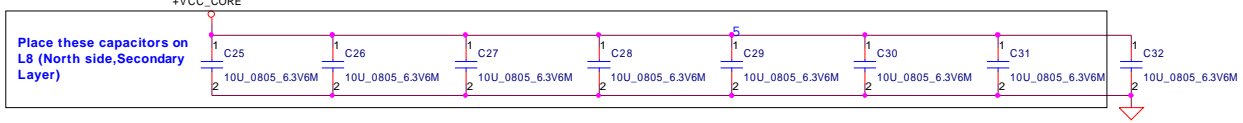
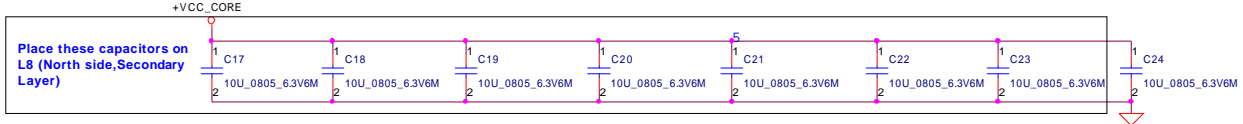
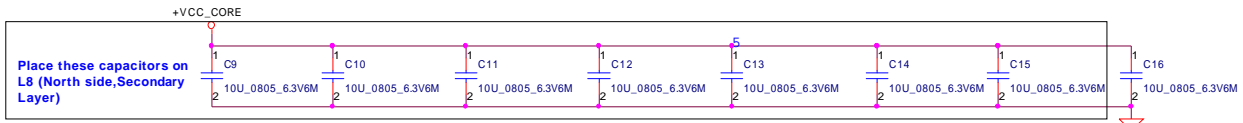


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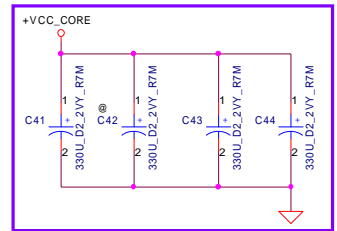
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JCPU1D		
A4	VSS1001	P6
A8	VSS1002	P21
A11	VSS1003	P24
A14	VSS1004	D2
A16	VSS1005	R5
A19	VSS1006	R22
A23	VSS1007	R25
A27	VSS1008	T1
A32	VSS1009	T4
A37	VSS1010	T23
A41	VSS1011	T26
A46	VSS1012	U8
A49	VSS1013	U21
A53	VSS1014	U24
A57	VSS1015	U2
A61	VSS1016	V5
A65	VSS1017	V22
A69	VSS1018	V25
A73	VSS1019	VW1
A77	VSS1020	VW4
A81	VSS1021	VW23
A85	VSS1022	VW26
A89	VSS1023	V6
A93	VSS1024	V10
A97	VSS1025	V21
A101	VSS1026	V24
A105	VSS1027	V8
A109	VSS1028	AA2
A113	VSS1029	AA5
A117	VSS1030	AA8
A121	VSS1031	AA11
A125	VSS1032	AA14
A129	VSS1033	AA16
A133	VSS1034	AA19
A137	VSS1035	AA22
A141	VSS1036	AA25
A145	VSS1037	AB1
A149	VSS1038	AB4
A153	VSS1039	AB8
A157	VSS1040	AB11
A161	VSS1041	AB13
A165	VSS1042	AB16
A169	VSS1043	AB19
A173	VSS1044	AB23
A177	VSS1045	AB26
A181	VSS1046	AC3
A185	VSS1047	AC8
A189	VSS1048	AC11
A193	VSS1049	AC14
A197	VSS1050	AC16
A201	VSS1051	AC19
A205	VSS1052	AC21
A209	VSS1053	AC24
A213	VSS1054	AD2
A217	VSS1055	AD5
A221	VSS1056	AD8
A225	VSS1057	AD11
A229	VSS1058	AD13
A233	VSS1059	AD16
A237	VSS1060	AD19
A241	VSS1061	AD22
A245	VSS1062	AD25
A249	VSS1063	AE1
A253	VSS1064	AE4
A257	VSS1065	AE8
A261	VSS1066	AE11
A265	VSS1067	AE14
A269	VSS1068	AE16
A273	VSS1069	AE19
A277	VSS1070	AE23
A281	VSS1071	AE26
A285	VSS1072	A2
A289	VSS1073	AF6
A293	VSS1074	AF8
A297	VSS1075	AF11
A301	VSS1076	AF13
A305	VSS1077	AF16
A309	VSS1078	AF19
A313	VSS1079	AF21
A317	VSS1080	A25
A321	VSS1081	AF25
A325	VSS1082	AF25
A329	VSS1083	AF25

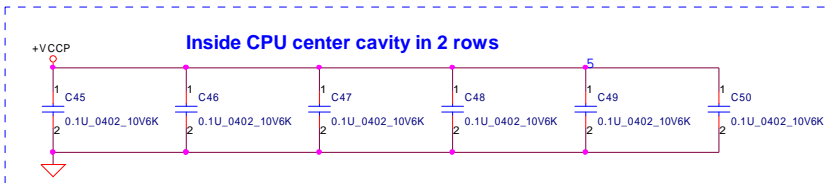


Mid Frequency Decoupling

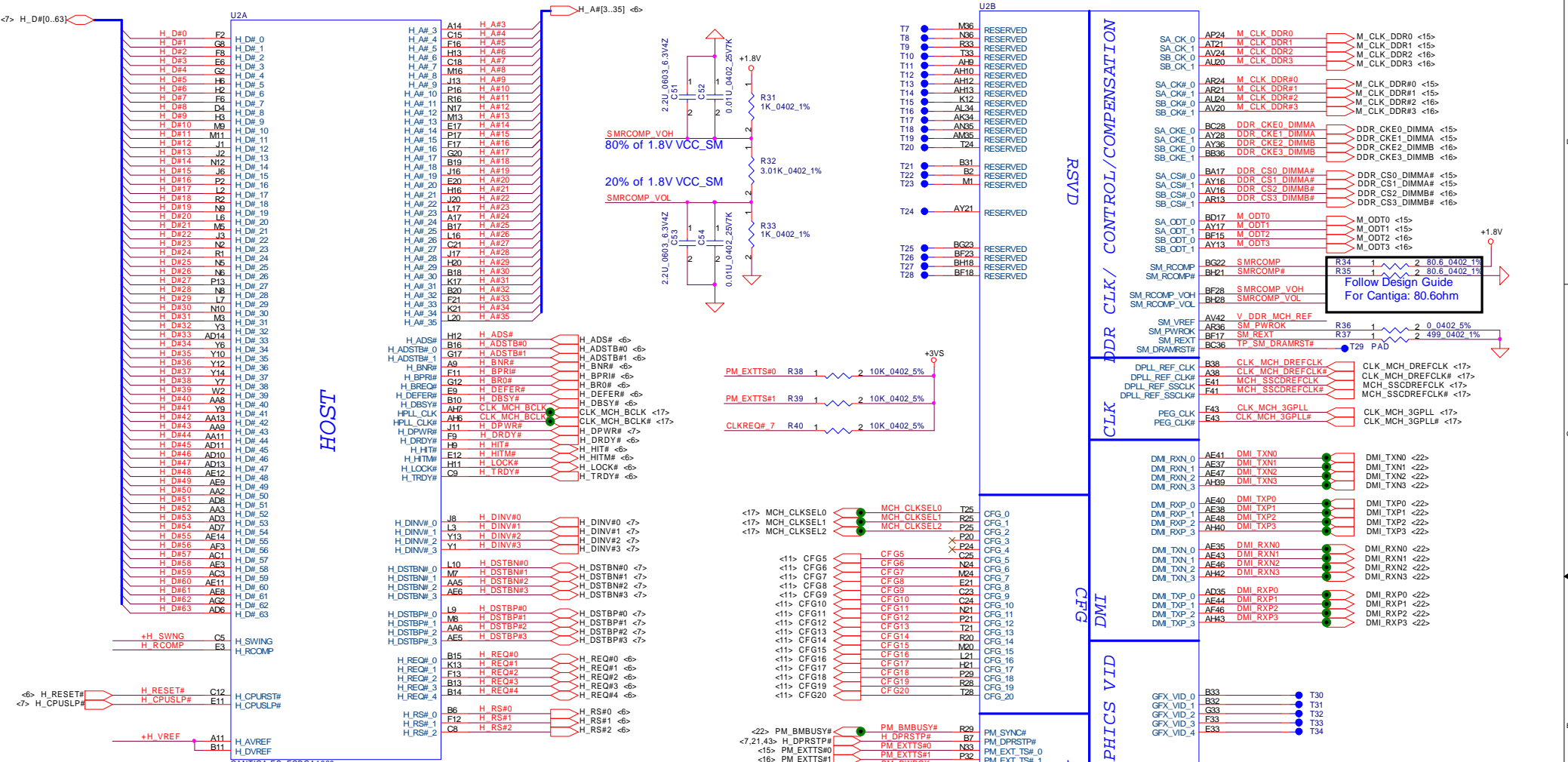
Near CPU CORE regulator
ESR <= 1.5m ohm
Capacitor > 1980uF



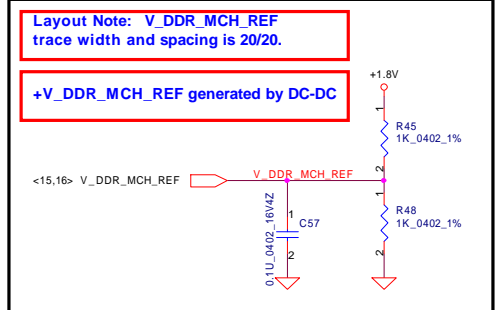
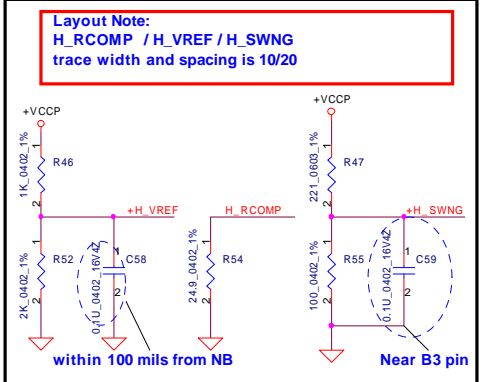
11/21 Change ESR=7m ohm



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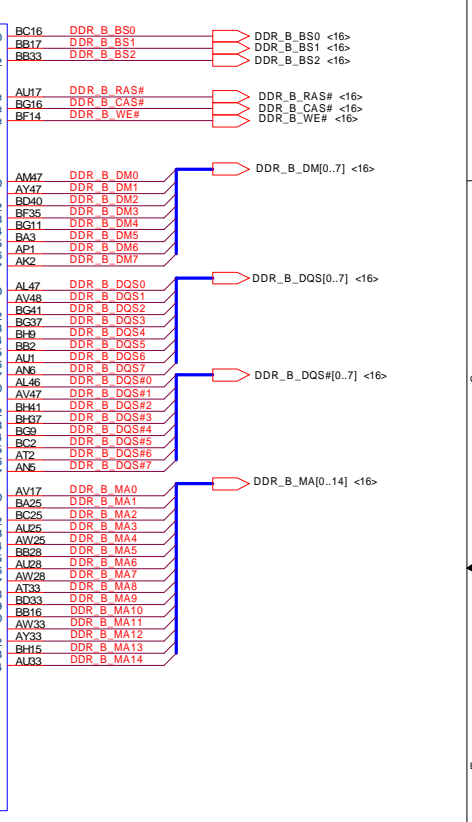
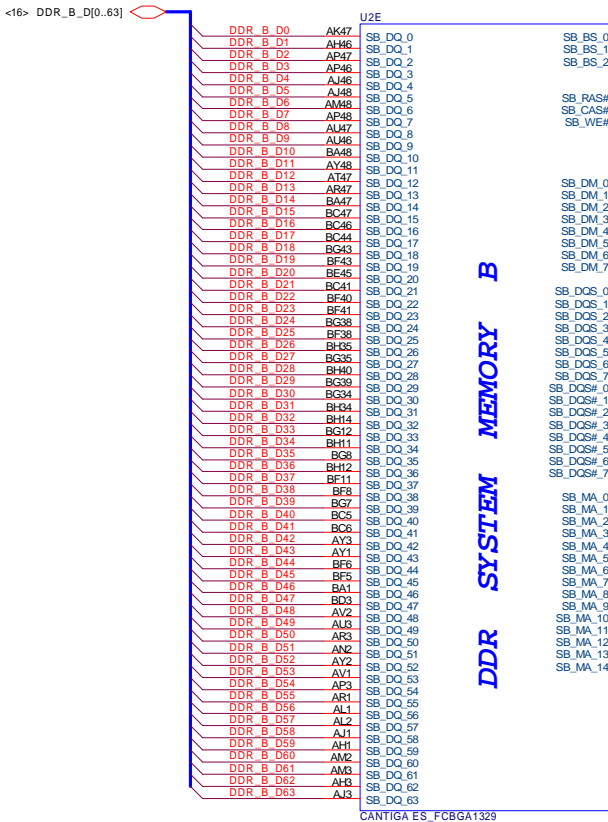
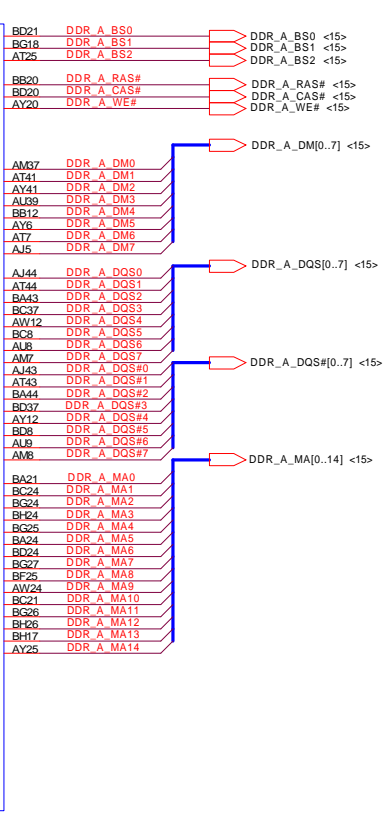
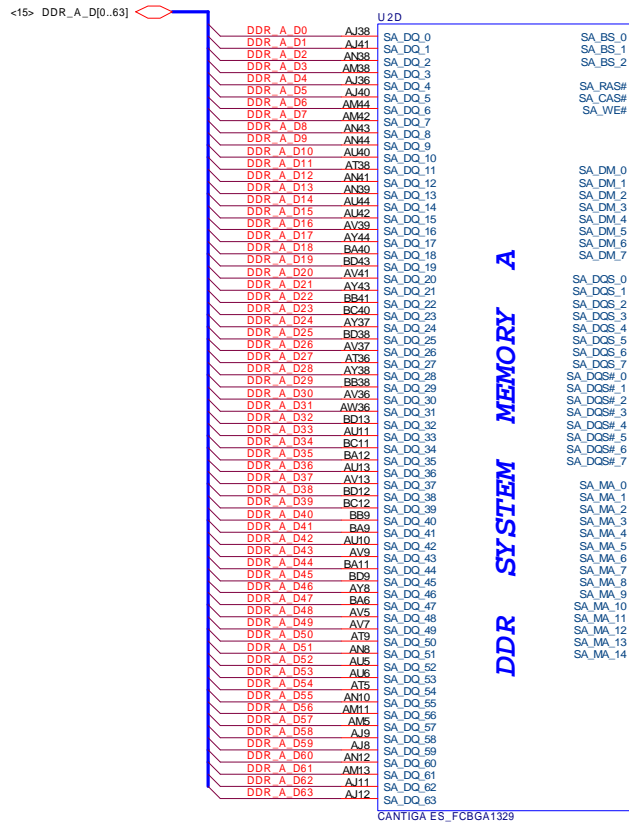


Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

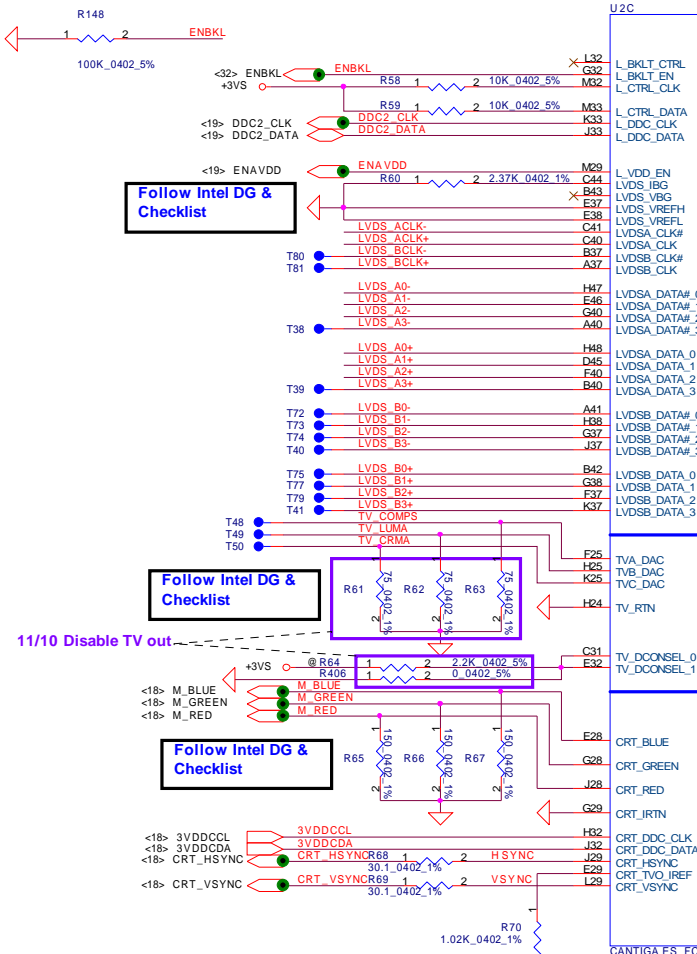


Follow Design Guide For Cantiga: 80.6ohm

R44 Follow Intel feedback



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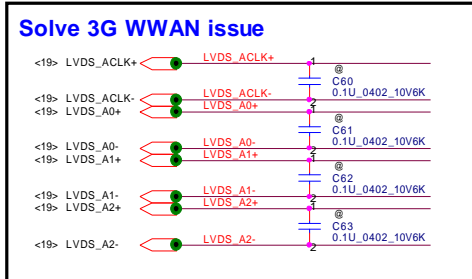


Follow Intel DG & Checklist

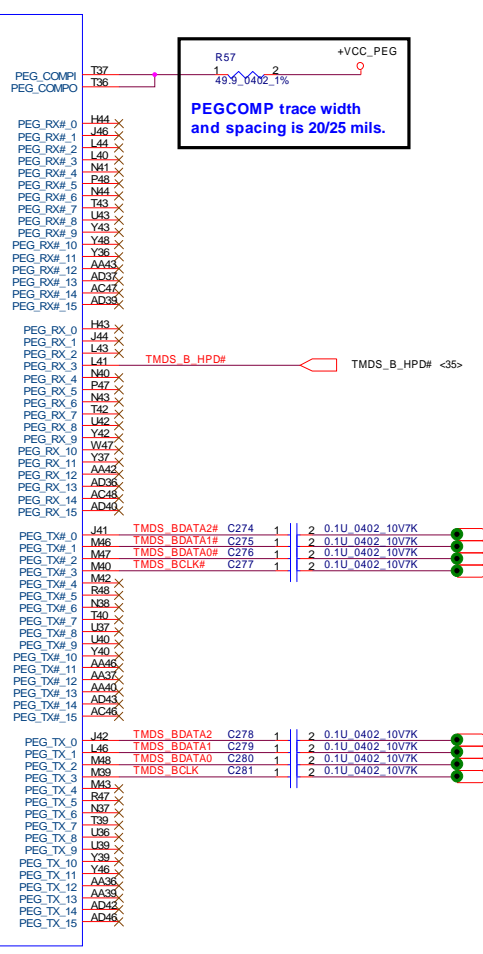
Follow Intel DG & Checklist

Follow Intel DG & Checklist

11/10 Disable TV out



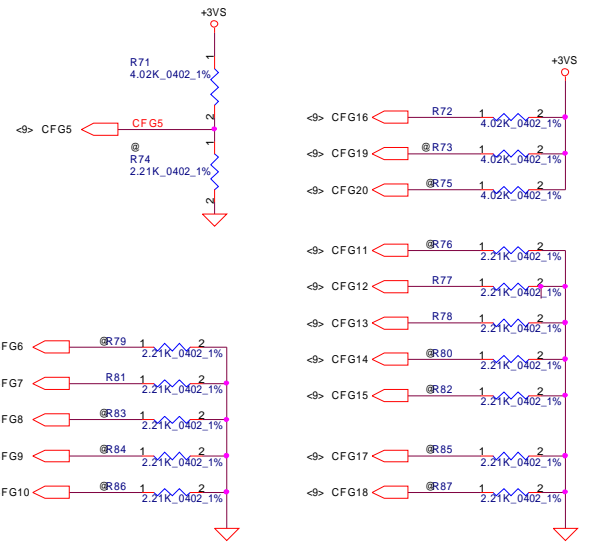
Solve 3G WWAN issue



PEGCOMP trace width and spacing is 20/25 mils.

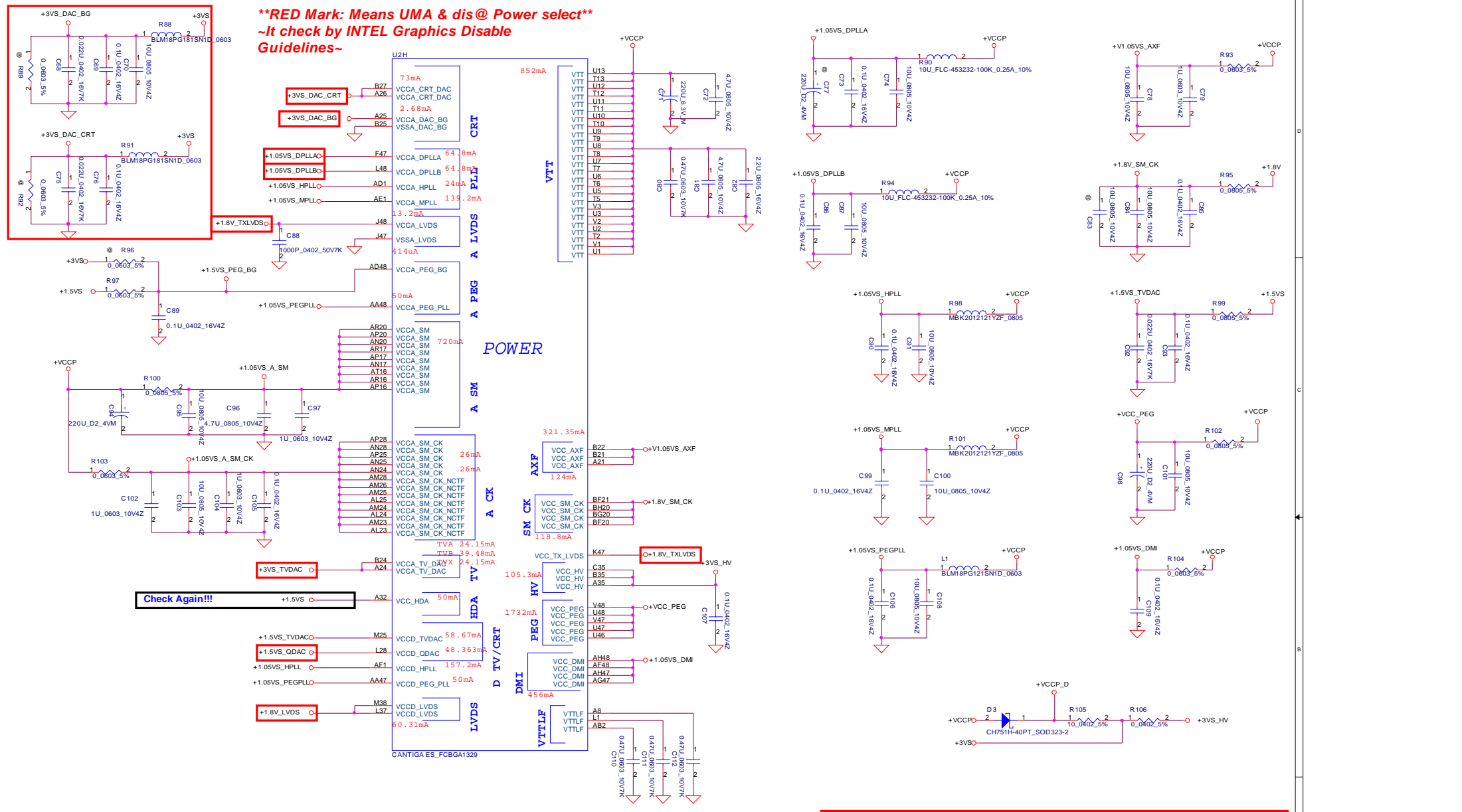
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled (Default) * 11 = Normal Operation
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

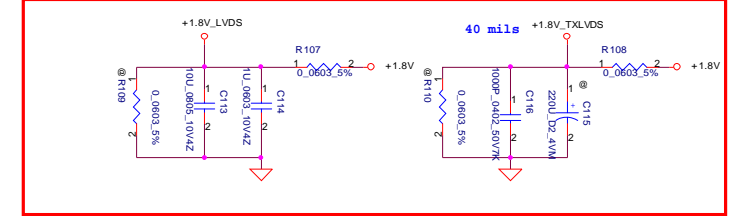
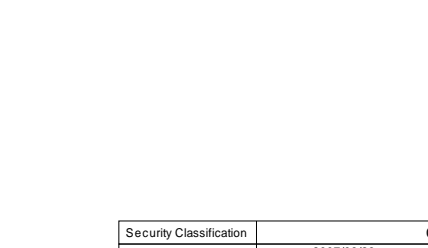
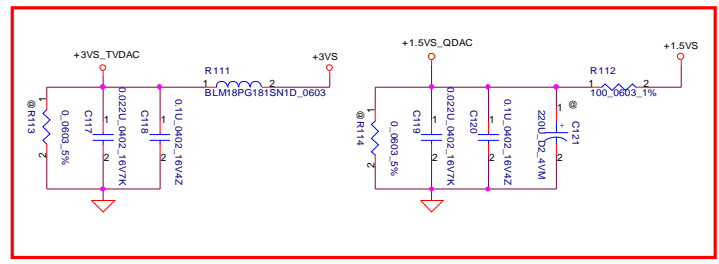


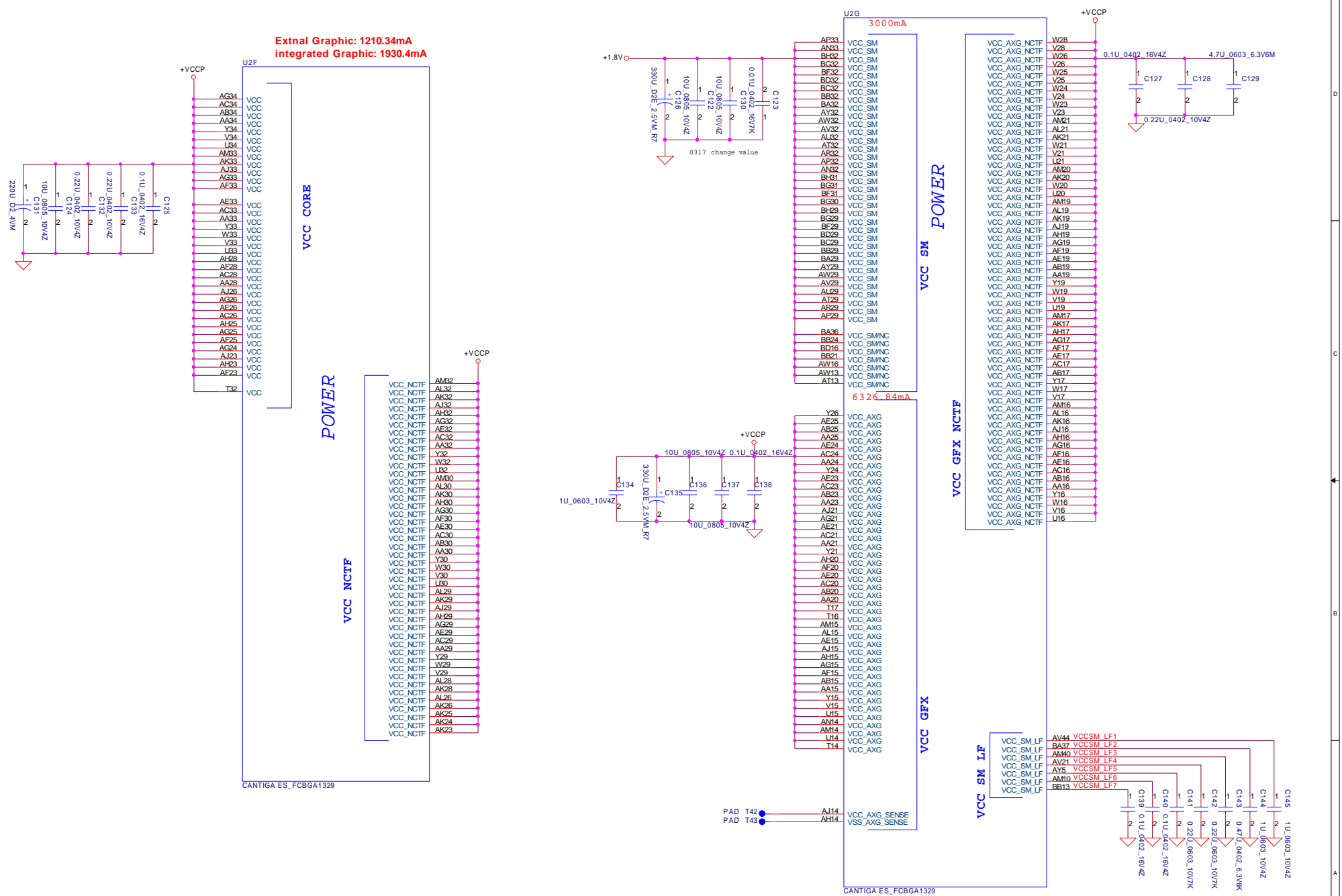
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****RED Mark: Means UMA & dis@ Power select****
~It check by INTEL Graphics Disable
Guidelines~

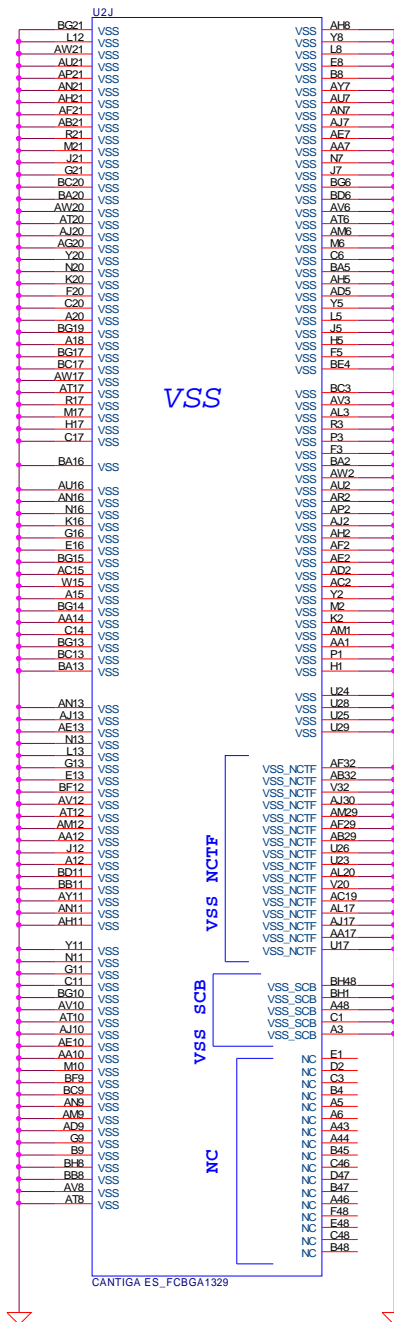
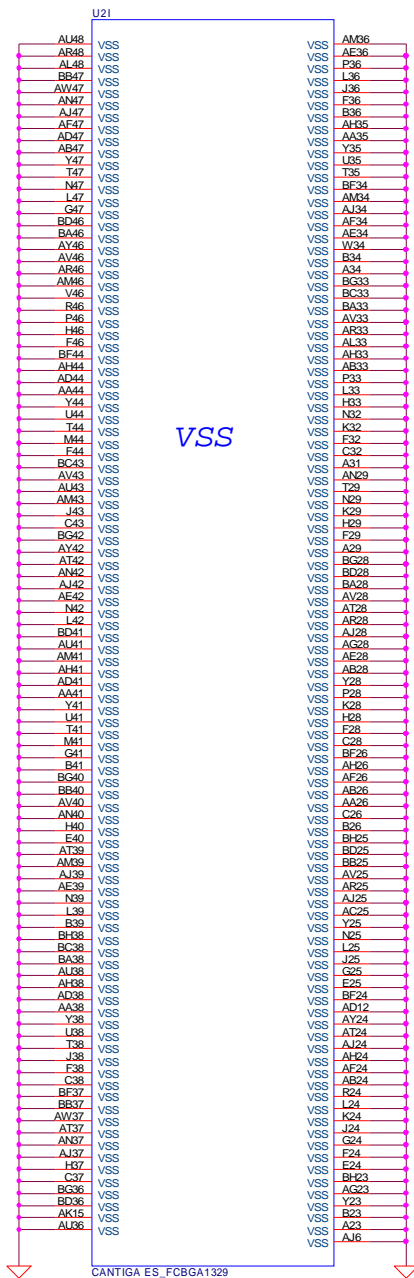


Check Again!!!





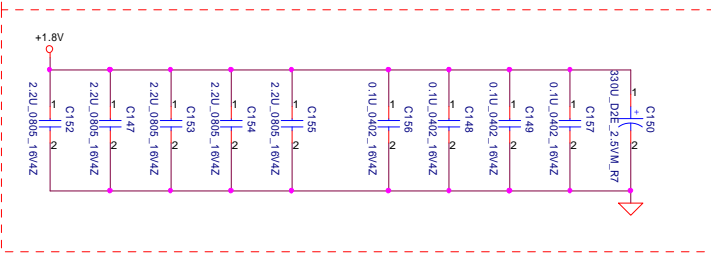
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Issued Date	2007/08/28	Deciphered Date	2006/03/10	Cantiga(5/6)-PWR/GND	
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				Custom	Montevina Blade UMA LA4101P
				Date:	Saturday, January 05, 2008
				Sheet	13 of 46
				Rev	0.3



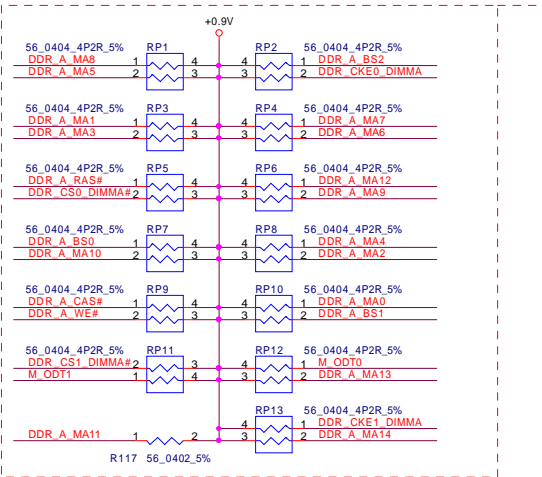
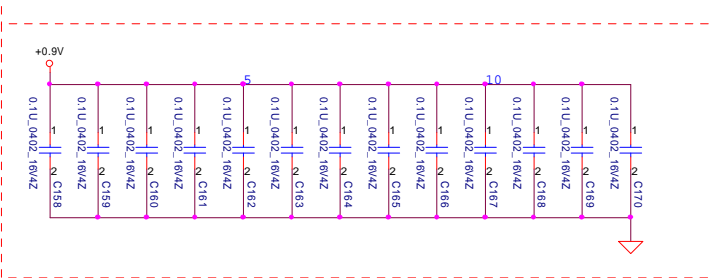
Security Classification	Compal Secret Data		Title		
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
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- <10> DDR_A_DQS#[0..7]
- <10> DDR_A_DQ[0..63]
- <10> DDR_A_DM[0..7]
- <10> DDR_A_DQS[0..7]
- <10> DDR_A_MA[0..14]

Layout Note:
Place near JP3



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V5



Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"

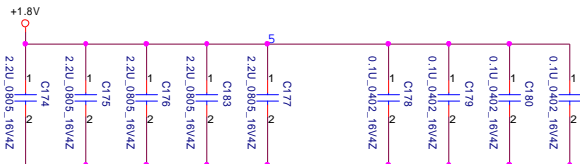


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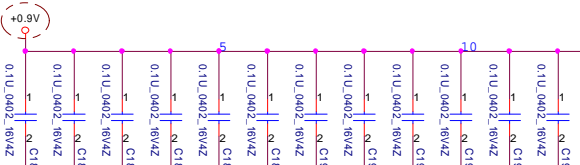
Compal Electronics, Inc.			
DDR2-SODIMM SLOT1			
Size	Document Number	Rev	
Custom	Montevina Blade UMA LA4101P	0.3	
Date:	Saturday, January 05, 2008	Sheet	15 of 46



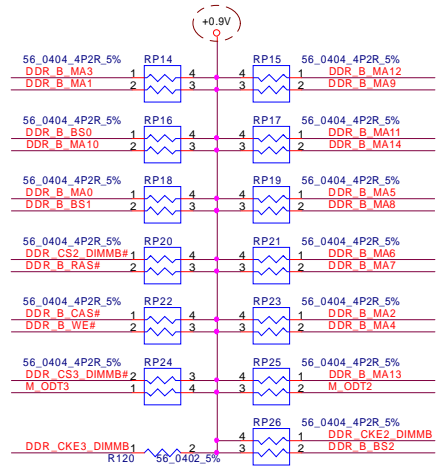
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



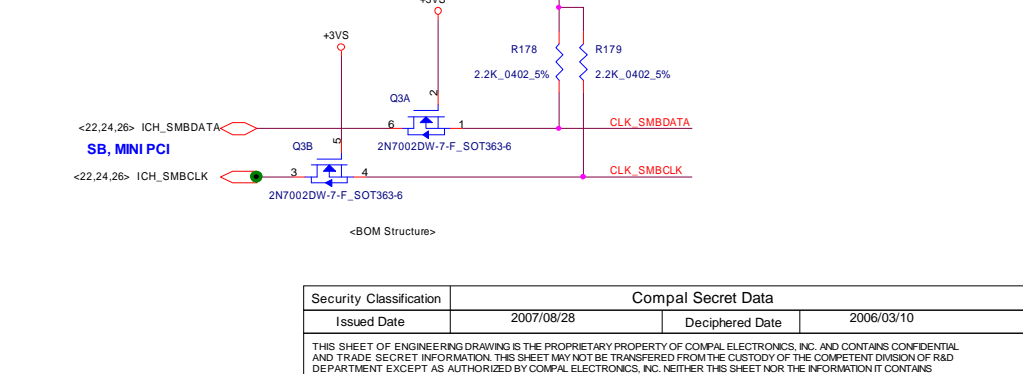
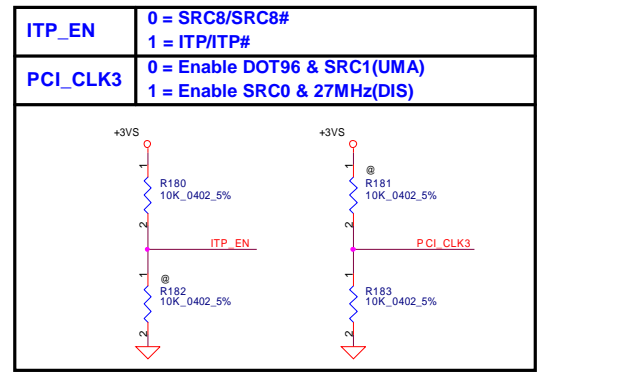
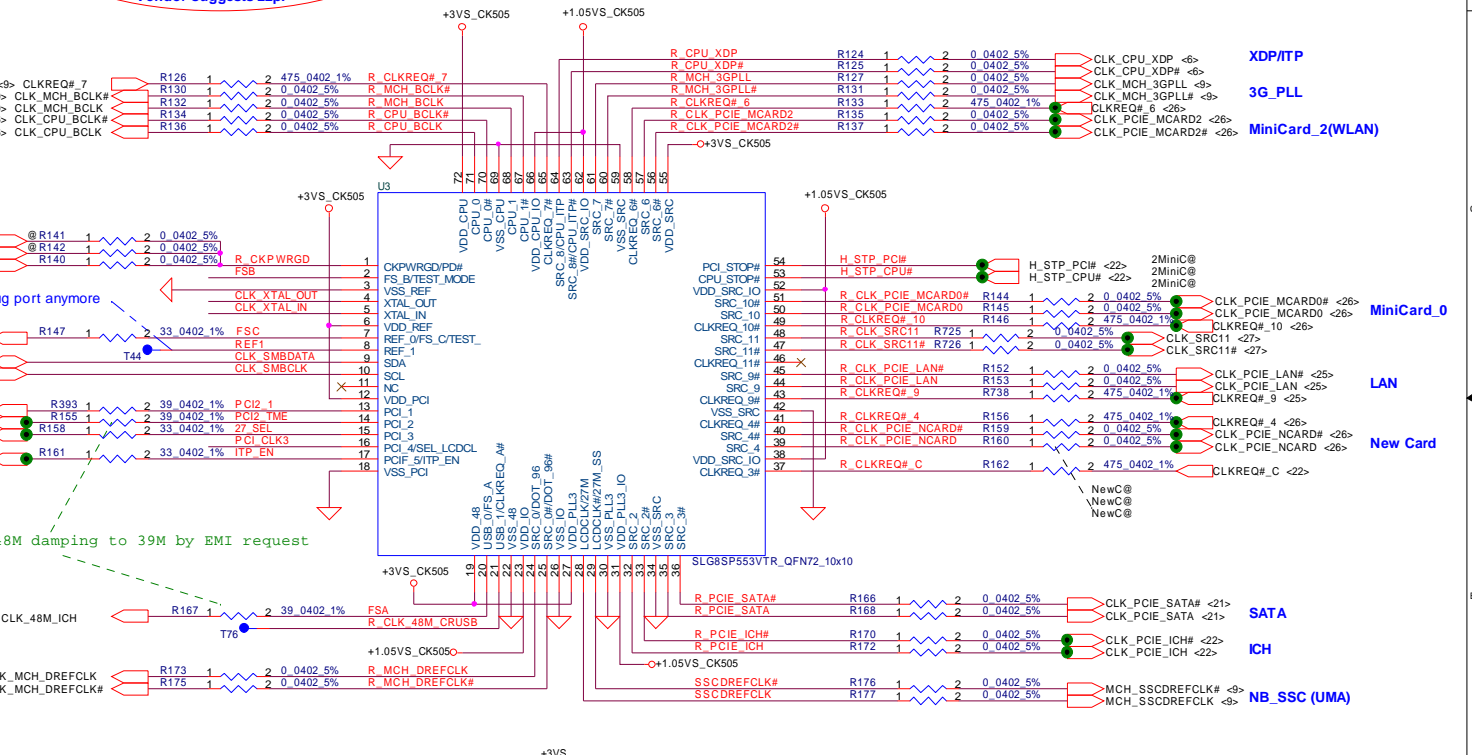
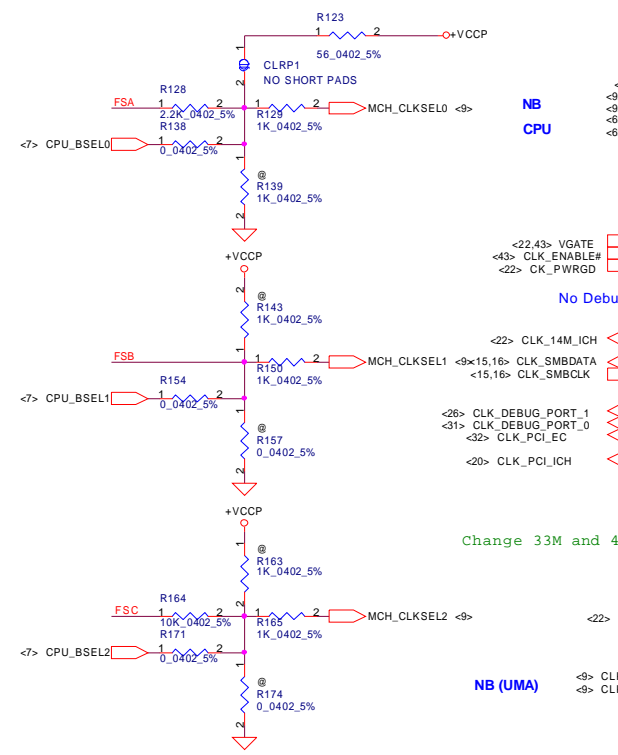
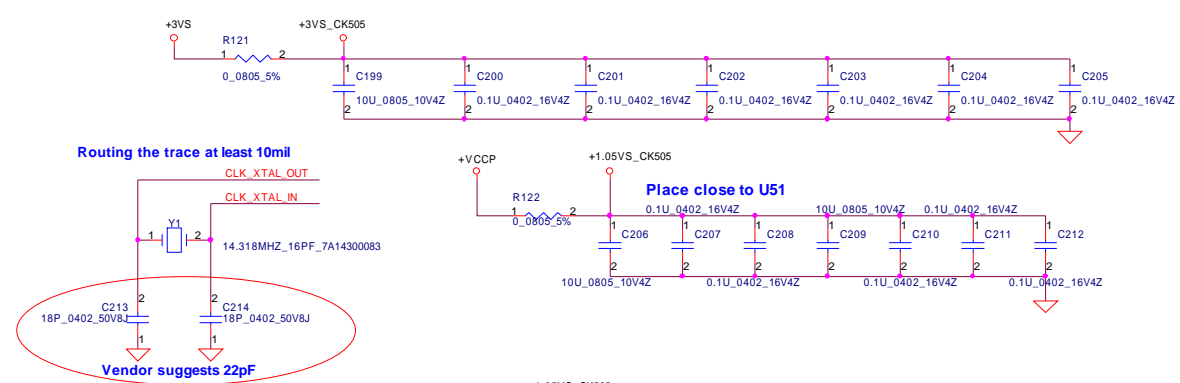
Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"



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Date:	Saturday, January 05, 2008	Sheet	16	of 46

FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						

Reserved



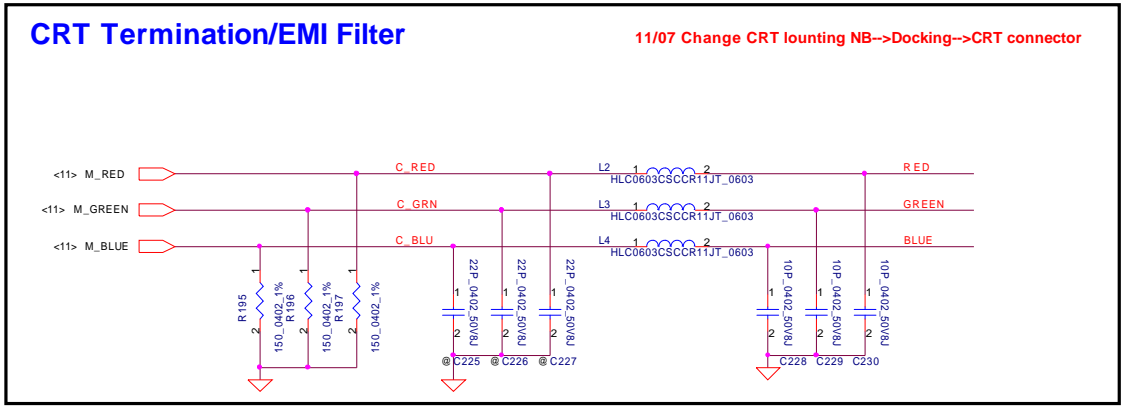
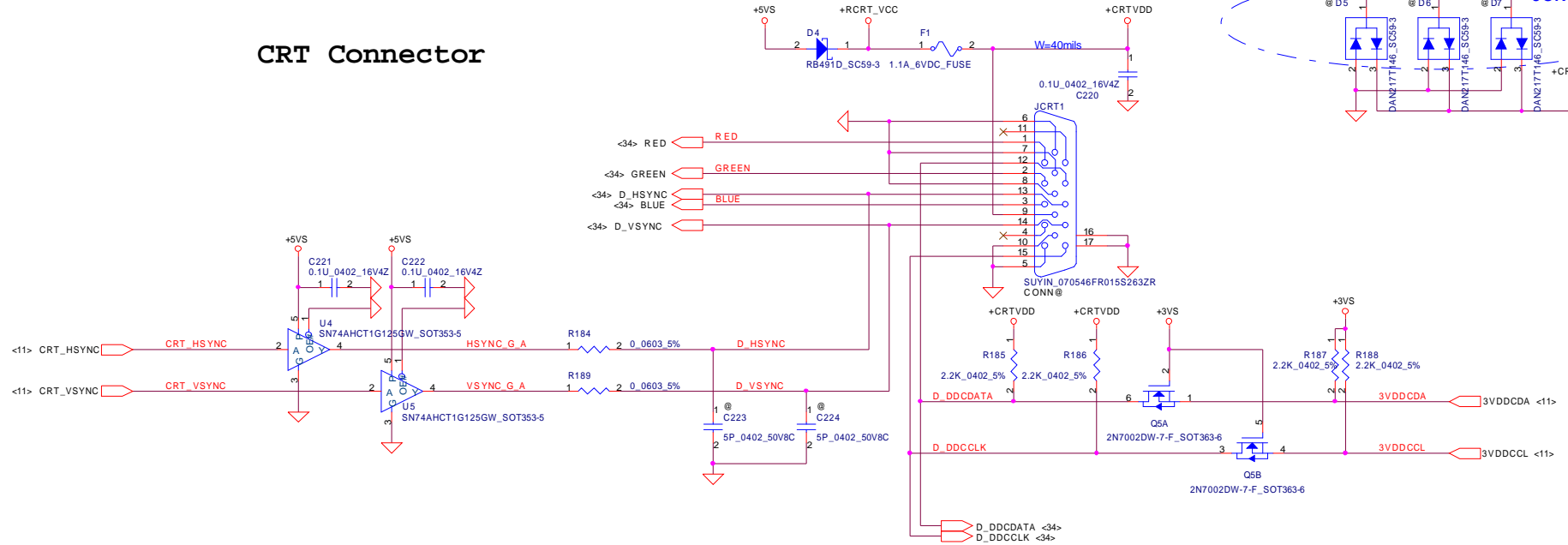
@C215	5P_0402_50V8C	2	1	CLK_48M_ICH
@C216	4.7P_0402_50V8C	2	1	CLK_14M_ICH
@C217	4.7P_0402_50V8C	2	1	CLK_PCI_ICH
@C218	4.7P_0402_50V8C	2	1	CLK_PCI_EC
@C219	5P_0402_50V8C	2	1	CLK_DEBUG_PORT_0

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Issued Date	2007/08/28	Deciphered Date
		2006/03/10

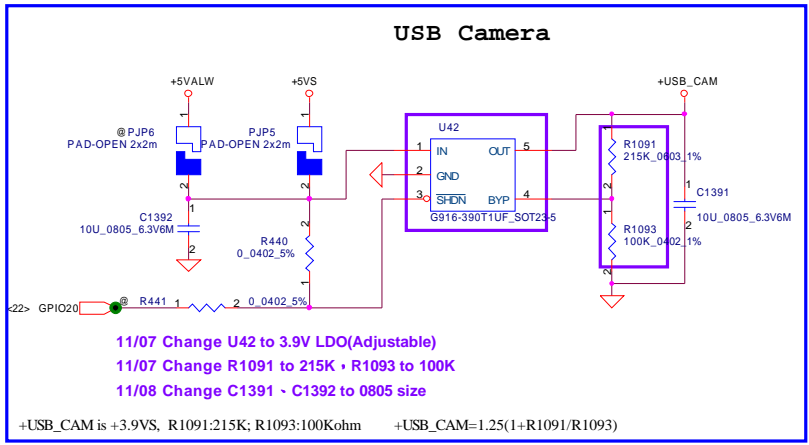
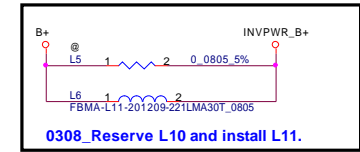
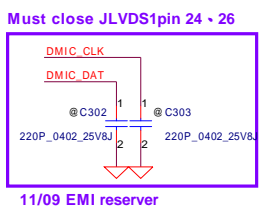
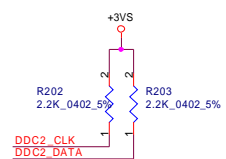
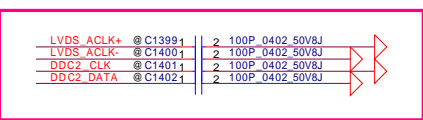
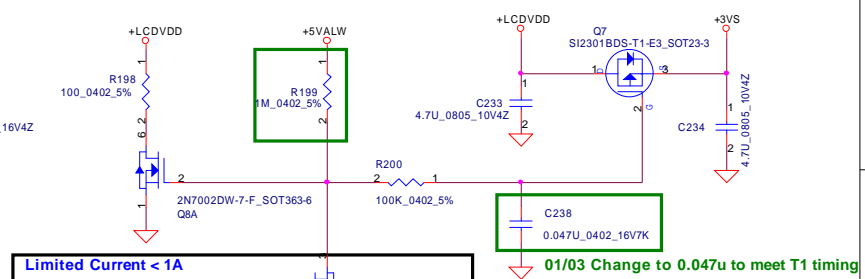
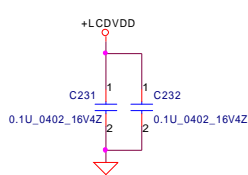
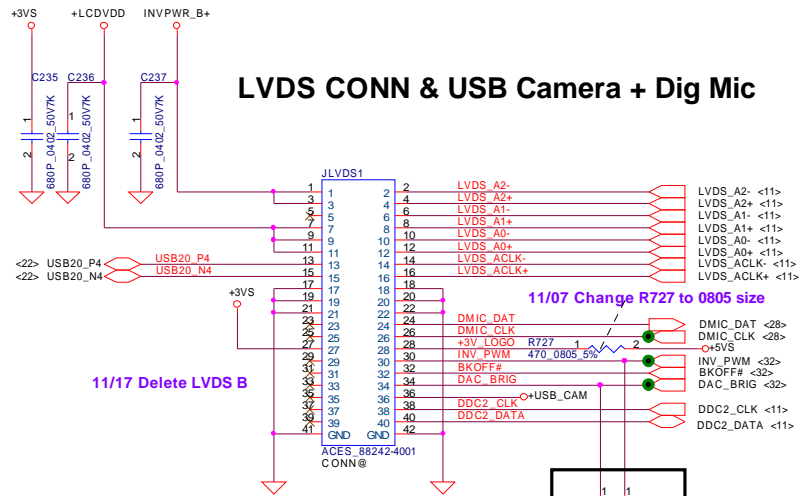
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Title		Compal Electronics, Inc.	
		Clock Generator CK505	
Size	Document Number	Montevina Blade UMA LA4101P	
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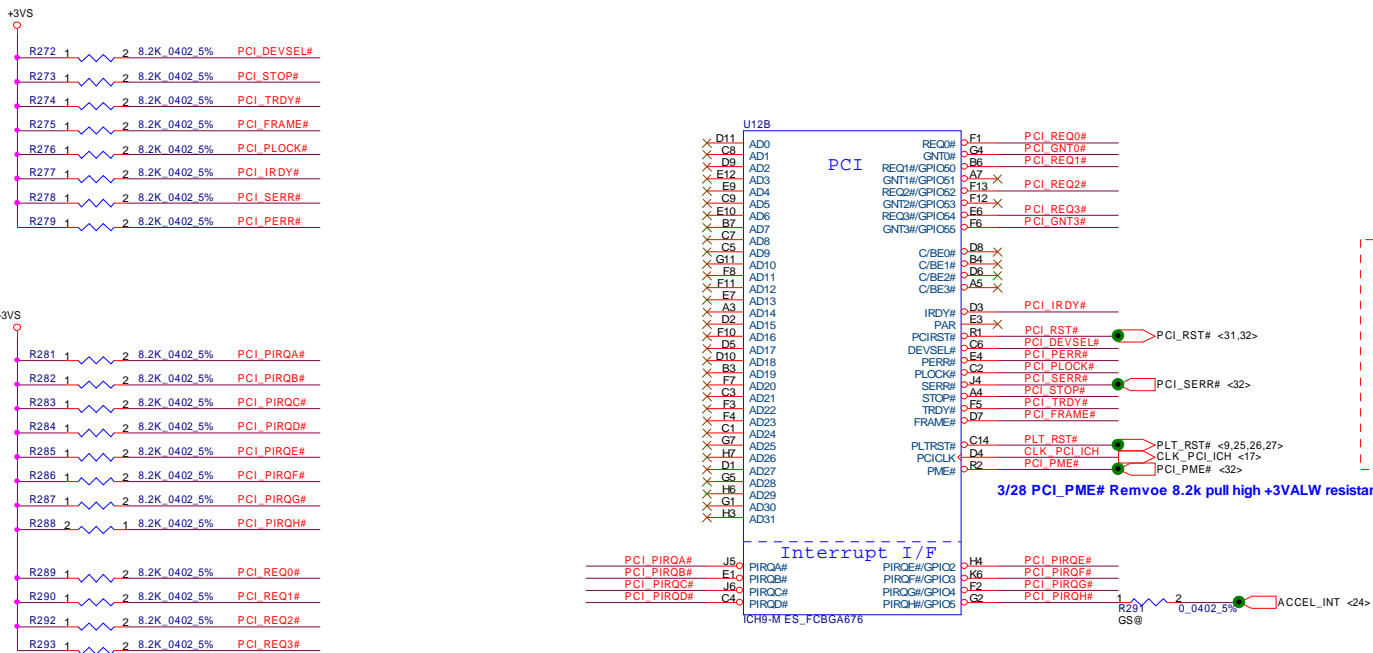
CRT Connector



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				Montevina Blade UMA LA4101P	
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Date:	Saturday, January 05, 2008	Sheet	19	of 46



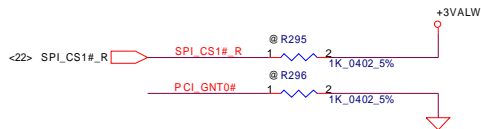
A16 swap override Strap

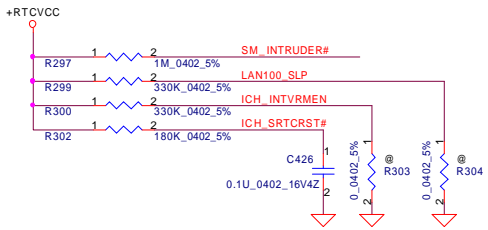
PCI_GNT3# Low= A16 swap override Enable
 High= Default *



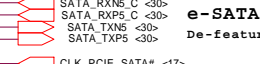
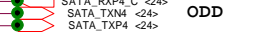
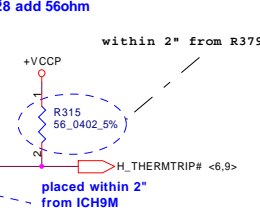
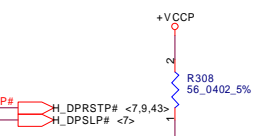
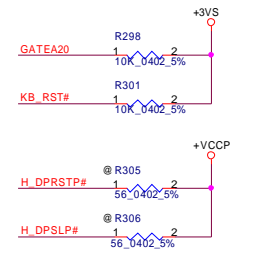
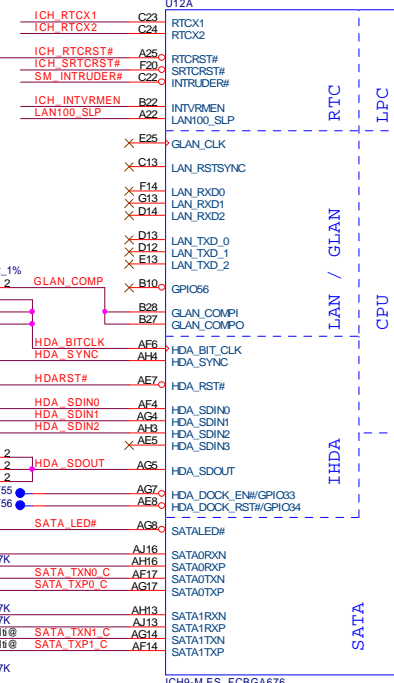
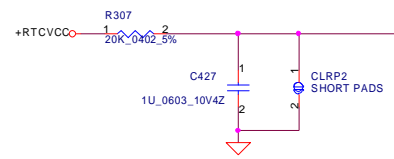
Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





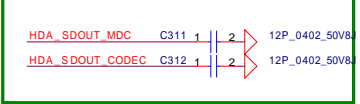
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



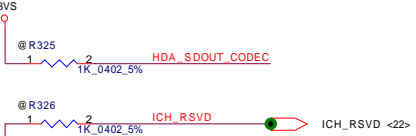
P-HDD

ODD
e-SATA
De-feature disable

Add 12p on HDA_SDOU and HDA_SDOU0T

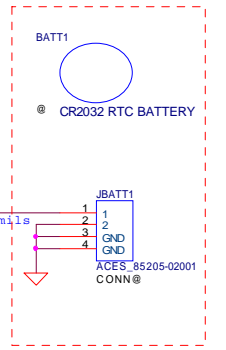
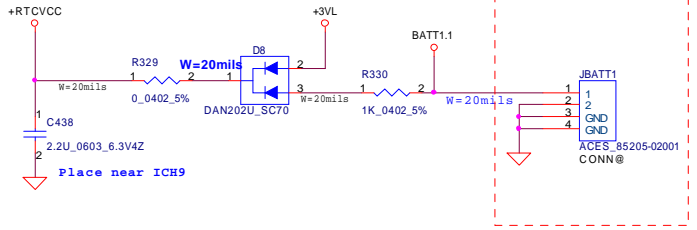
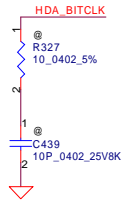
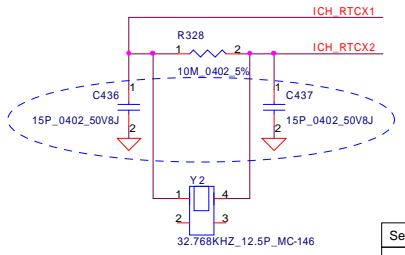


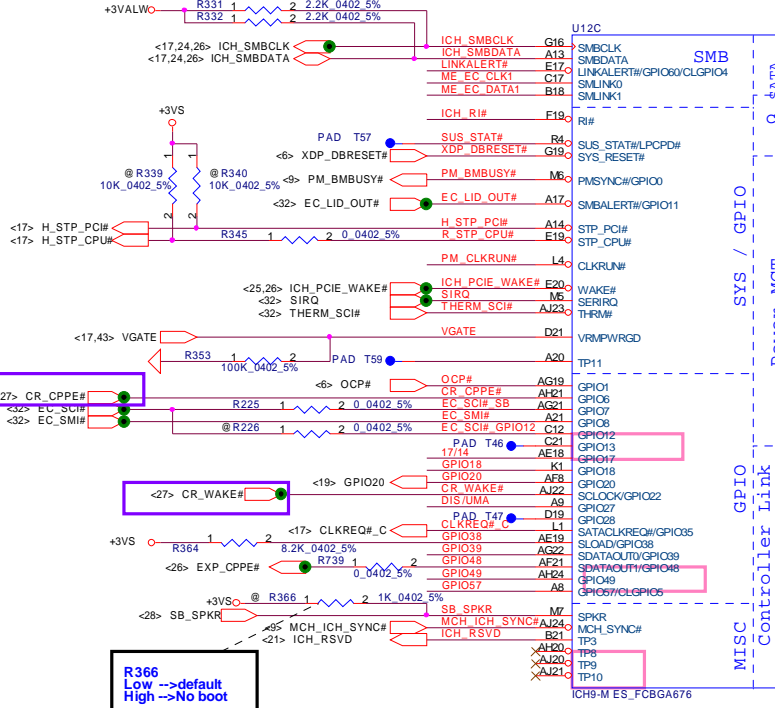
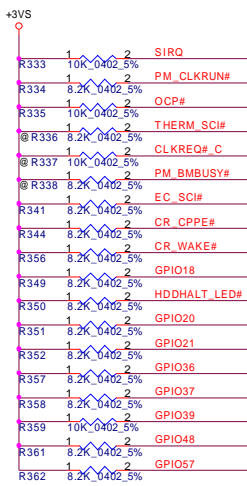
XOR CHAIN ENTRANCE STRAP:RSVD



ICH_RSVD	HDA_SDOU_CODEC
0	0
0	1
1	0
1	1

0821 Change C528 and C516 to 15PF





R366 Low -> default High -> No boot

11/17 Swap PCIE LAN and New card

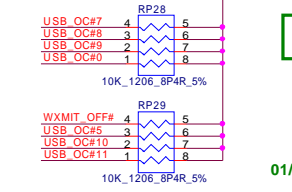
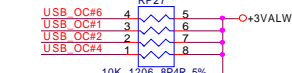
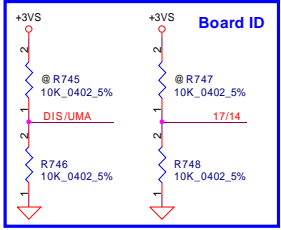
WLAN

LAN

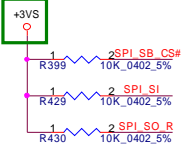
Card Reader

New Card

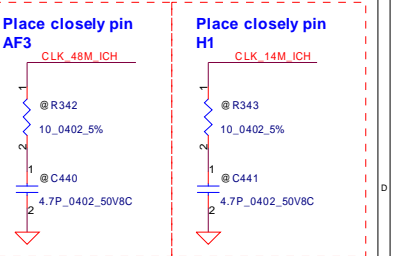
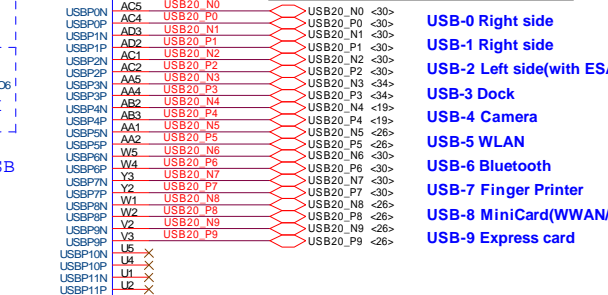
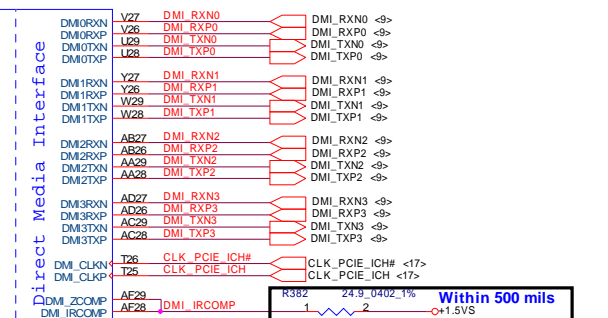
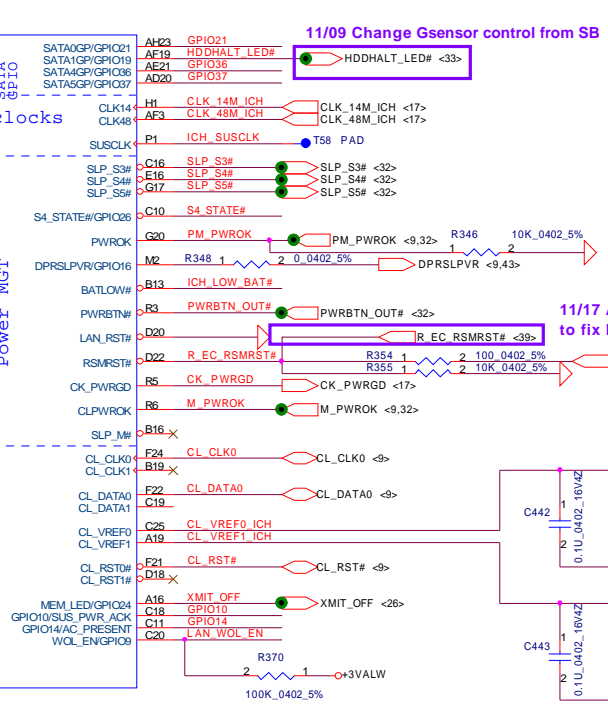
11/20 Add HDCP ROM for ICH9M



01/03 Change HDCP ROM to +3VS

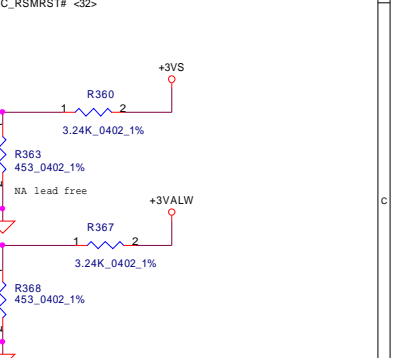


Within 500 mils



Place closely pin AF3

Place closely pin H1



Within 500 mils

- USB-0 Right side
- USB-1 Right side
- USB-2 Left side(with ESATA)
- USB-3 Dock
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8 MiniCard(WWAN/TV)
- USB-9 Express card

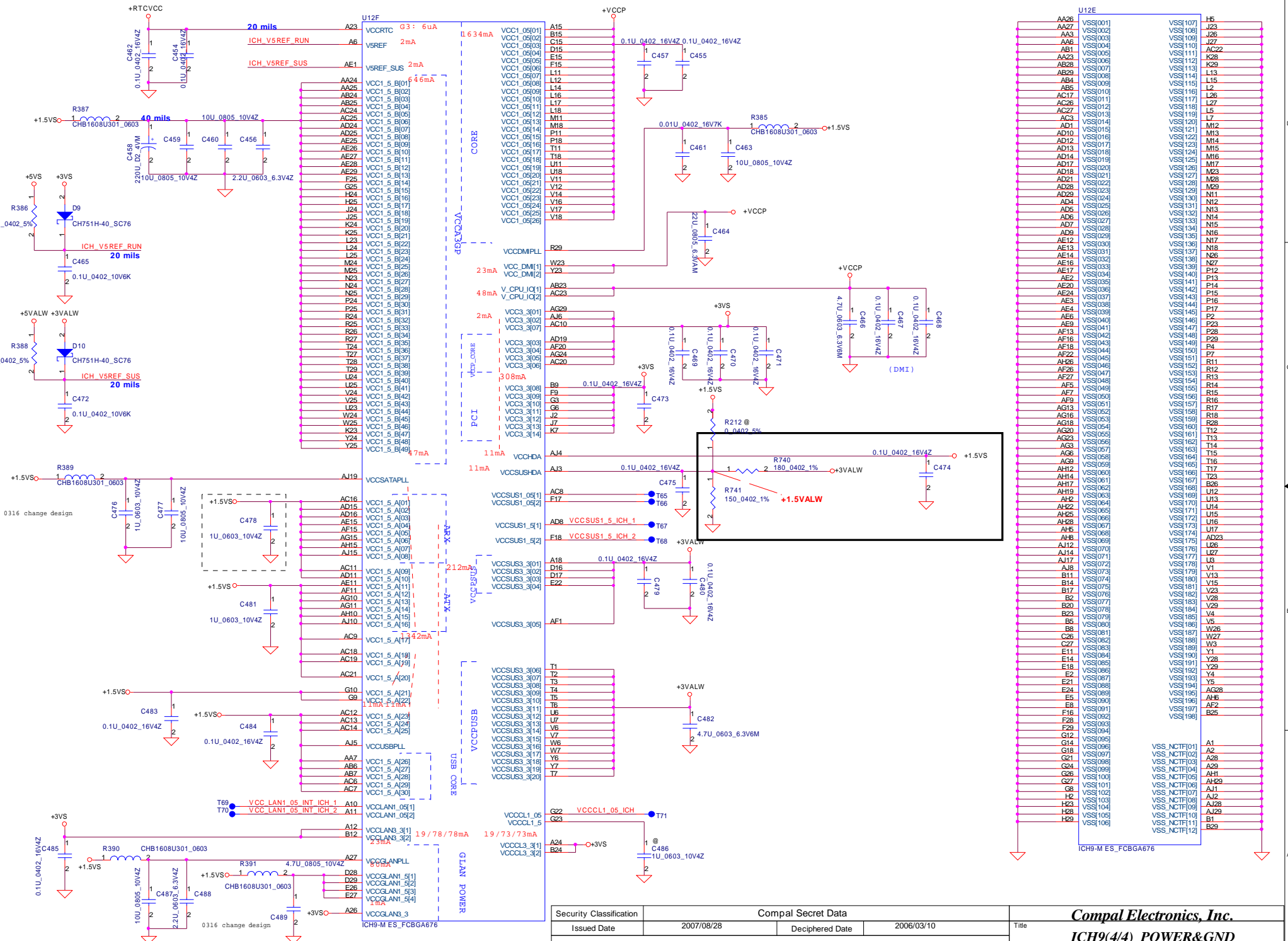
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Issued Date	2007/08/28	Deciphered Date
		2006/03/10

Compal Electronics, Inc.

ICH9(3/4) DMI,USB,GPIO,PCIE

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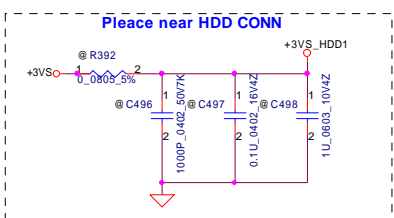
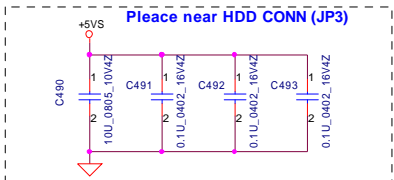
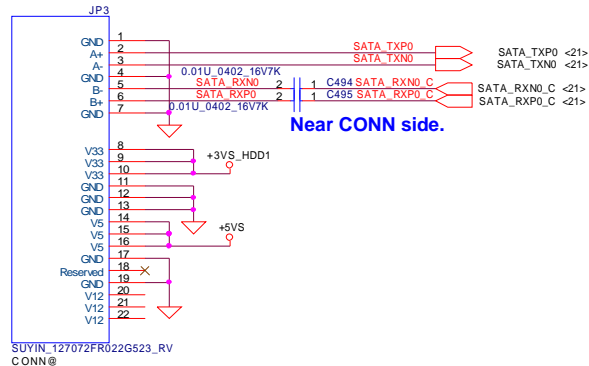
Size	Document Number	Rev
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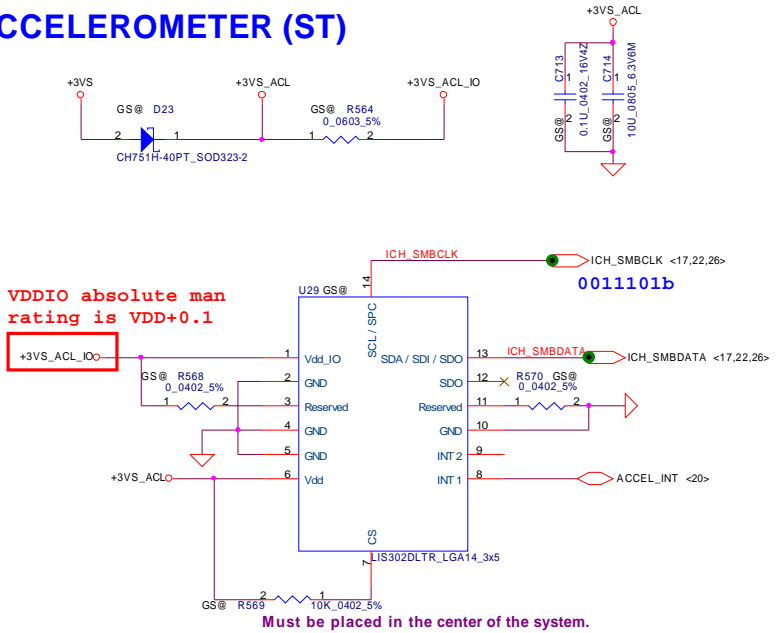
U12E	Pin	Signal	Pin	Signal
AA26	VSS[001]	VSS[107]	H5	
AA27	VSS[002]	VSS[108]	J23	
AA3	VSS[003]	VSS[109]	J26	
AA6	VSS[004]	VSS[110]	J27	
AB1	VSS[005]	VSS[111]	AC22	
AA23	VSS[006]	VSS[112]	K28	
AB28	VSS[007]	VSS[113]	K29	
AB29	VSS[008]	VSS[114]	L13	
AB4	VSS[009]	VSS[115]	L15	
AB6	VSS[010]	VSS[116]	L2	
AC17	VSS[011]	VSS[117]	L26	
AC26	VSS[012]	VSS[118]	L27	
AC27	VSS[013]	VSS[119]	L7	
AC3	VSS[014]	VSS[120]	M12	
AD1	VSS[015]	VSS[121]	M13	
AD10	VSS[016]	VSS[122]	M14	
AD12	VSS[017]	VSS[123]	M15	
AD13	VSS[018]	VSS[124]	M16	
AD14	VSS[019]	VSS[125]	M17	
AD17	VSS[020]	VSS[126]	M28	
AD18	VSS[021]	VSS[127]	M29	
AD21	VSS[022]	VSS[128]	M30	
AD28	VSS[023]	VSS[129]	N12	
AD29	VSS[024]	VSS[130]	N11	
AD4	VSS[025]	VSS[131]	N12	
AD6	VSS[026]	VSS[132]	N14	
AD7	VSS[028]	VSS[134]	N15	
AD9	VSS[029]	VSS[135]	N16	
AE12	VSS[030]	VSS[136]	N17	
AE13	VSS[031]	VSS[137]	N27	
AE14	VSS[032]	VSS[138]	N26	
AE16	VSS[033]	VSS[139]	N27	
AE17	VSS[034]	VSS[140]	P12	
AE2	VSS[035]	VSS[141]	P13	
AE3	VSS[036]	VSS[142]	P14	
AE37	VSS[037]	VSS[143]	P15	
AE4	VSS[038]	VSS[144]	P16	
AE9	VSS[039]	VSS[145]	P2	
AF1	VSS[040]	VSS[146]	P23	
AF16	VSS[042]	VSS[148]	P29	
AF18	VSS[043]	VSS[149]	P4	
AF22	VSS[044]	VSS[150]	P7	
AF24	VSS[045]	VSS[151]	R11	
AF25	VSS[046]	VSS[152]	R12	
AF27	VSS[047]	VSS[153]	R13	
AF28	VSS[048]	VSS[154]	R14	
AF5	VSS[049]	VSS[155]	R15	
AF7	VSS[050]	VSS[156]	R16	
AF9	VSS[051]	VSS[157]	R17	
AG13	VSS[052]	VSS[158]	R18	
AG16	VSS[053]	VSS[159]	R18	
AG18	VSS[054]	VSS[160]	R28	
AG20	VSS[055]	VSS[161]	T12	
AG23	VSS[056]	VSS[162]	T13	
AG3	VSS[057]	VSS[163]	T14	
AG6	VSS[058]	VSS[164]	T15	
AH1	VSS[059]	VSS[165]	T16	
AH12	VSS[060]	VSS[166]	T17	
AH14	VSS[061]	VSS[167]	T23	
AH17	VSS[062]	VSS[167]	B26	
AH18	VSS[063]	VSS[168]	U12	
AH22	VSS[064]	VSS[169]	U13	
AH25	VSS[065]	VSS[170]	U14	
AH28	VSS[066]	VSS[171]	U15	
AH5	VSS[067]	VSS[172]	U16	
AH8	VSS[068]	VSS[173]	U17	
AH12	VSS[069]	VSS[174]	AD23	
AH14	VSS[070]	VSS[175]	U26	
AH17	VSS[071]	VSS[176]	U27	
AH22	VSS[072]	VSS[177]	U3	
B11	VSS[073]	VSS[178]	V1	
B14	VSS[074]	VSS[179]	V13	
B17	VSS[075]	VSS[180]	V22	
B2	VSS[076]	VSS[181]	V28	
B20	VSS[077]	VSS[182]	V29	
B23	VSS[078]	VSS[183]	V4	
B8	VSS[079]	VSS[184]	V5	
C26	VSS[080]	VSS[185]	W26	
C27	VSS[081]	VSS[186]	W27	
E11	VSS[082]	VSS[187]	W3	
E14	VSS[083]	VSS[188]	Y1	
E18	VSS[084]	VSS[189]	Y28	
E21	VSS[085]	VSS[190]	Y29	
E23	VSS[086]	VSS[191]	Y3	
E24	VSS[087]	VSS[192]	Y5	
E5	VSS[088]	VSS[193]	AC28	
E8	VSS[089]	VSS[194]	AH6	
F18	VSS[090]	VSS[195]	AH23	
F29	VSS[091]	VSS[196]	AF2	
G12	VSS[092]	VSS[197]	B25	
G14	VSS[093]	VSS[198]		
G18	VSS[094]	VSS[096]	VSS_NCTF[01]	A1
G21	VSS[095]	VSS[097]	VSS_NCTF[02]	A2
G24	VSS[096]	VSS[098]	VSS_NCTF[03]	A28
G26	VSS[097]	VSS[099]	VSS_NCTF[04]	A29
G27	VSS[100]	VSS[100]	VSS_NCTF[05]	AH
G8	VSS[101]	VSS[101]	VSS_NCTF[06]	AH23
H2	VSS[102]	VSS[102]	VSS_NCTF[07]	AJ1
H23	VSS[103]	VSS[103]	VSS_NCTF[08]	AJ2
H28	VSS[104]	VSS[104]	VSS_NCTF[09]	AJ28
H29	VSS[105]	VSS[105]	VSS_NCTF[10]	B1
	VSS[106]	VSS[106]	VSS_NCTF[11]	B2
			VSS_NCTF[12]	

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Custom	Montevina Blade UMA LA410IP	Saturday, January 05, 2008	0.3

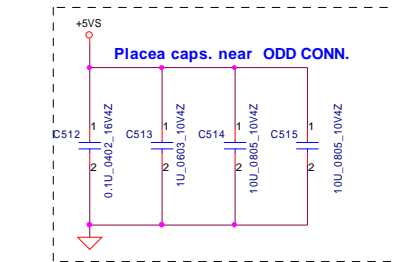
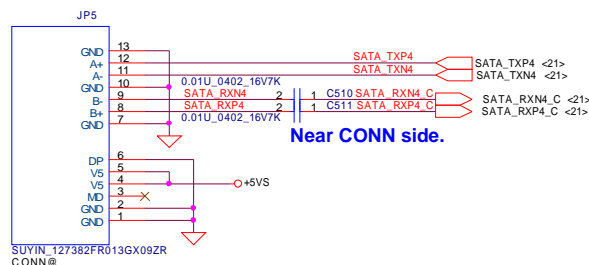
HDD Connector



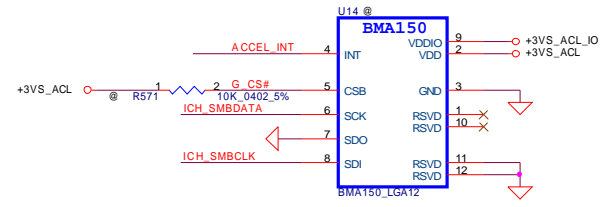
ACCELEROMETER (ST)



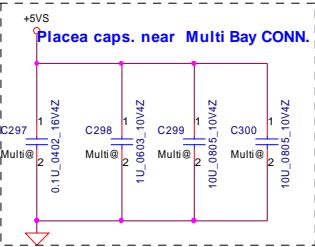
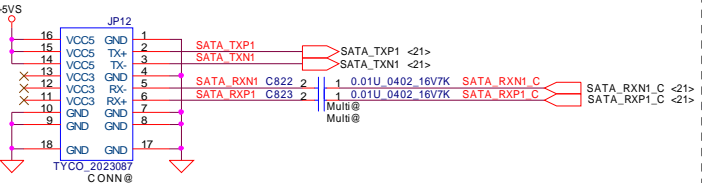
CD-ROM Connector



ACCELEROMETER (Bosch)

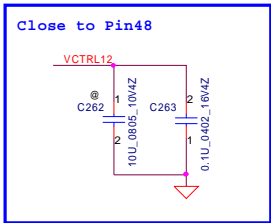
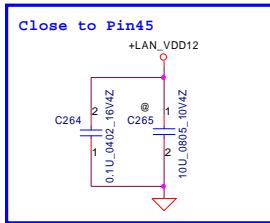
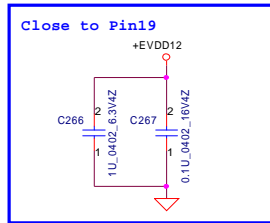
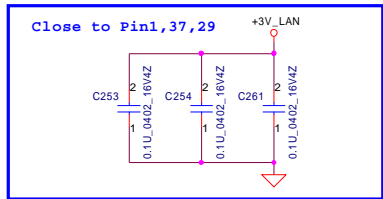
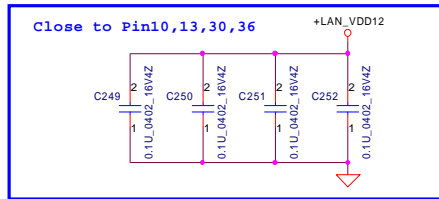
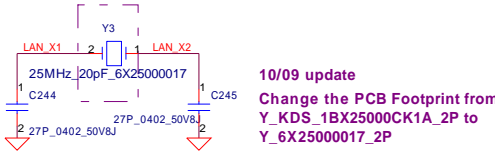
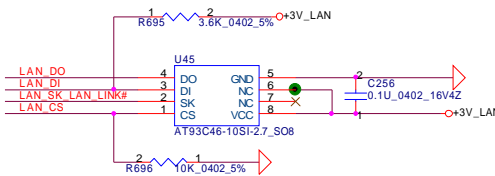
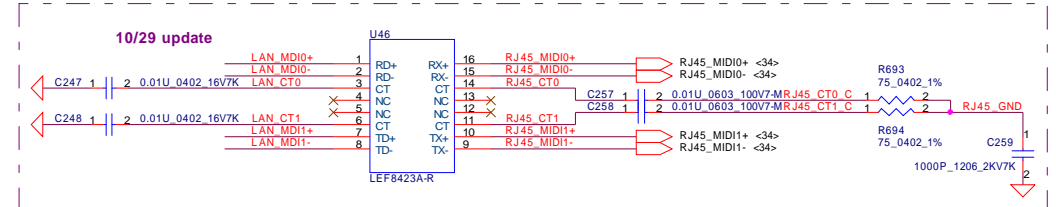
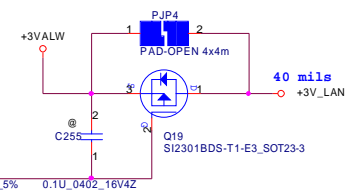
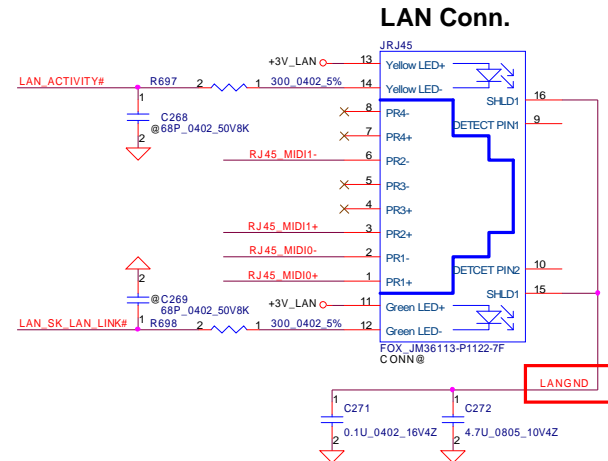
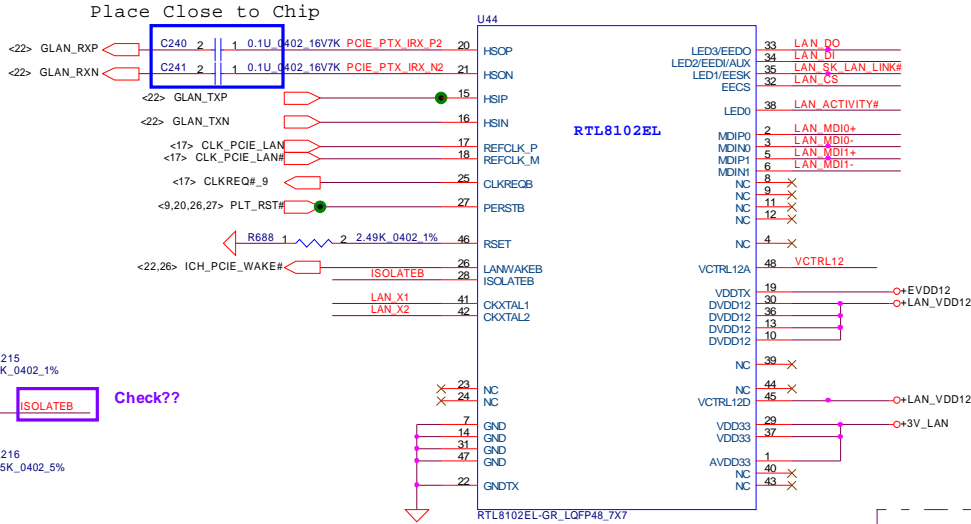


Multi Bay



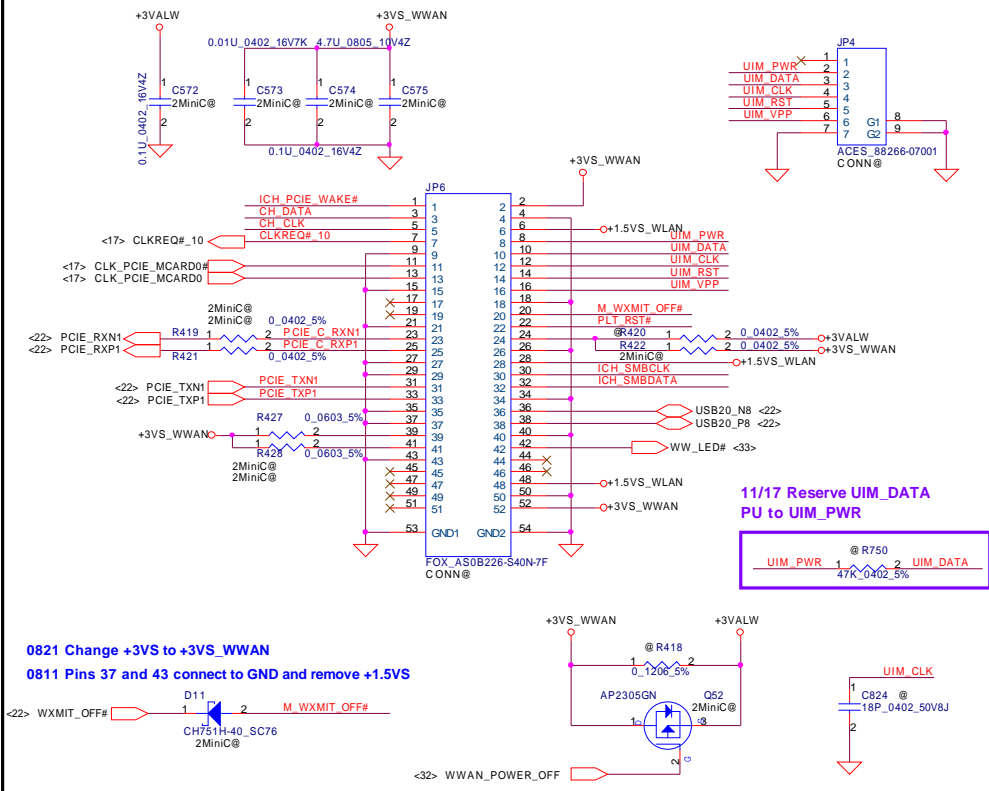
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Compal Electronics, Inc.	
HDD & CDROM	
Size	Document Number
Custom	Montevina Blade UMA LA410IP
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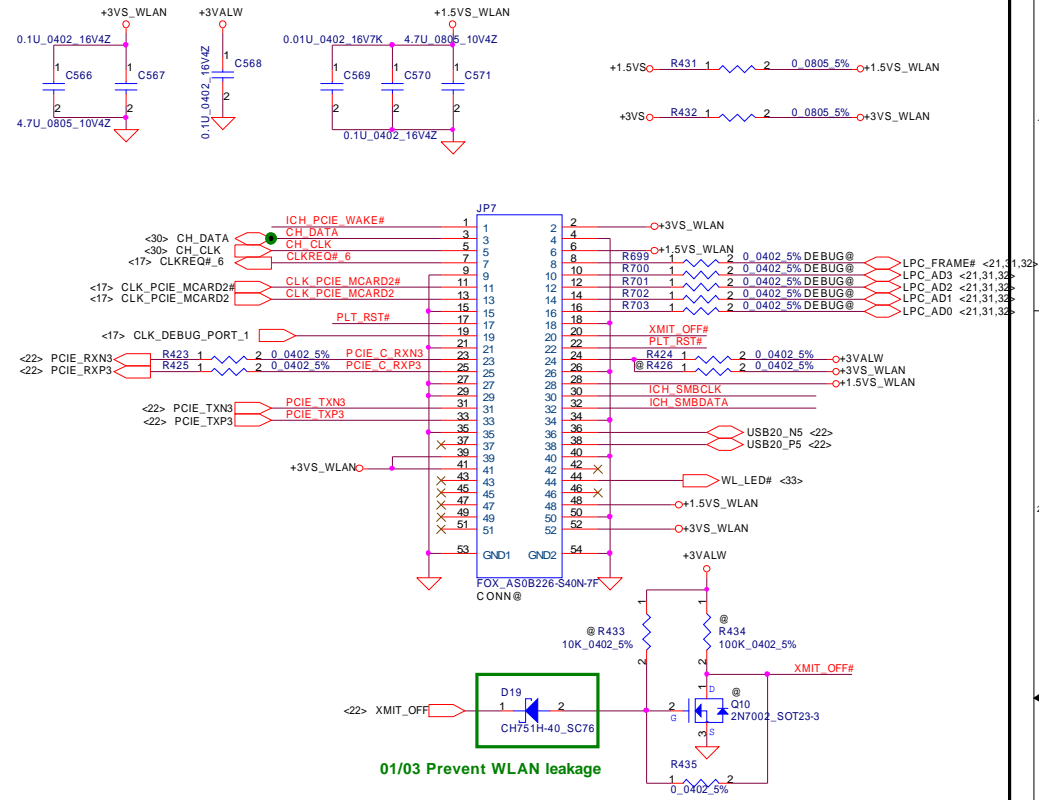


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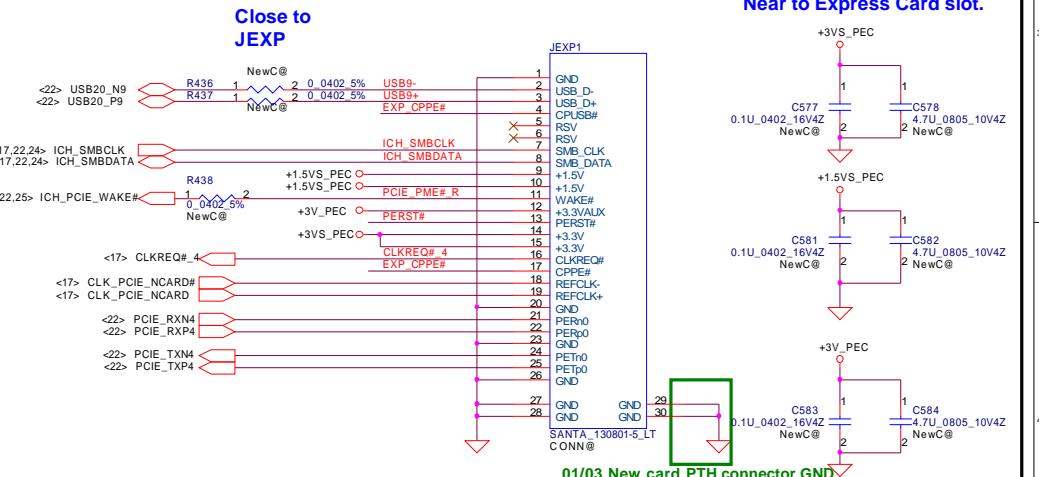
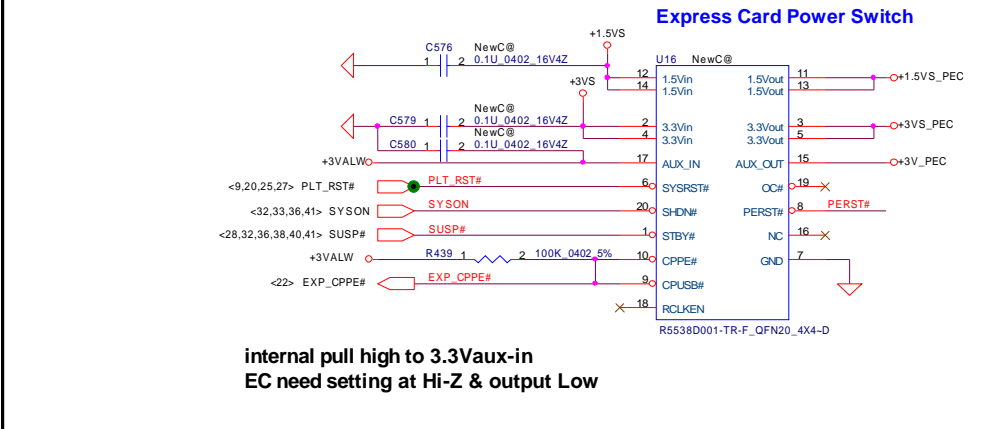
Mini Card 0--TV tuner/WWAN/Robson SIM card Connector



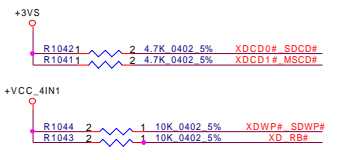
Mini Card 2---WLAN



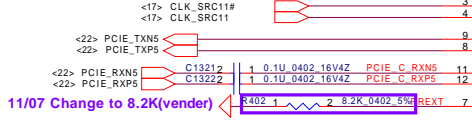
New Card



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Date:	Saturday, January 05, 2008	Sheet	26 of 46

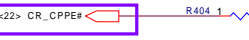


09/26 (JMicron)recommend width/length: 12mil / <250mil for PREXT signal (pin 7)



11/07 Change to 8.2K(vender)

09/26 (JMicron)recommend add a test point for pin 13 - 14



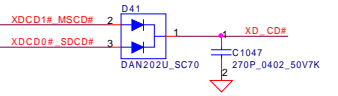
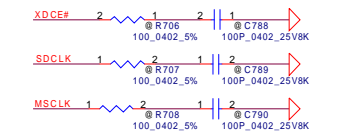
11/09 Add D18 for cardreader wake up

use for PWR_EN#
CR_LED#
8mA sink current



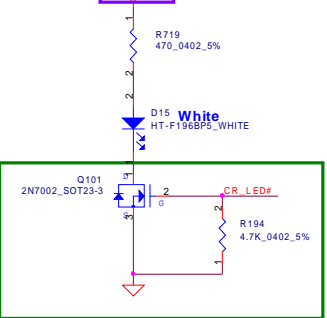
11/07 Change to 10K(vender)

01/03 Change Cardreader LED control

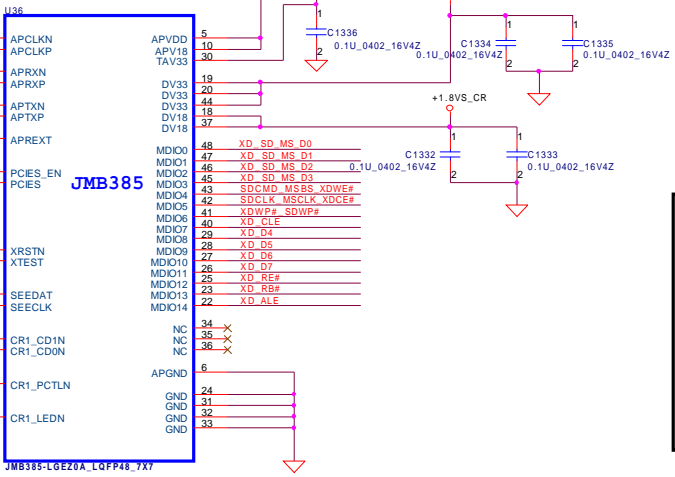


White LED: VF=3V, IF = 5mA, Res = 56ohm

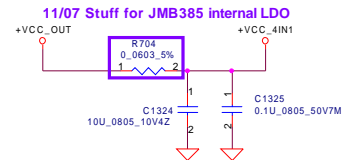
11/09 don't support DIM function



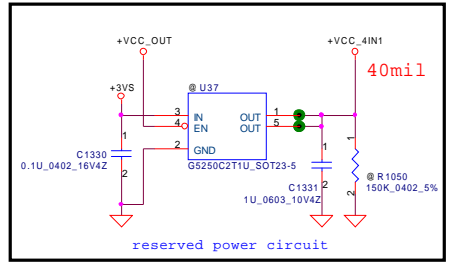
01/03 Change Cardreader LED control



09/26 (JMicron)recommend C1328/1000pF close to U36 pin5
09/26 (JMicron)recommend place C1329/0.1uF near by C1328
09/26 (JMicron)recommend (APVDD, 20 mil width, less than 120mil long)

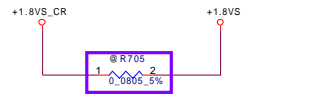


Use 0603 type and over 20 mils trace width on both side
09/26 (JMicron)recommend change to 0805 size
09/26 (JMicron)recommend +VCC_OUT >30mil



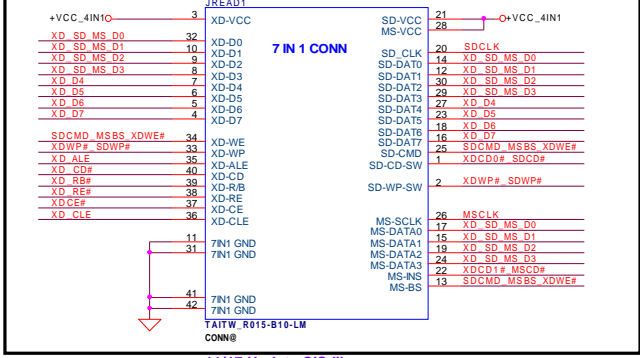
11/07 Change U37 correct PCBFootprint SOT23
11/07 BOM delete for JMB385 internal LDO

09/26 Must change P mos FET



11/07 Don't stuff for JMB385 internal LDO

Card Reader Connector

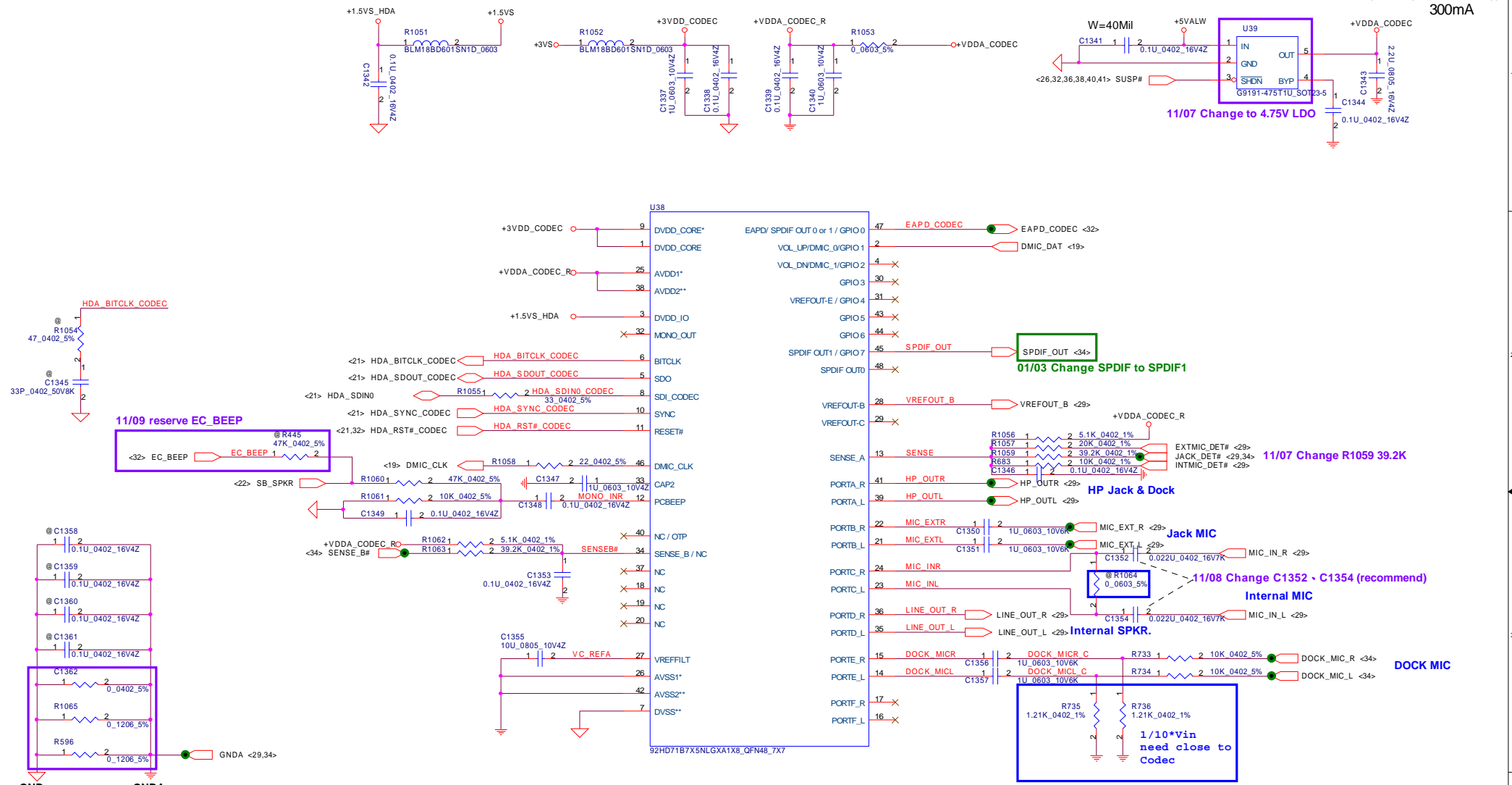


11/17 Update CIS library

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CODEC POWER

(4.75V(4.56~4.94V))
300mA

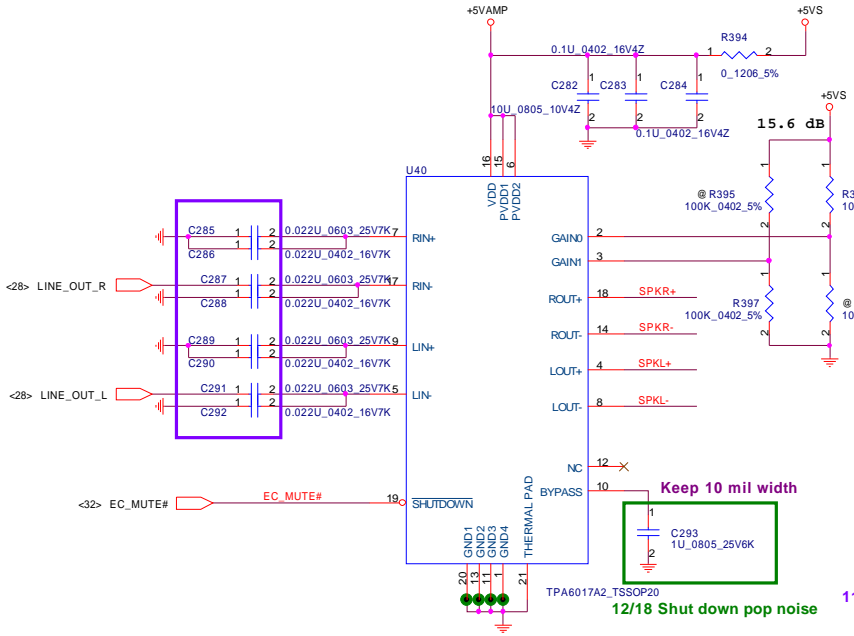


11/07 Stuff 0 Ohm for AGND and GND

SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

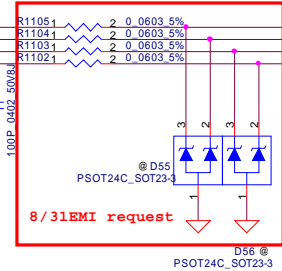
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Issued Date	2007/08/28	Deciphered Date	2006/07/26	Size	Document Number	Rev	
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GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



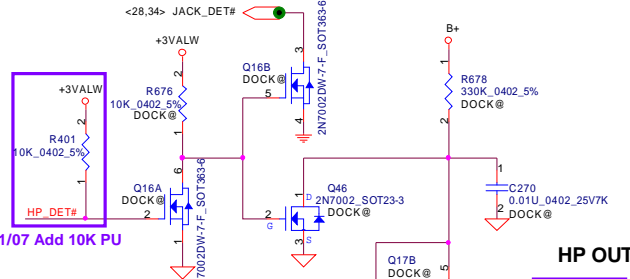
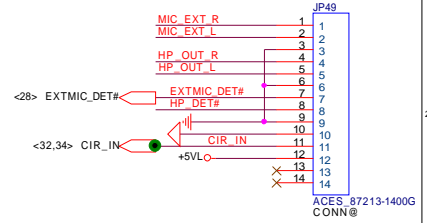
11/17 Change to 15.6 dB

SPKR+
SPKR-
SPKL+
SPKL-



11/07 Change JP60 PCB Footprint from ACES_85204-04001_4P to ACES_88231-04001_4P

Audio/B & CIR



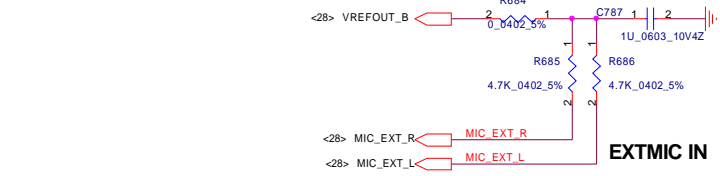
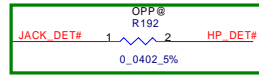
11/07 Add 10K PU

HP OUT

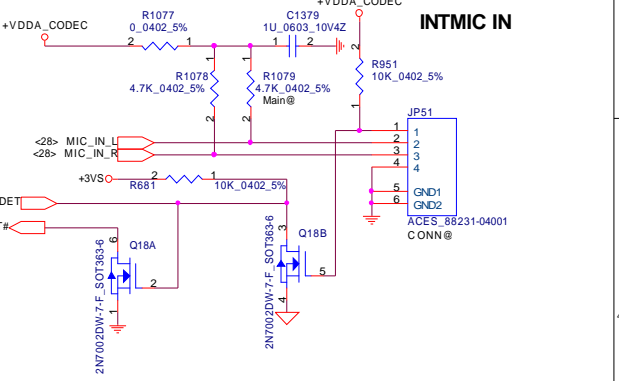
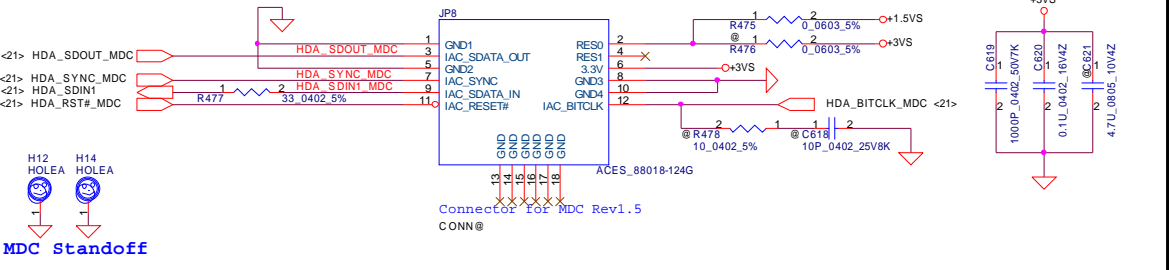
HP OUT For Docking
DOCK_LOUT_R <34>
DOCK_LOUT_L <34>

11/07 Add Capacitor avoid DC lever to Docking audio

HP OUT For M/B

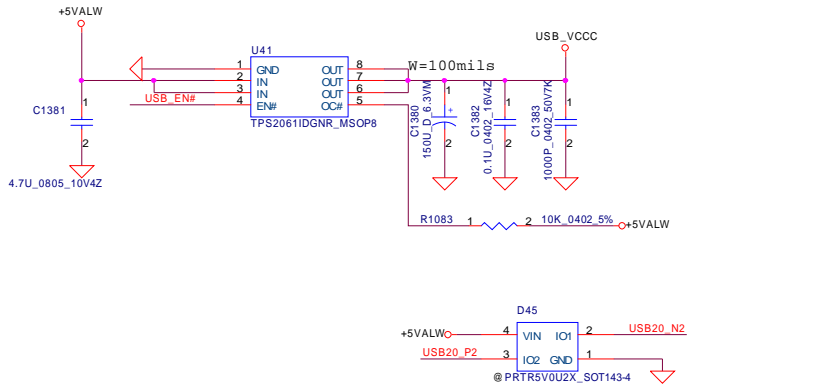


MDC 1.5 Conn.

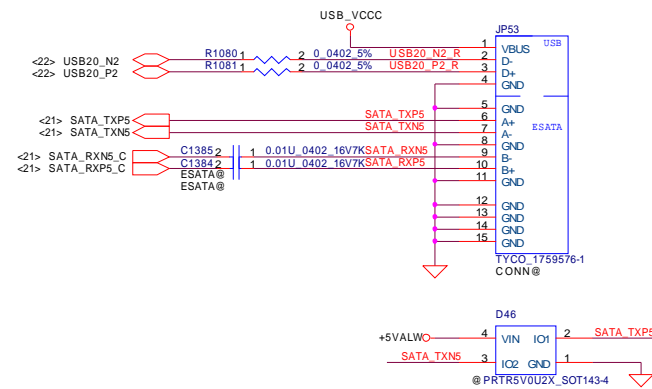


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Size	Document Number	Rev		Date	
Custom	Montevina Blade UMA LA4101P	0.3		Saturday, January 05, 2008	
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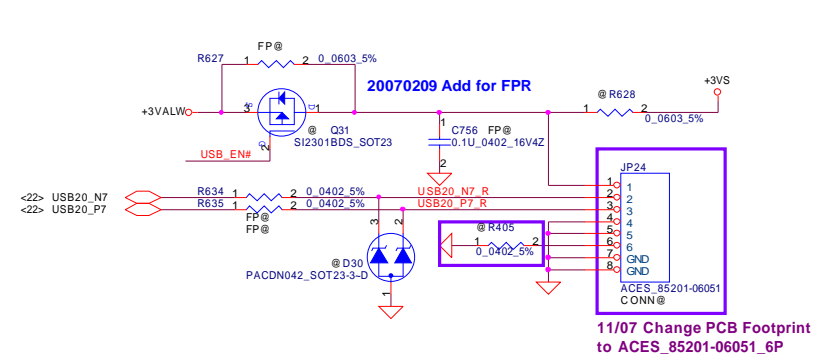
Left side USB Connector



Left side ESATA/USB combination Connector

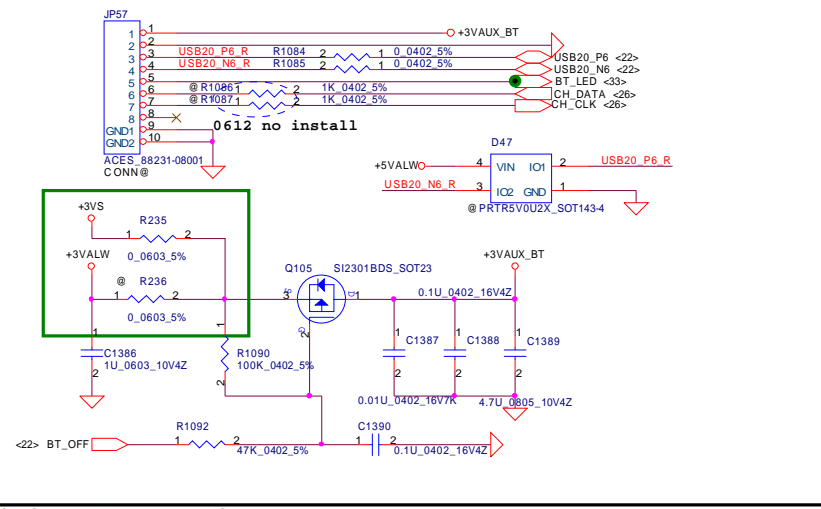


Finger printer

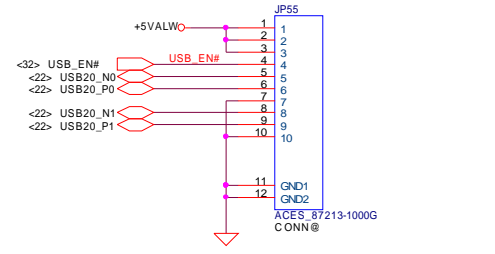


BT Connector

Need change to New version

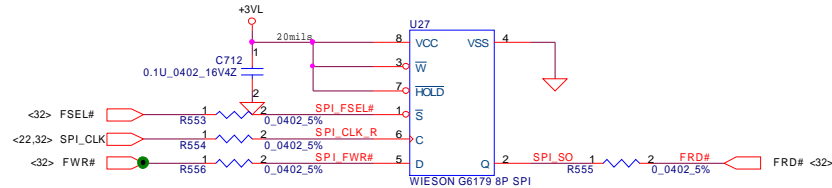


USB cable connector for Right side

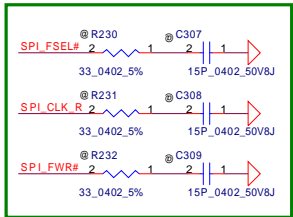


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SPI ROM

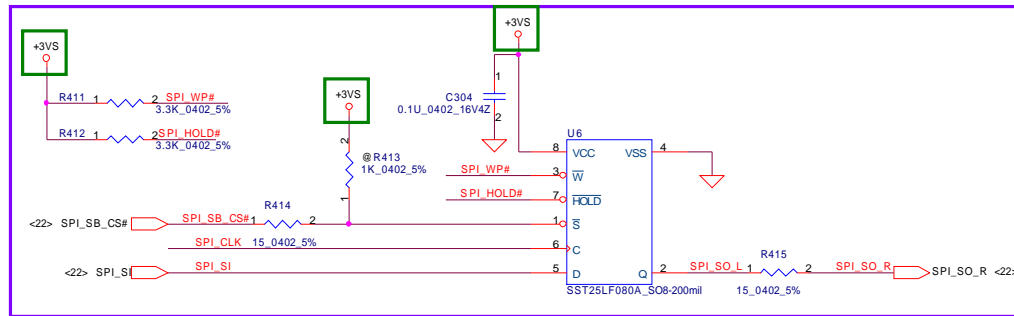
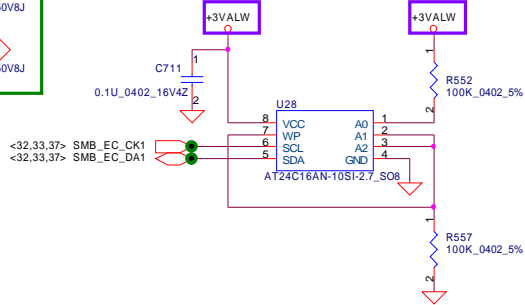


SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P



12/27EMI request

11/16 Change TO +3VALW

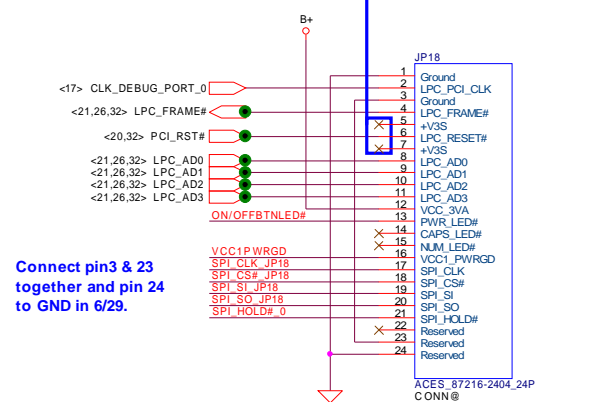


11/17 Add SB HDCP ROM

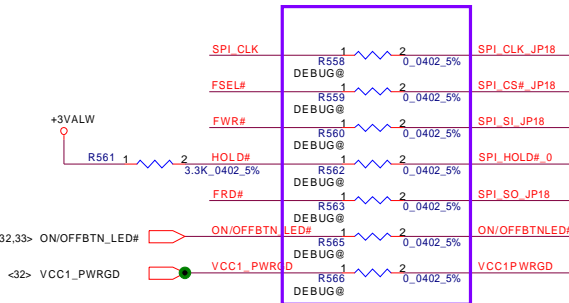
01/03 Change HDCP ROM to +3VS

LPC Debug Port

Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13

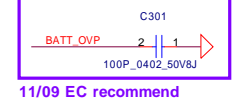
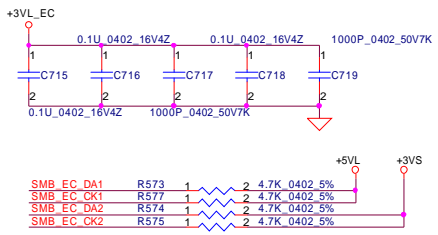


Connect pin3 & 23 together and pin 24 to GND in 6/29.

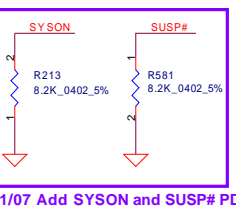
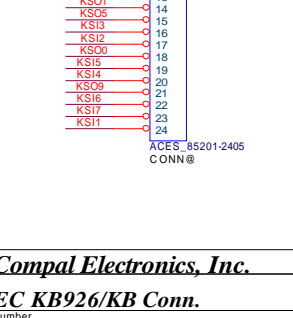
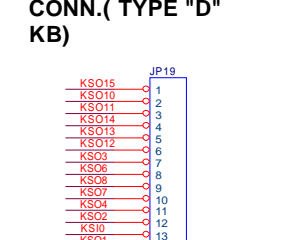
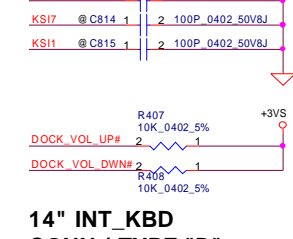
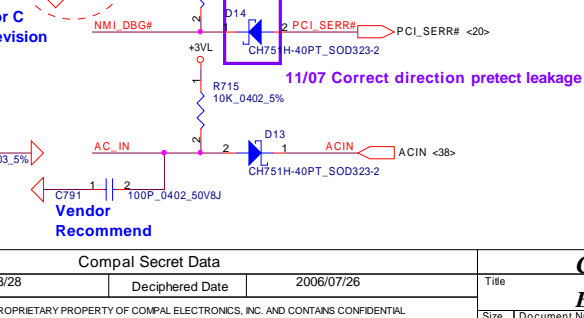
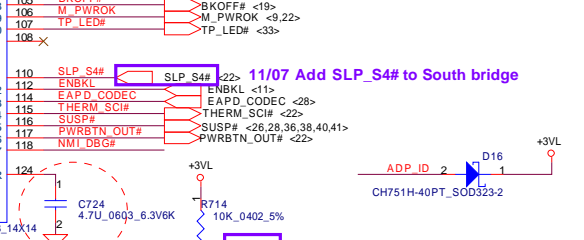
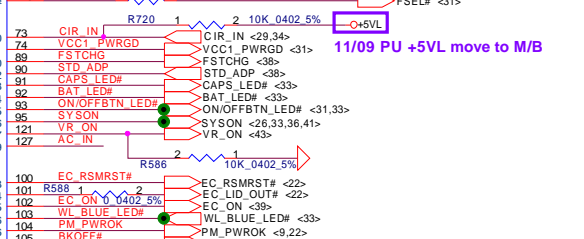
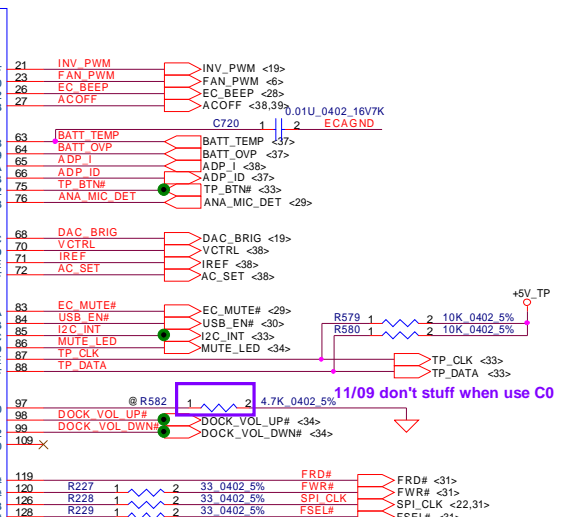
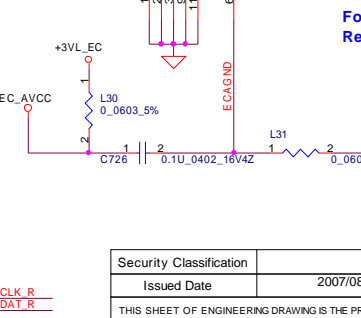
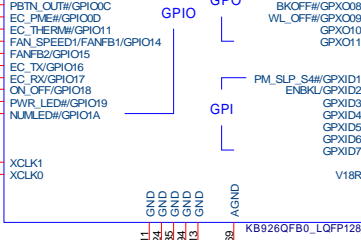
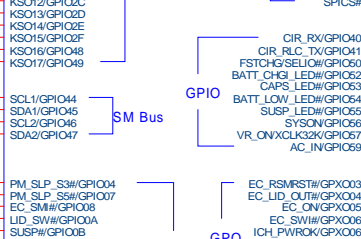
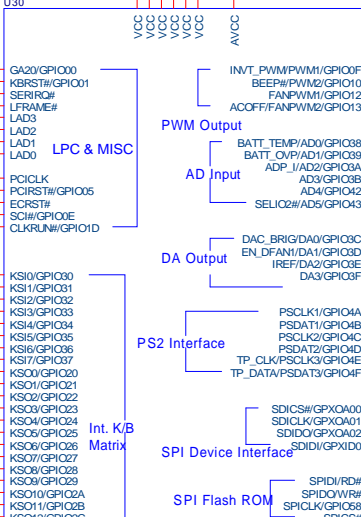
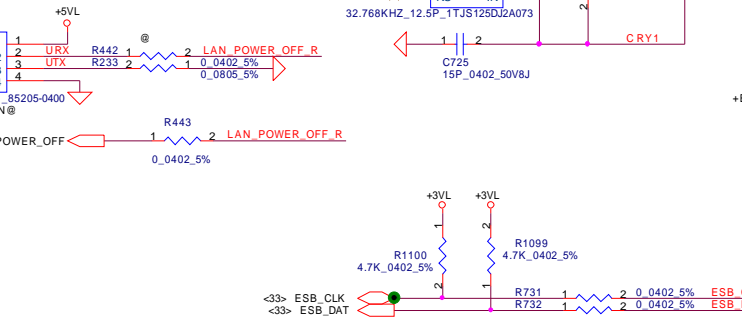
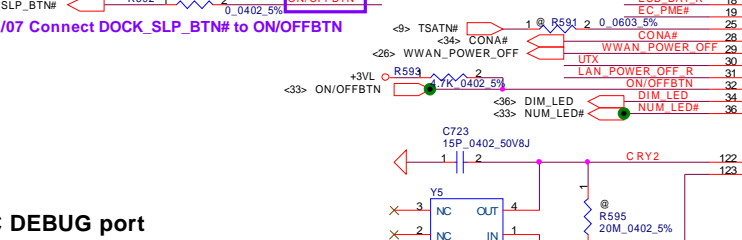
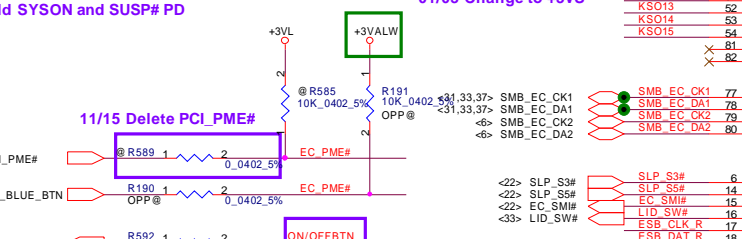
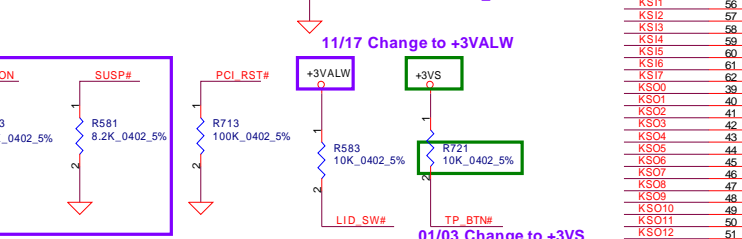
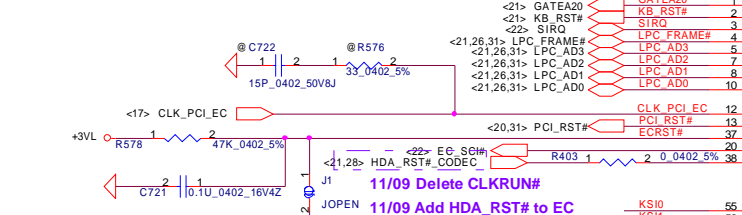


11/07 Add 0 Ohm for debug port

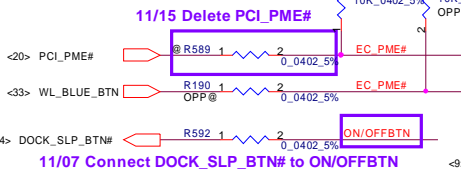
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Issued Date	2007/08/28	Deciphered Date	2006/07/26	Compal Electronics, Inc.		
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Size	Document Number	Date		Rev		
	Montevina Blade UMA LA4101P	Saturday, January 05, 2008		0.3		
Sheet 31 of 46						



- SMB_EC_DA1 R573 1 2 4.7K 0402 5%
- SMB_EC_CK1 R577 1 2 4.7K 0402 5%
- SMB_EC_DA2 R574 1 2 4.7K 0402 5%
- SMB_EC_CK2 R575 1 2 4.7K 0402 5%



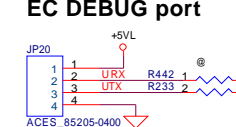
11/07 Add SYSON and SUSP# PD



11/15 Delete PCI_PME#



11/07 Connect DOCK_SLP_BTN# to ON/OFFBTN



EC DEBUB port



LAN_POWER_OFF

11/17 Change to +3VALW

11/09 Delete CLKRUN#

11/09 Add HDA_RST# to EC

11/09 don't stuff when use C0

11/09 PU +5V_L move to M/B

11/07 Add SLP_S4# to South bridge

11/07 Correct direction protect leakage

For C Revision

Vendor Recommend

11/07 Add SLP_S4# to South bridge

11/07 Correct direction protect leakage

For C Revision

Vendor Recommend

11/07 Add SLP_S4# to South bridge

11/07 Correct direction protect leakage

For C Revision

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Vendor Recommend

11/07 Add SLP_S4# to South bridge

11/07 Correct direction protect leakage

For C Revision

Vendor Recommend

11/07 Add SLP_S4# to South bridge

11/07 Correct direction protect leakage

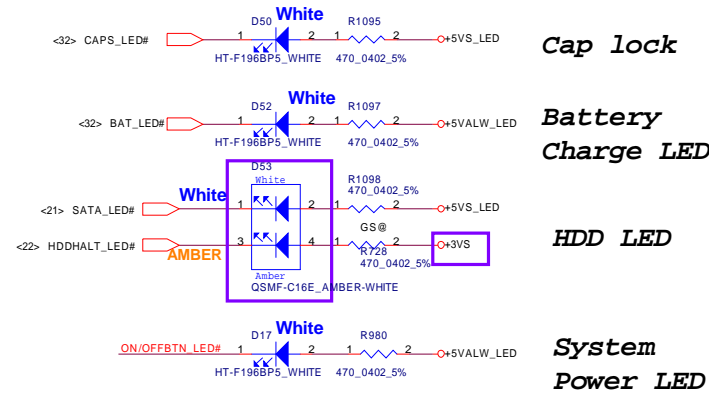
For C Revision

Vendor Recommend

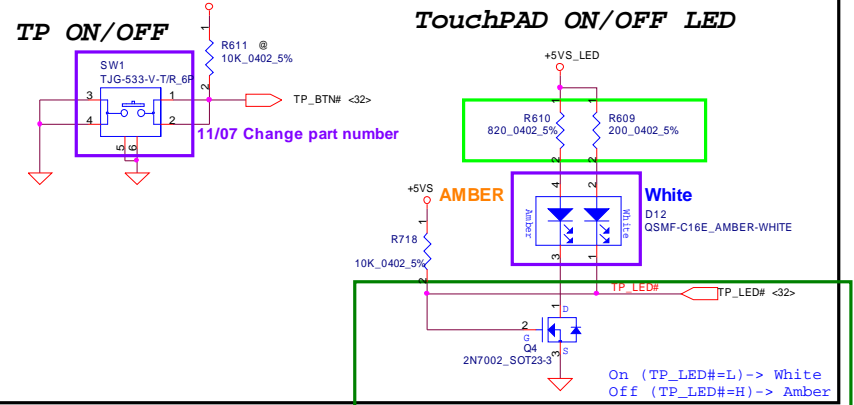
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Compal Electronics, Inc.		
EC KB926/KB Conn.		
Title	Size	Document Number
		Montevina Blade UMA LA4101P
Date	Sheet	Rev
Saturday, January 05, 2008	32 of 46	0.3

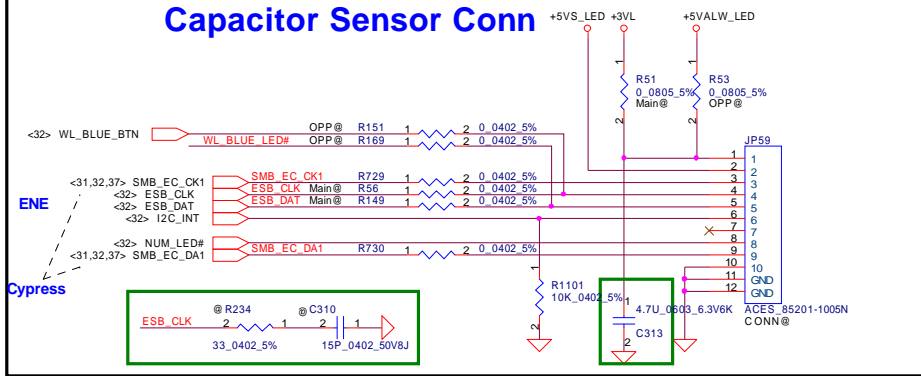
System LED



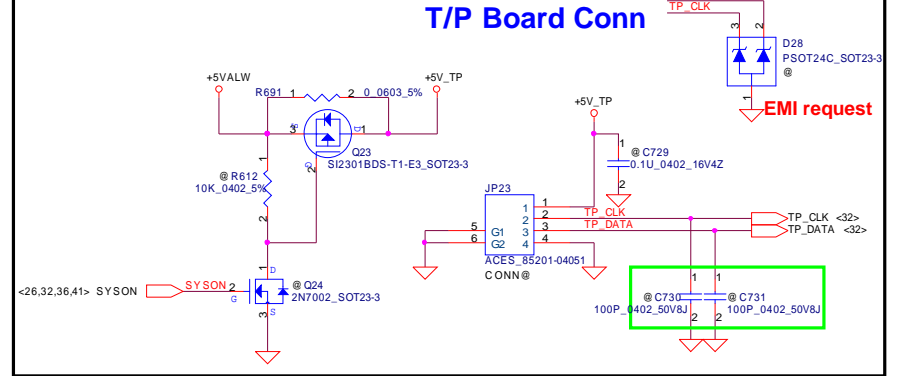
T/P Board (Include T/P_ON/OFF)



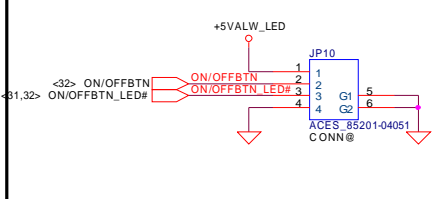
Capacitor Sensor Conn



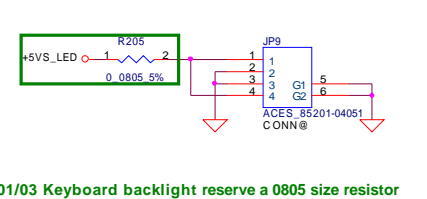
T/P Board Conn



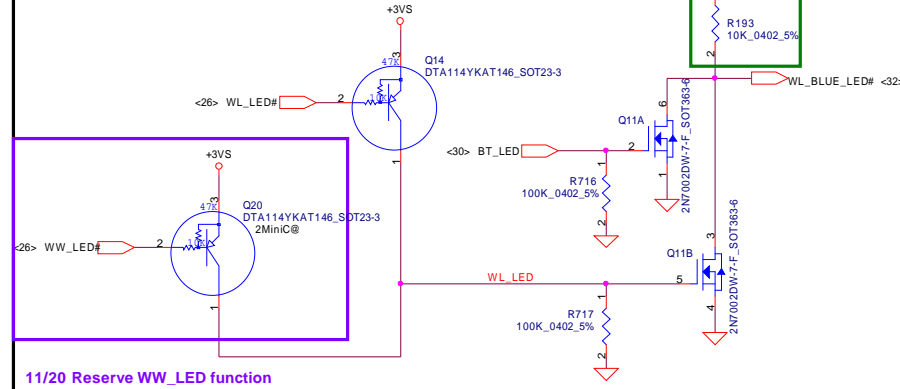
ON/OFF Button Connector



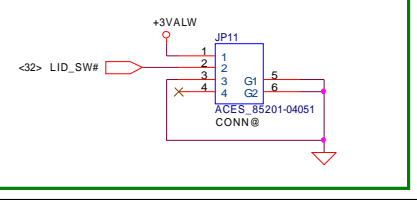
Keyboard backlight Conn



Mini card LED



Lid Switch Connector

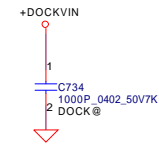
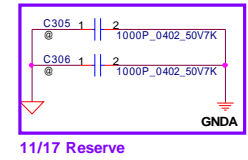
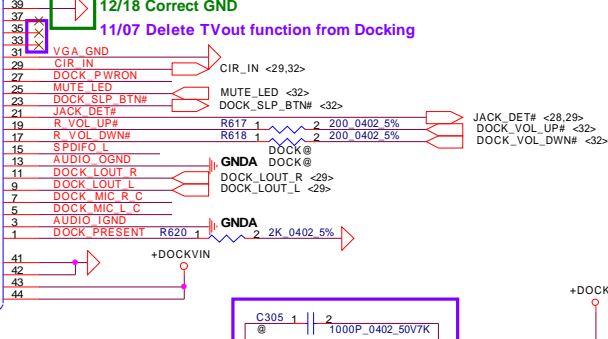
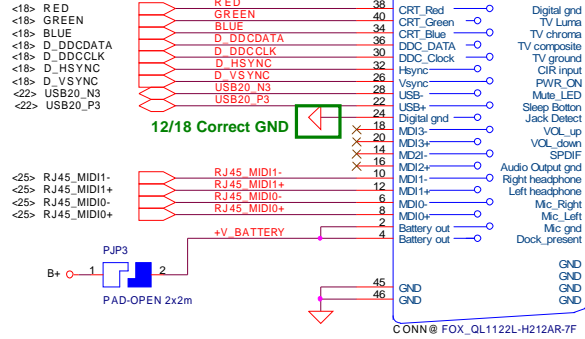
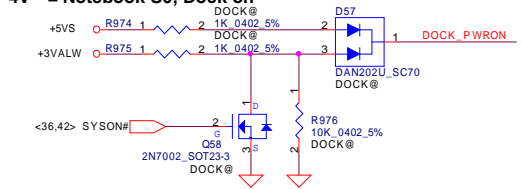


01/03 Change Lid switch connector type

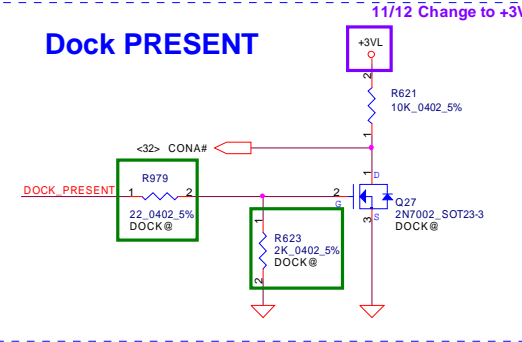
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			Montevina Blade UMA LA4101P	0.3
Date:	Saturday, January 05, 2008	Sheet	33	of 46

Atlas/ Saturn Dock

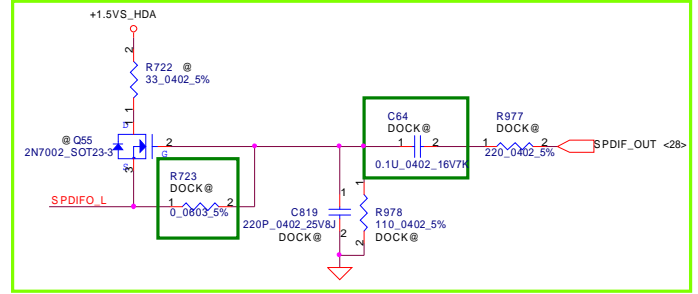
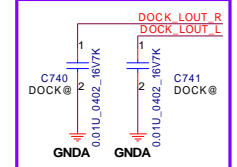
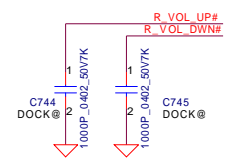
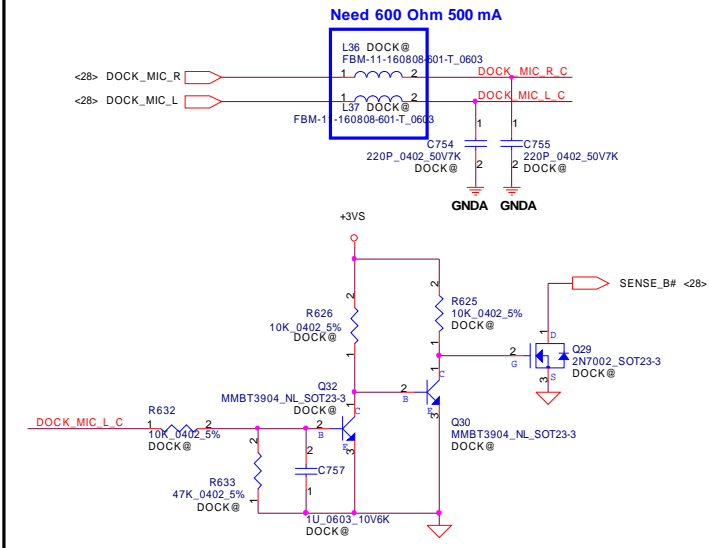
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on



Dock PRESENT

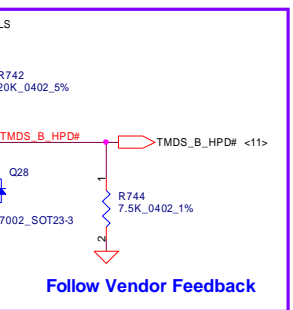
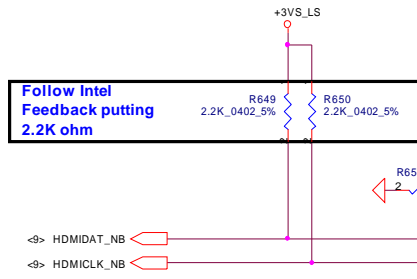


MIC_Dock

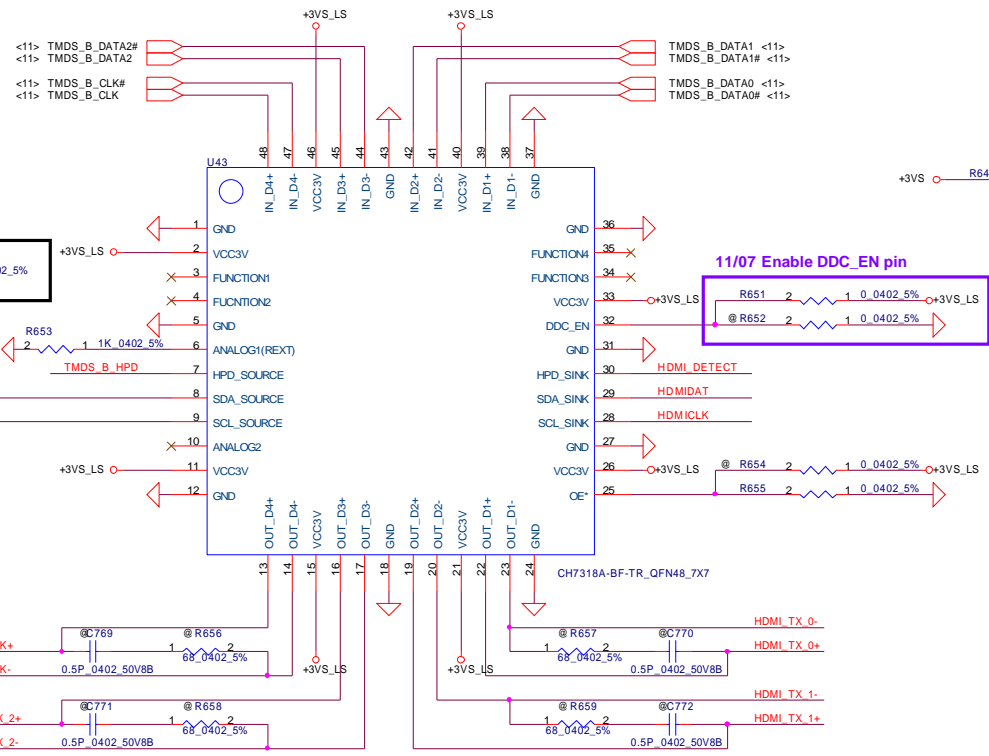


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Customer	Montevina Blade UMA LA4101P	0.3		
Date:	Saturday, January 05, 2008	Sheet	34	of 46

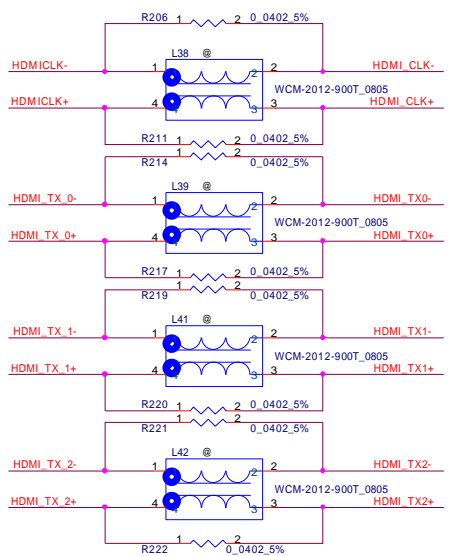
Follow Intel Feedback putting 2.2K ohm



11/07 correct TMDS_B_HPD# connection to North bridge

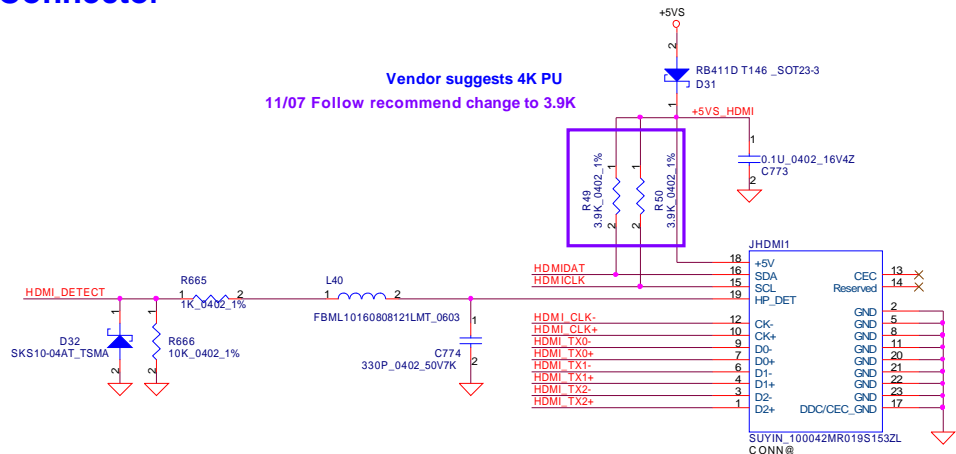


11/07 Enable DDC_EN pin



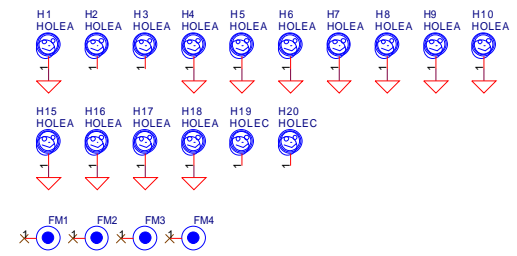
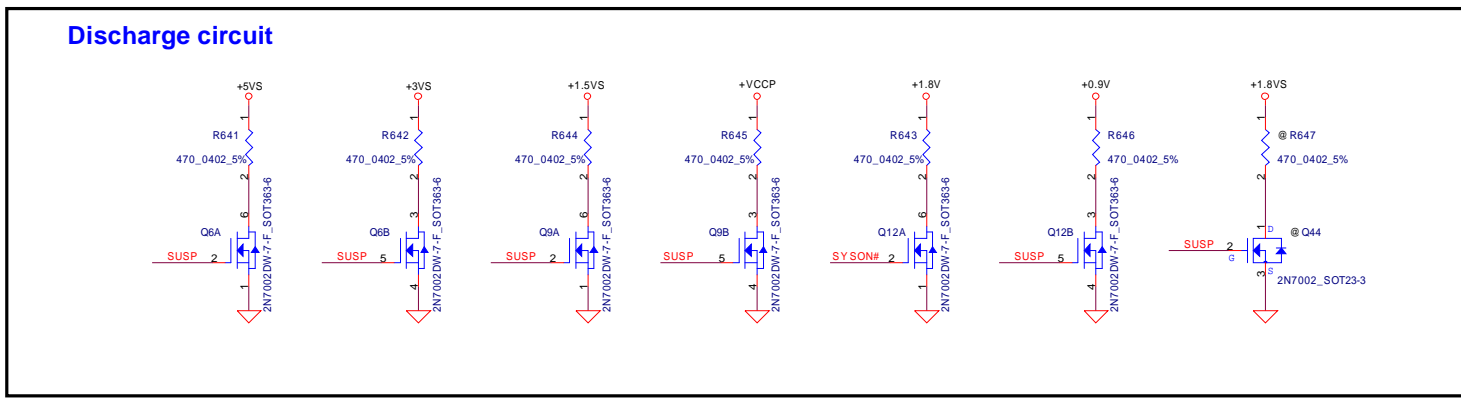
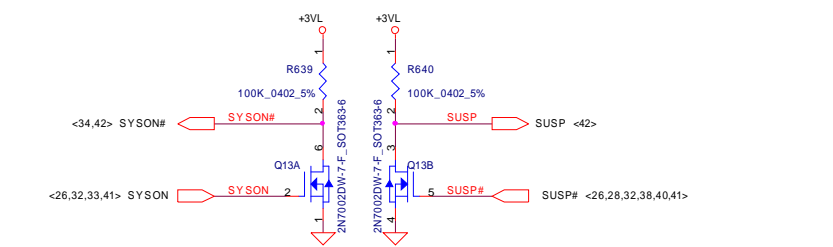
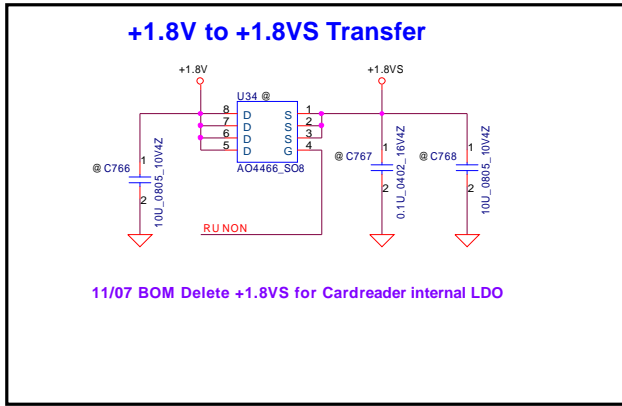
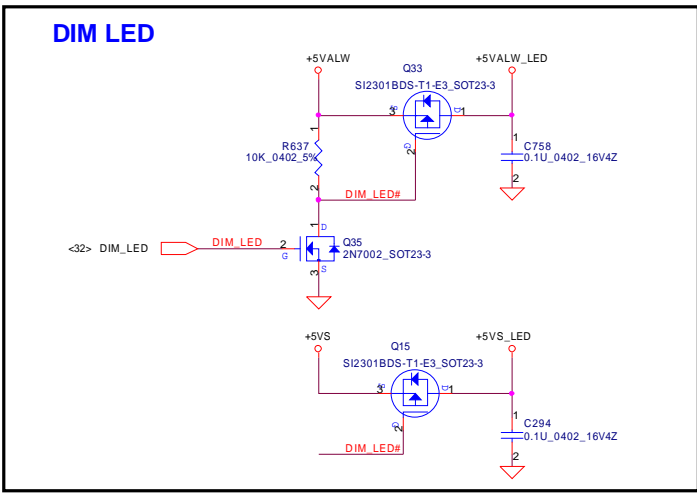
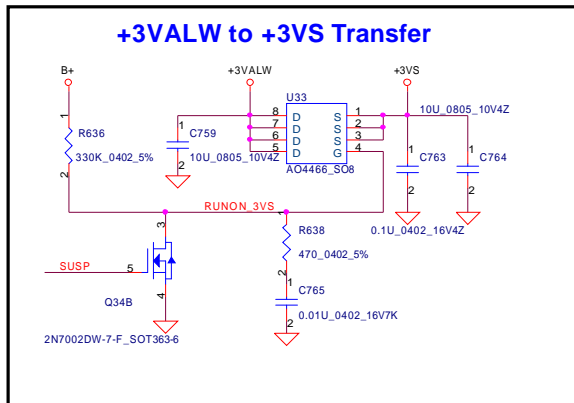
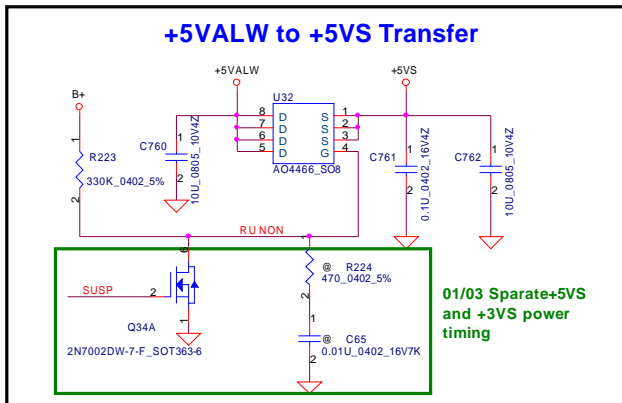
01/03 Reserver 0 ohm co lay with common choke

HDMI Connector

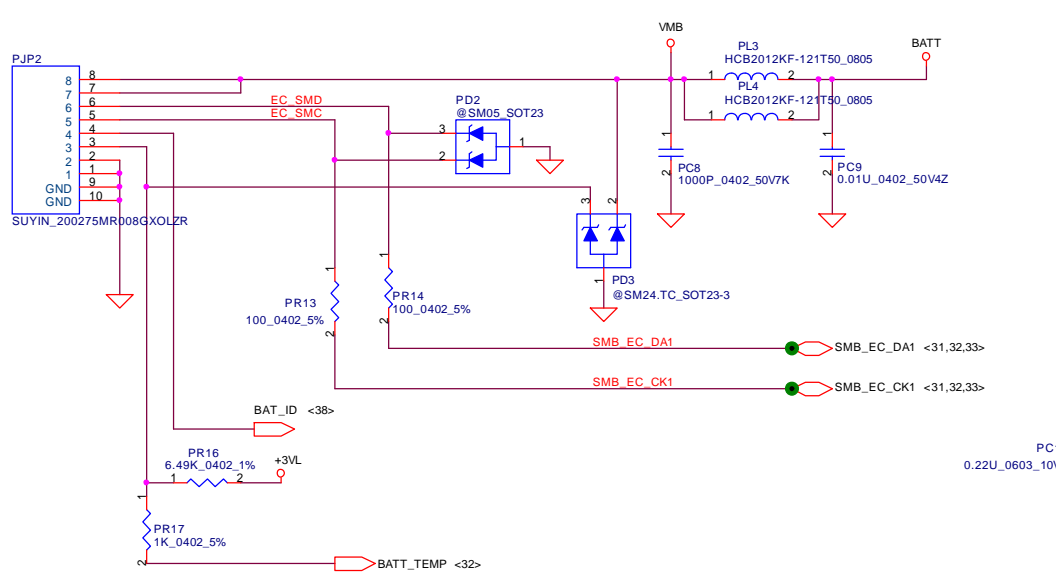
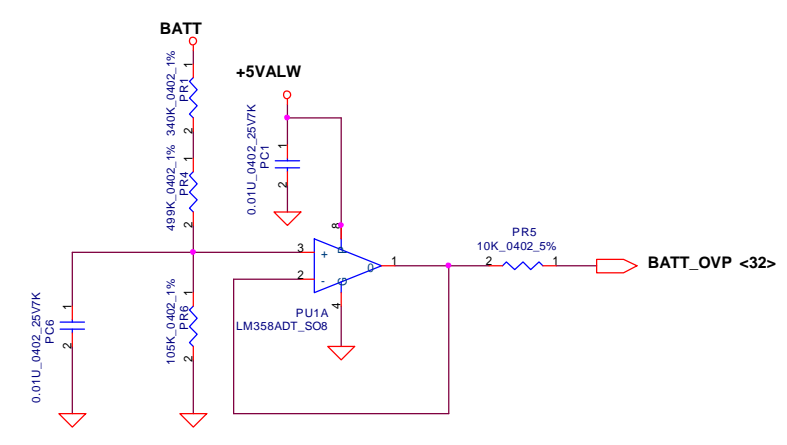
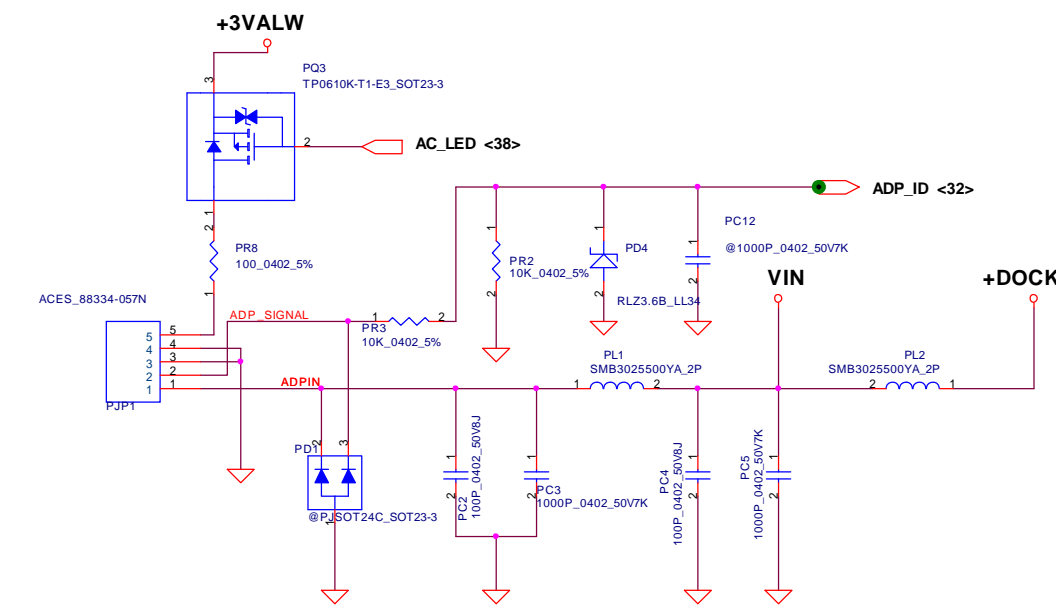


**Vendor suggests 4K PU
11/07 Follow recommend change to 3.9K**

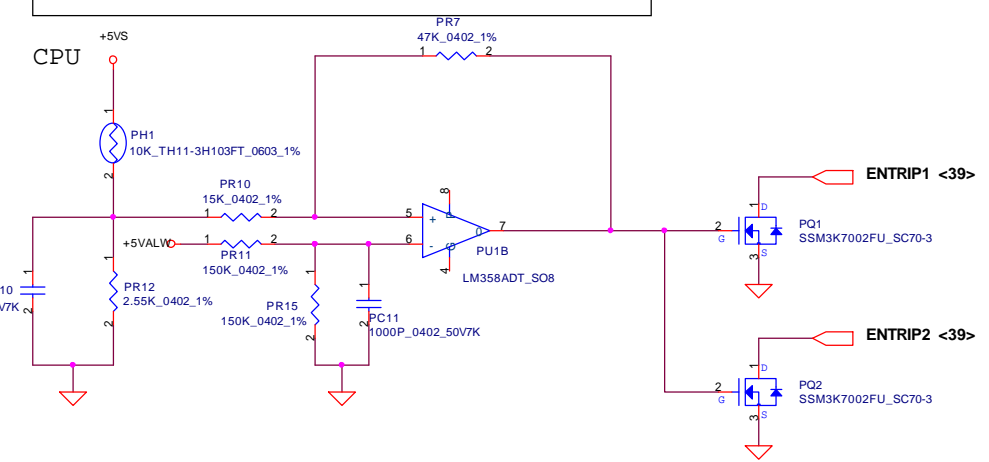
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				Sheet	35 of 46



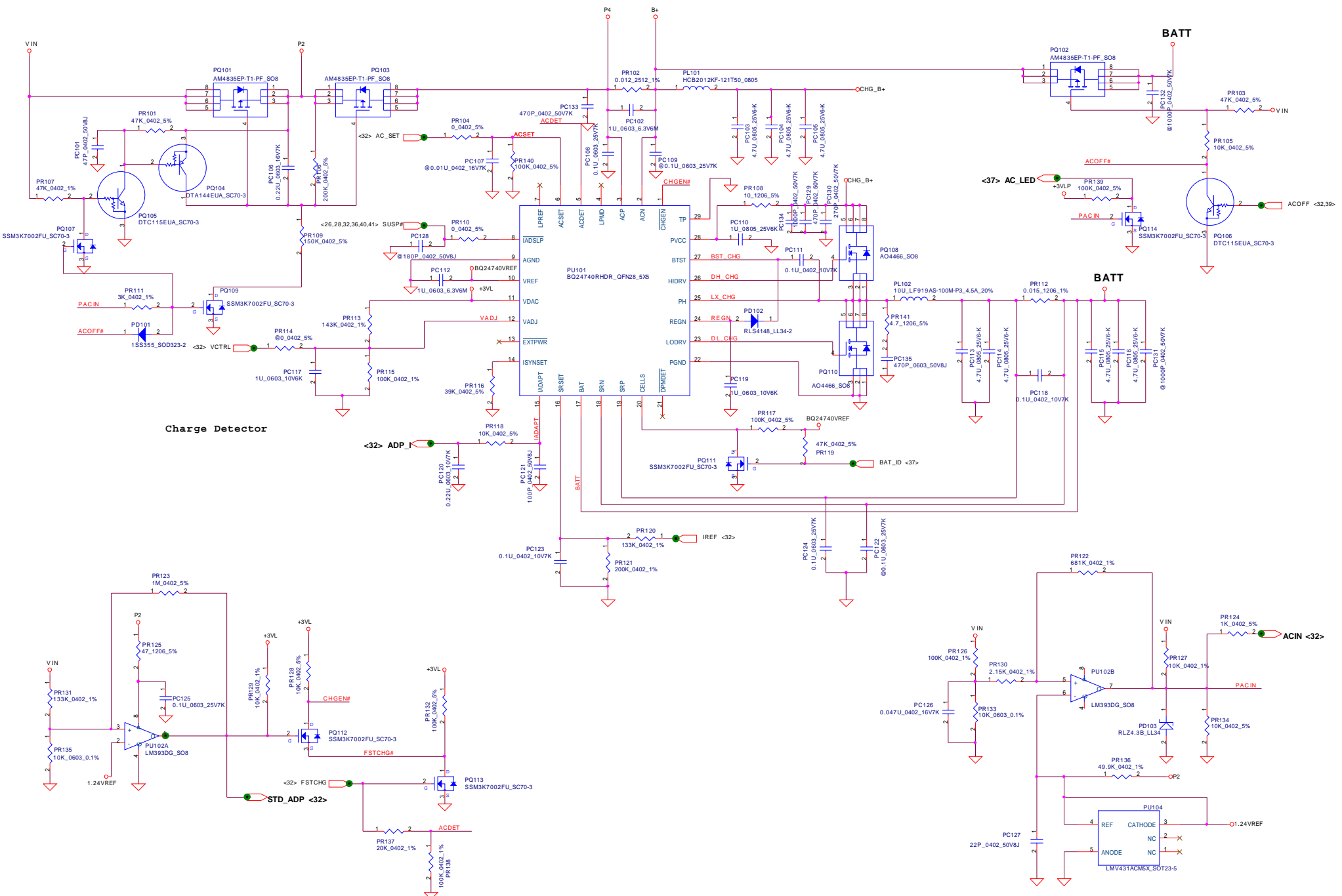
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Issued Date	2007/08/28	Deciphered Date	2006/07/26	Compal Electronics, Inc.	
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Size		Document Number		Rev	
		Montevina Blade UMA LA4101P		0.3	
Date:				Saturday, January 05, 2008	
Sheet				36 of 46	



PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 47 +/-3 degree C

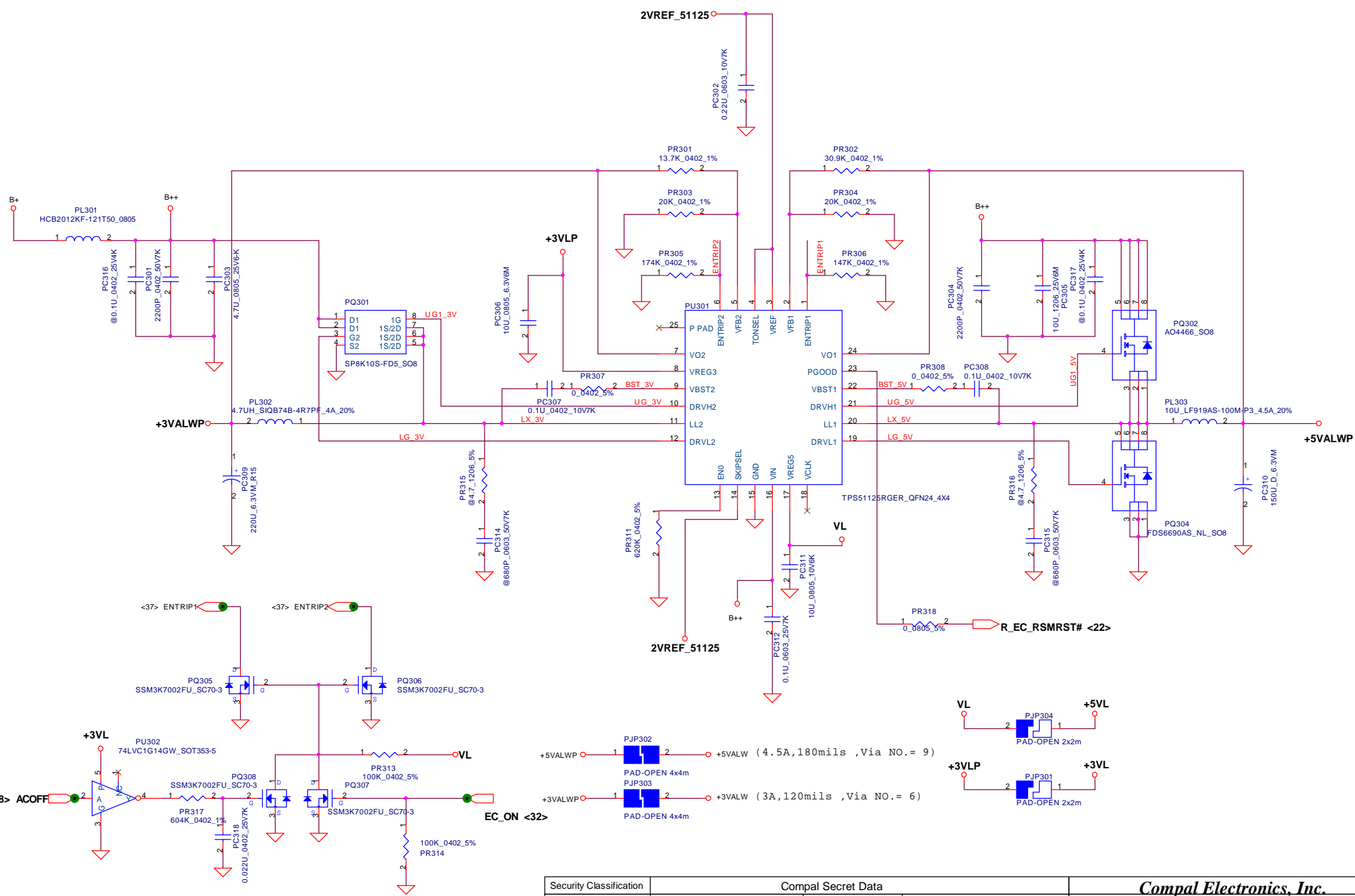


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					Rev 0.3
Date: Saturday, January 05, 2008					Sheet 37 of 46



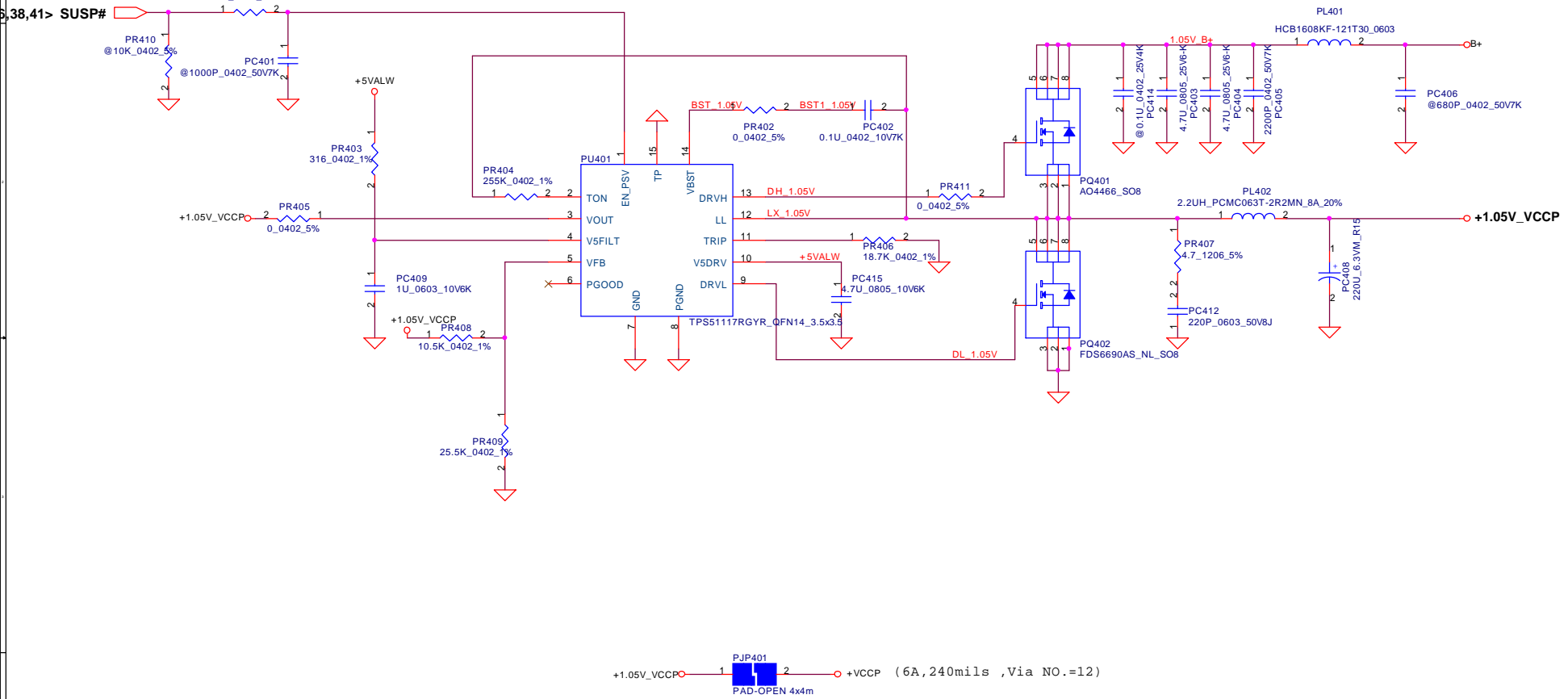
Charge Detector

Security Classification		Compal Secret Data		Title	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	Charger	
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Date:	Saturday, January 05, 2008	Sheet	38	of 46	

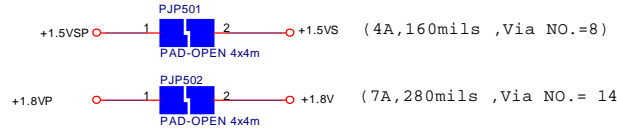
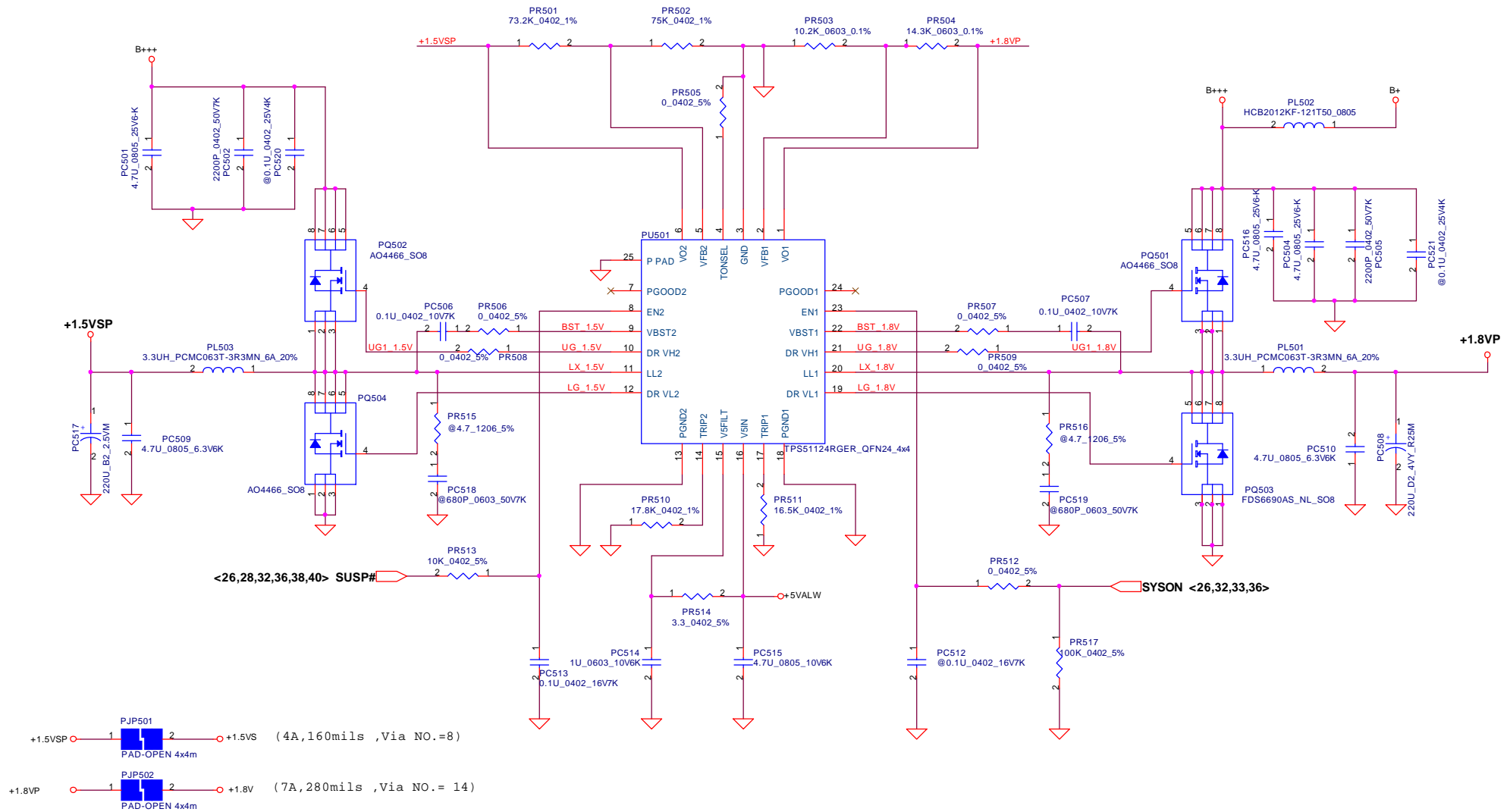


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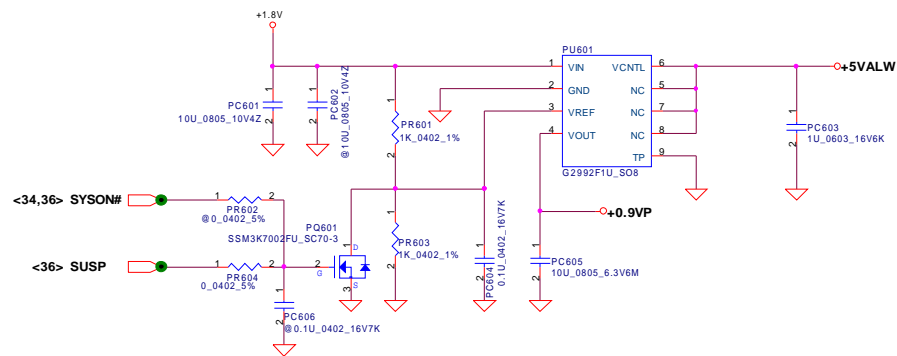
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Size			3.3VALWP/5VALWP	
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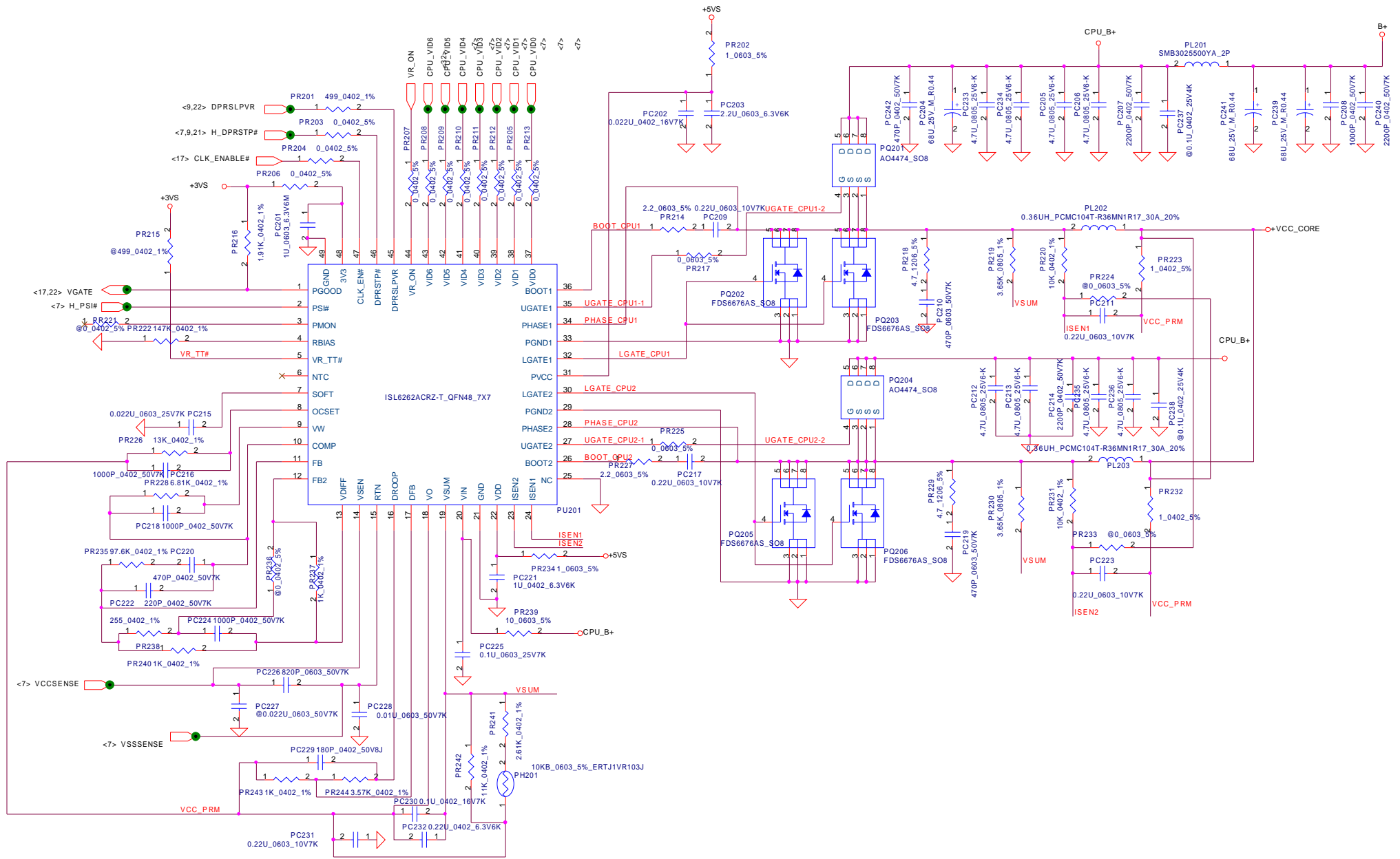
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Title: +CPU_CORE			
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41、C42、C43、C44 Change ESR=7m ohm	11/21	SI-1
2	Disable TV out function from Docking	11、34	R61、R62、R63 change to 75 Ohm、TV_DCONSEL_0、TV_DCONSEL_1 connect to GND	11/07	SI-1
3	Update Connetor Library		CRT(JCRT1)、HDMI(JHDMI1)、ESATA(JP53)、Finger print(JJP24)、FAN(JP2)、Speaker(JP60)、Multi bay(JP12)、Dual LED(D53、D12)	11/17	SI-1
4	Delete LVDS B channel	11、19	Schematic Delete	11/17	SI-1
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K、R1093=100K	11/07	SI-1
6	Reserve Card reader D3E function	22、27	GPIO6= CR_CPPE#、GPIO22=CR_WAKE#	11/17	SI-1
7	Swap PCIE LAN and New card	22	Swap PCIE4 and PICE6	11/17	SI-1
8	Add HDCP ROM for ICH9M	22、31	Add HDCP ROM for ICH9M	11/17	SI-1
9	Change G sensor control from SB、LED drive by +5VS	22、33	Change G sensor control from SB	11/17	SI-1
10	Avoid Battery mode can't boot issue	22、39	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	SI-1
11	Add G sensor ST and Bosch	24	Add G sensor ST and Bosch	11/17	SI-1
12	Change LAN solution (Marvell to Realtek)	25	Change LAN solution (Marvell to Realtek)	11/17	SI-1
13	LAN can't work	25	U46 Change to correct transformer type	11/17	SI-1
14	Cardreader schematic review and update, add D3E function	27	R709-->10K、R402-->8.2K、R704-->Stuff、R705-->@、U37-->@、Cardreader LED-->+5VS、add D3E function	11/17	SI-1
15	Jack can't detect normal	28	R1059 change from 39.2 to 39.2K	11/17	SI-1
16	Speaker work un normal	28	Add and Stuff C1362、R1065、R596	11/17	SI-1
17	HP audio team recommend	28、29	C285-C292、C1352、C1354 change to 0.022U、Amp output setup to 15.6 dB、Reserve C305、C306 for GNDA and GND	11/17	SI-1
18	Audio jack can't detect normal	29	Add Pull up resistor R401 to +3VALW	11/17	SI-1
19	Docking HP audio test fail	29	Add C295、BC296 to avoid DC level, and add R409、R410 to reduce HP out level	11/17	SI-1
20	Leakage problem	32	Correct direction prectect leakage	11/07	SI-1
21	EC pin define update	32	Delete EC_PME#、SYSON PU、SUSP# PU、LID_SW# change to +3VALW、Delete CLKRUN#、R582->@ for C0 chip、CIR PU+5VL、add 100P to BATT_OVP(EC recommend)	11/07	SI-1
22	Can't Hibernation(SLP_S4#)	32	Connect SLP_S4# to SB	11/17	SI-1
23	EC can't receive docking present	34	CONA# change +3VL	11/12	SI-1
24	HDMI can't detect	35	DDC_EN must enable、TMDS_B_HPDP# inverse	11/07	SI-1
25	LVDS power on timing	19	C238 change to 0.047u to meet TI timing	01/03	SI-2
26	Prevent WWAN nosie	21	Add 12p on HDA_SDOOUT and HDA_SDOOUT	01/03	SI-2
27	Power leakage	21、31	Change HDCP ROM to +3VS power plane	01/03	SI-2
28	Prevent WLAN leakage	26	Add Diode prevent WLAN leakage	01/03	SI-2

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	New card PTH connector GND	26	New card PTH connector GND	01/03	SI-2
30	Change Cardreader LED control	27	Change Cardreader LED control	01/03	SI-2
31	Change SPDIF to SPDIF1	28	Change to SPDIF1	01/03	SI-2
32	Shut down pop noise	29	Change C293 to 1U	01/03	SI-2
33	Change BT power to +3VS	30	Change BT power to +3VS	01/03	SI-2
34	EMI Request	31	SPI_FSEL#、SPI_CLK_R、SPI_FWR# reserver RC	01/03	SI-2
35	Reserver 0 ohm co lay with common choke	35	Reserver 0 ohm co lay with common choke	01/03	SI-2
36	Sparate+5VS and +3VS power timing	36	Sparate+5VS and +3VS power timing	01/03	SI-2
37	Keyboard backlight reserve a 0805 size resistor	33	Keyboard backlight reserve a 0805 size resistor	01/03	SI-2
38	Change Lid switch connector type	33	Change Lid switch connector type	01/03	SI-2
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Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	39	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301 cancel PQ303	
3	38	Charger	11/06	Compal	EMI solution	Add pc128	
4	43	+CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	39	3.3VALWP/5VALWP	11/14	Compal	for Layout	Change PL303 and PC310	
6	38	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
7	43	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
8	39	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
9							
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11							
12							
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14							

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