

Compal confidential

Low Cost Los Angeles 10AL+

NBWAE LA-5831P Schematics Document

Mobile AMD S1G2

RS780MN & RS780MC / SB700

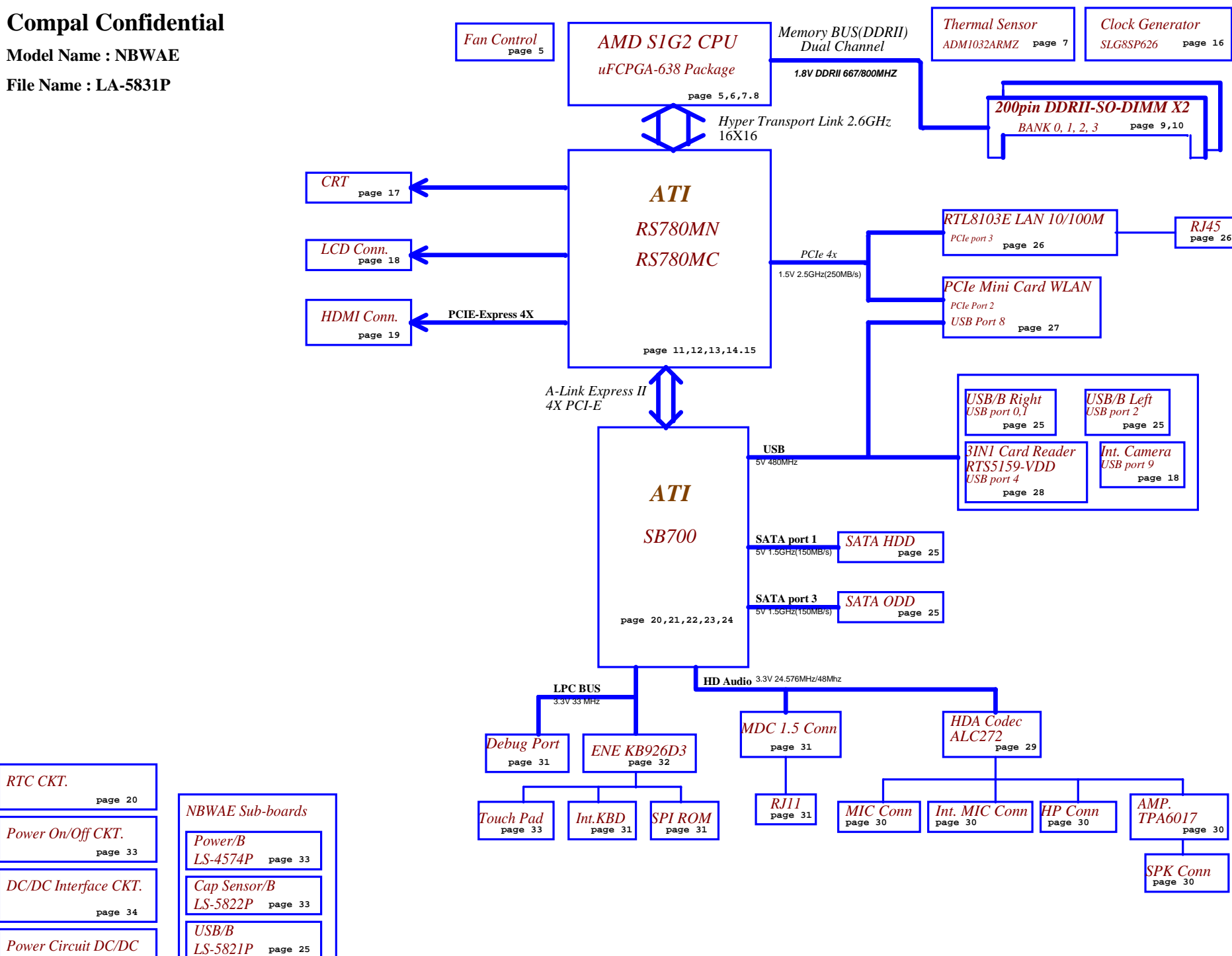
2009-08-12 Rev. 1.0

Security Classification	Compal Secret Data			Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Compal Electronics, Inc. Cover Sheet	
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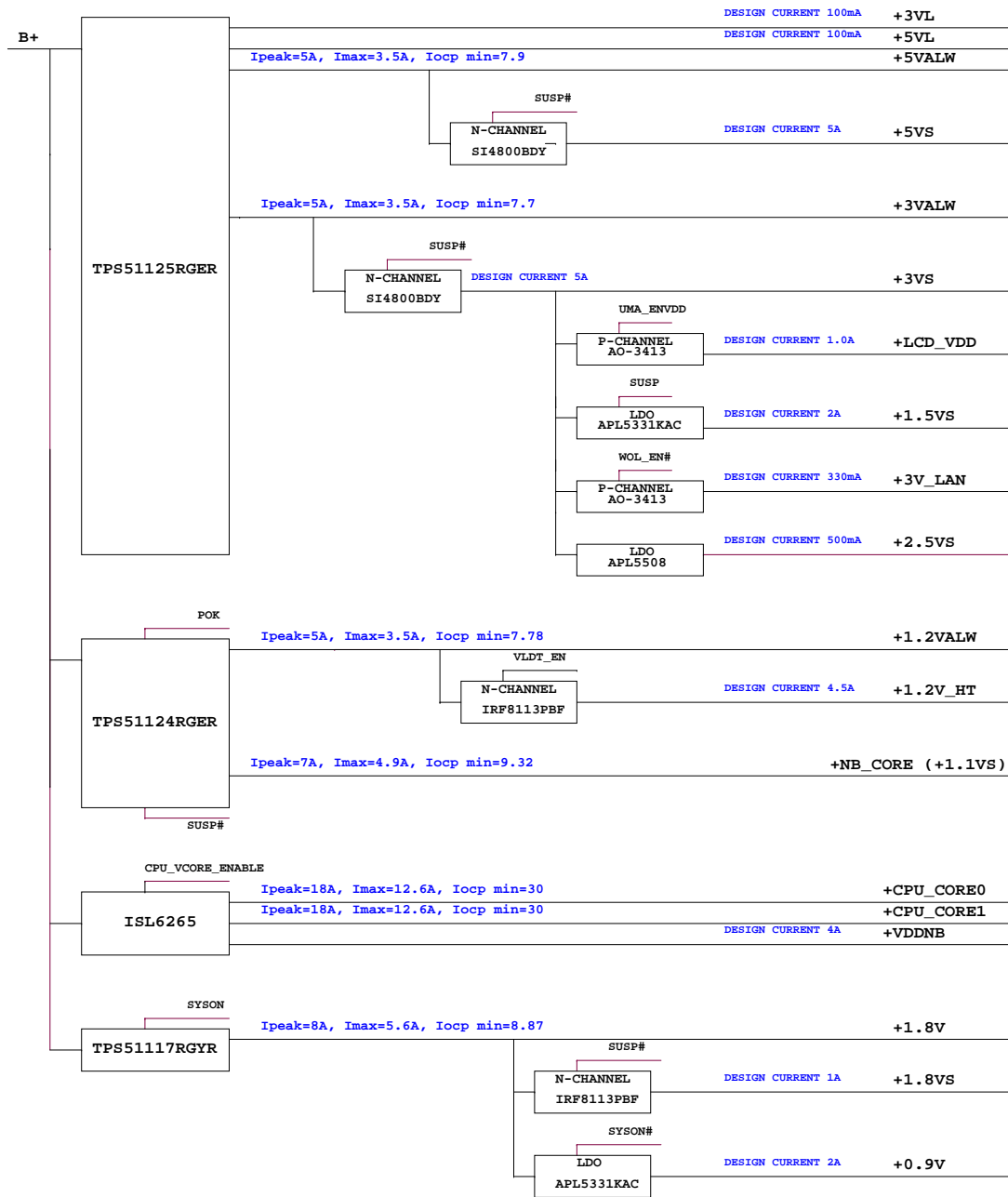
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Model Name : NBWAE

File Name : LA-5831P



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Voltage Rails

O : ON
X : OFF

State	B+ +3VL +5VL +RTCVC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.2V_HT +VDDNB +CPU_CORE_0 +CPU_CORE_1
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Platform	CPU	NB	SB
PUMA@	S1G2	RS780MC	SB700
	S1G2	RS780MN	SB700
TIGRIS@	S1G3	RS880MC	SB710
	S1G3	RS880M	SB710

@ : just reserve , no build

BTO (Build-To-Order) Option Table

Function	Modem	HDMI	CAMERA & MIC	
Description	(R)	(Y)	(X)	
Explain			CAMERA	MIC
BTO	MDC@	HDMI@	CAM@	MIC@

SBUS Control Table

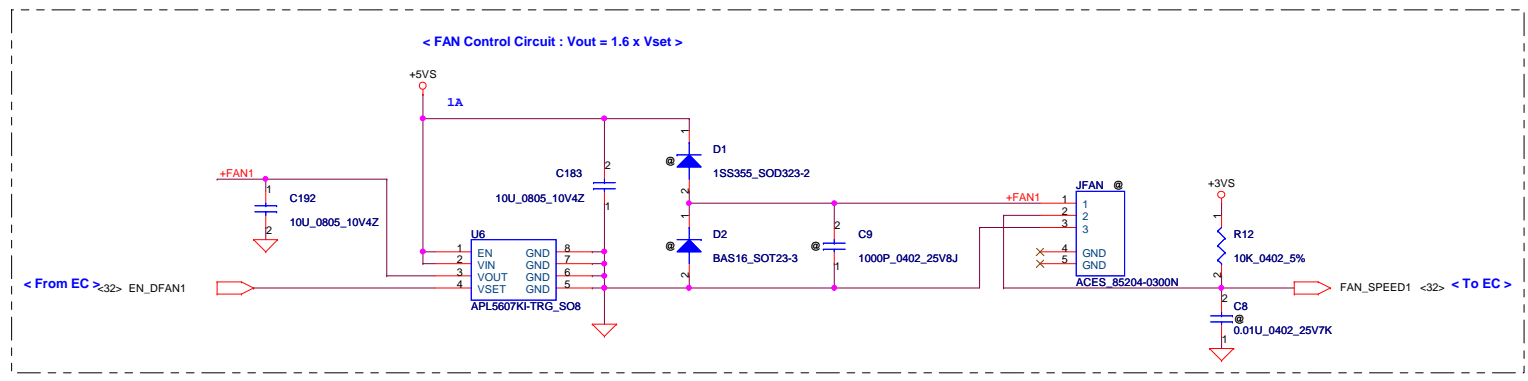
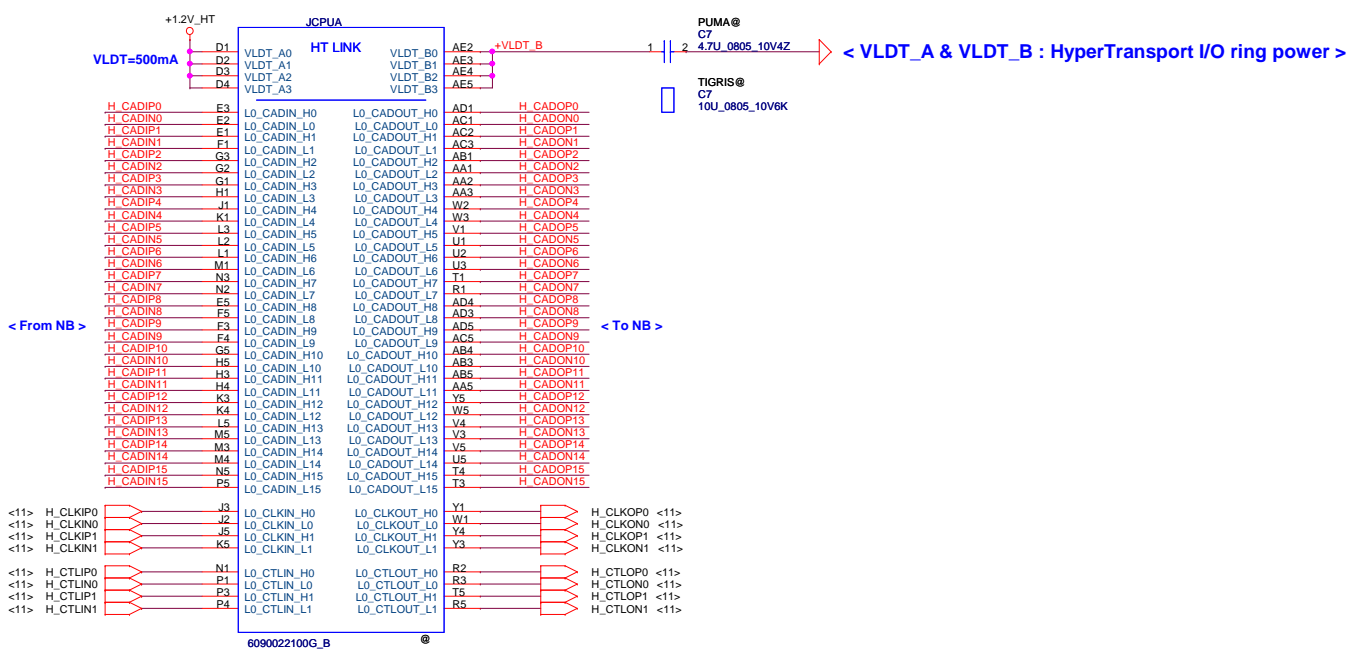
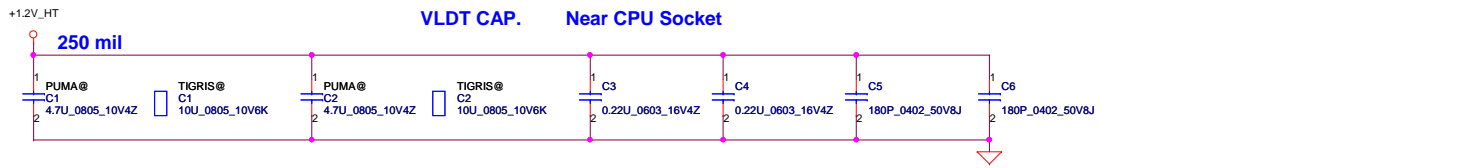
	SOURCE	INVERTER	BATT	HDMI CEC	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	NEW CARD
EC_SMB_CK1 EC_SMB_DA1	KB926		V								
EC_SMB_CK2 EC_SMB_DA2	KB926				V						
I2C_CLK I2C_DATA	RS780MN RS780MC								V		
DDC_CLK0 DDC_DATA0	RS780MN RS780MC									V	
DDC_CLK1 DDC_DATA1	RS780MN RS780MC										
SCL0 SDA0	SB700					V	V				
SCL1 SDA1	SB700							V			
SCL2 SDA2	SB700										
SCL3 SDA3	SB700										

SB700 SM Bus0 Address				SB700 SM Bus1 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b	+3VALW	WLAN/WIMAX		
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b				
+3VS	Clock Generator	D2 H	1101 0010 b				

KB926 SM Bus1 Address				KB926 SM Bus2 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011X b	+3VS	CPU_ADM1032-1	98 H	1001 100X b

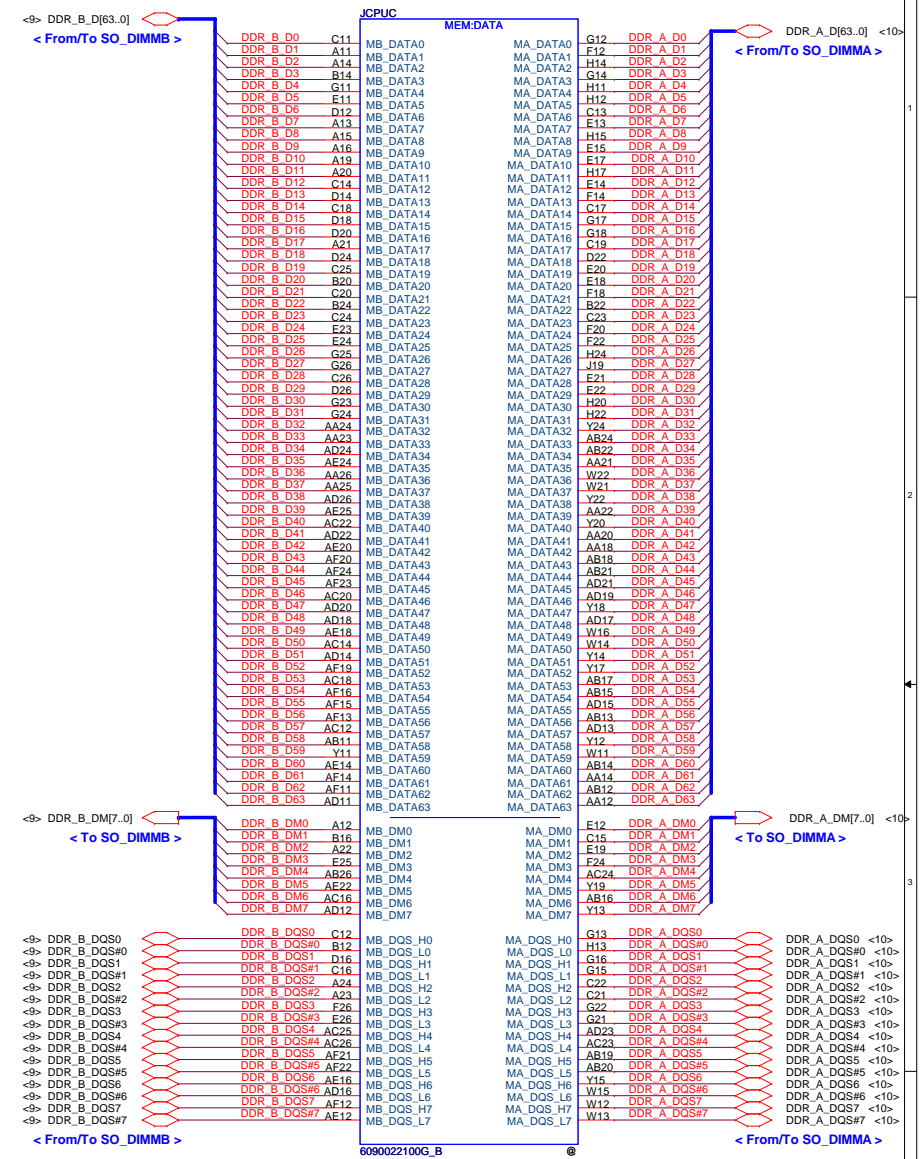
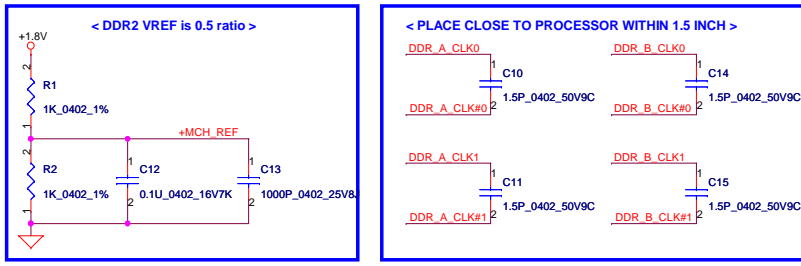
KB926 ESB Address			
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

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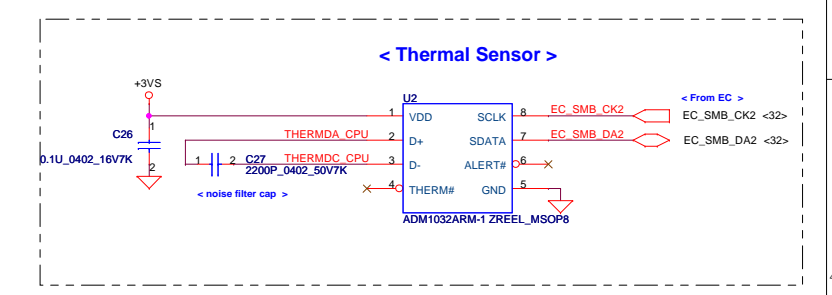
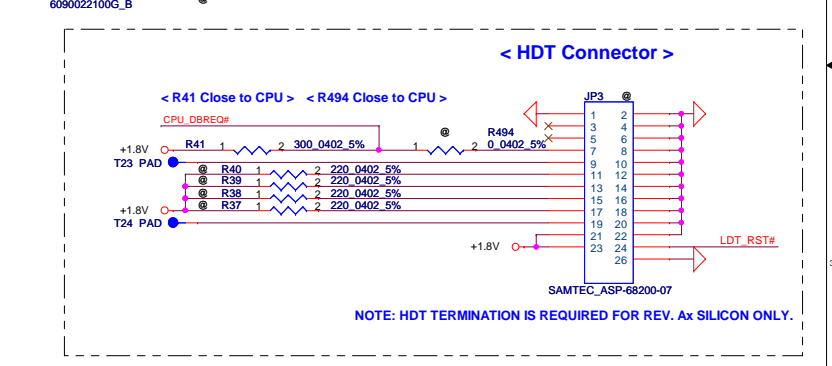
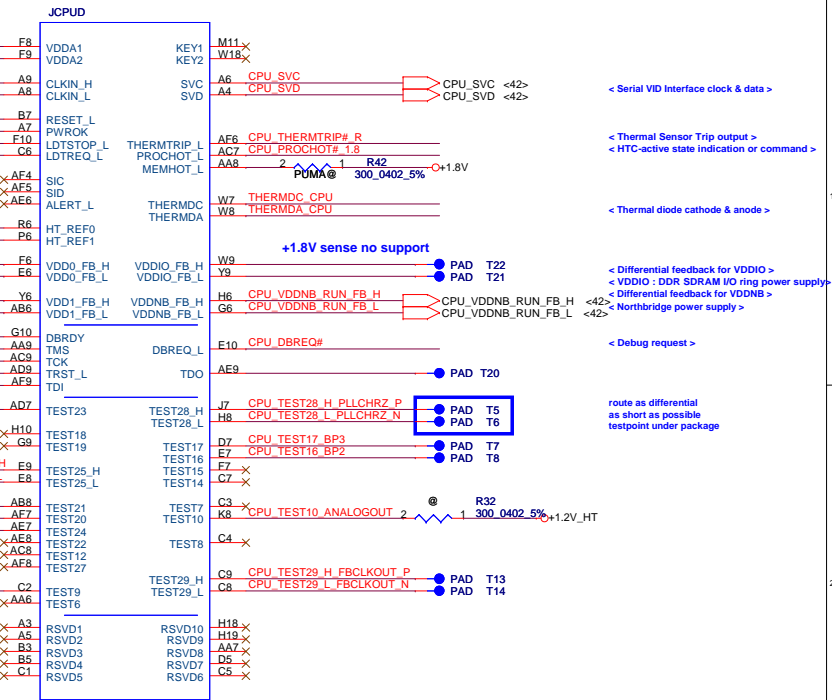
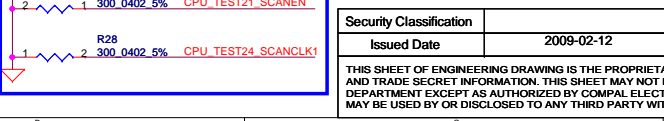
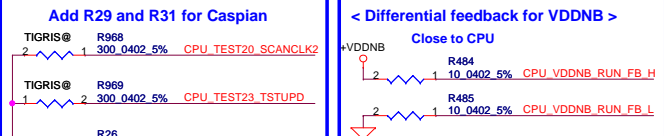
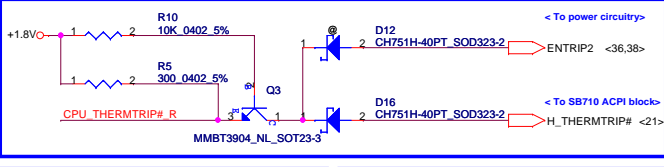
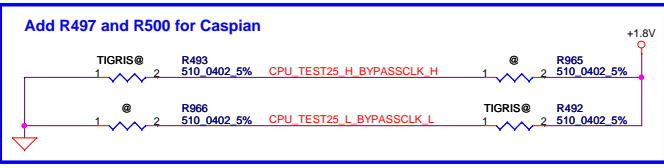
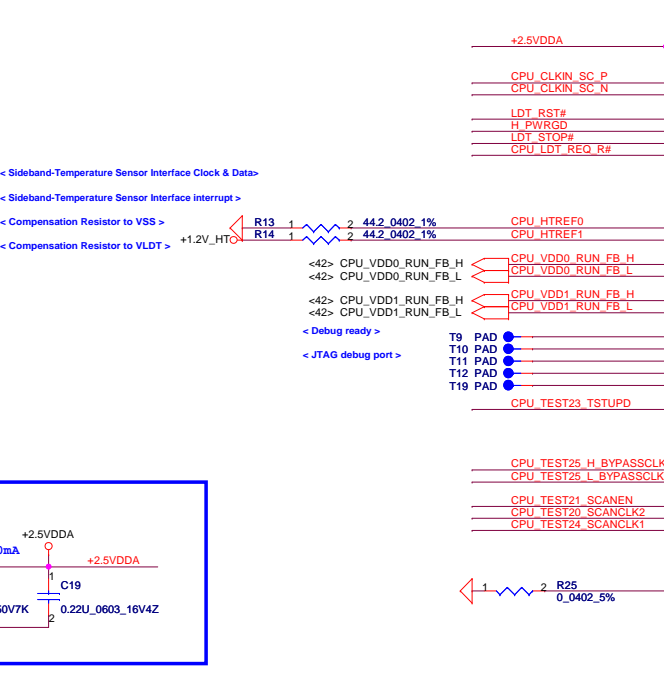
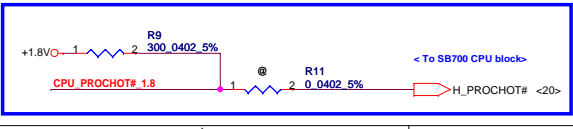
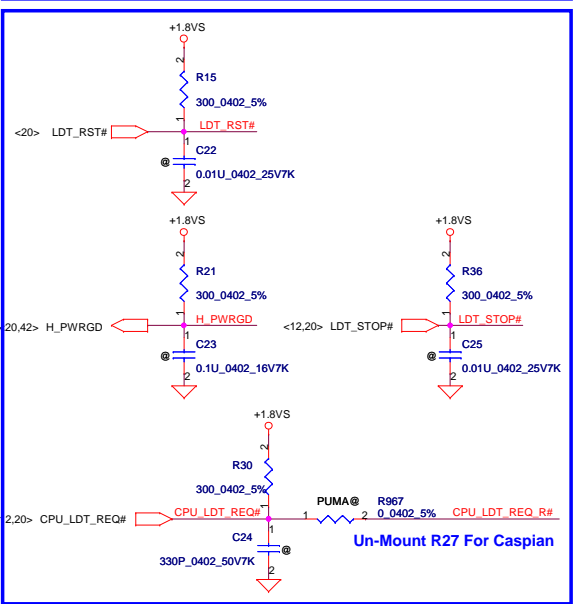
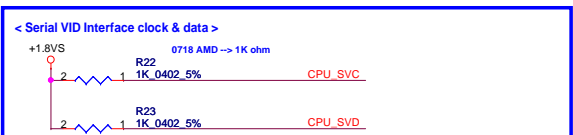
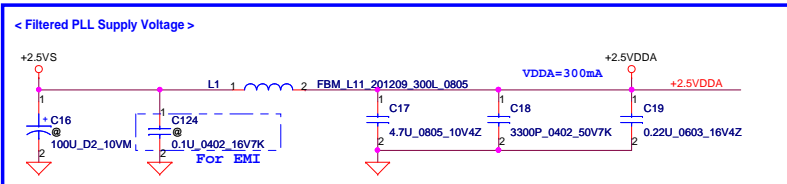
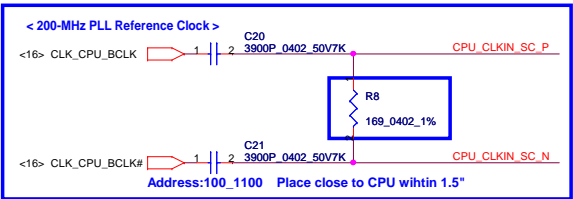
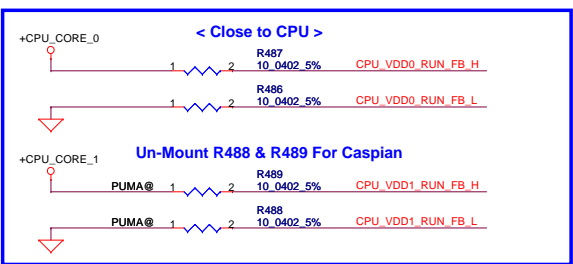


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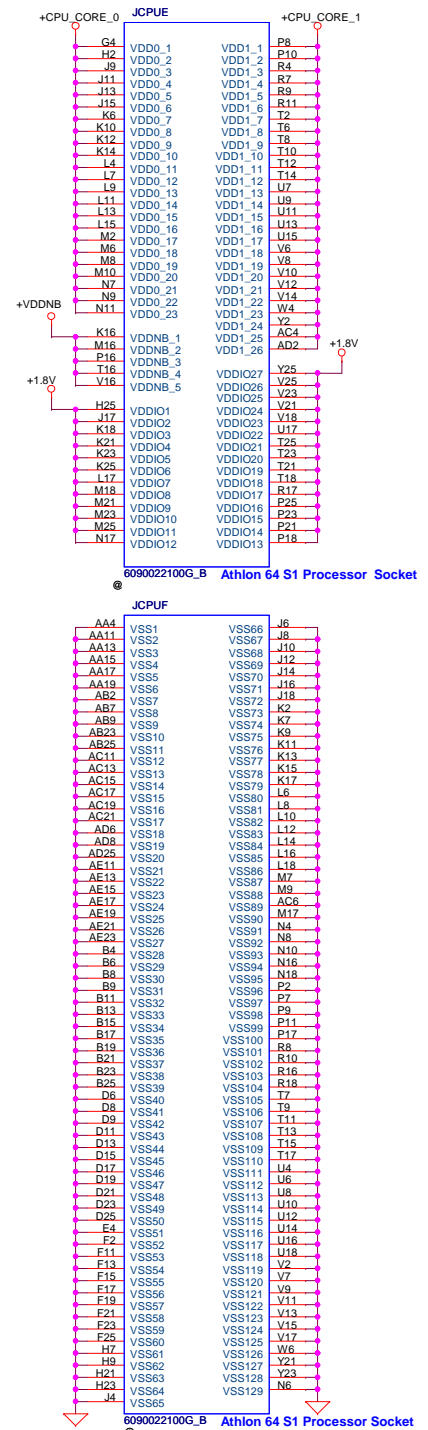
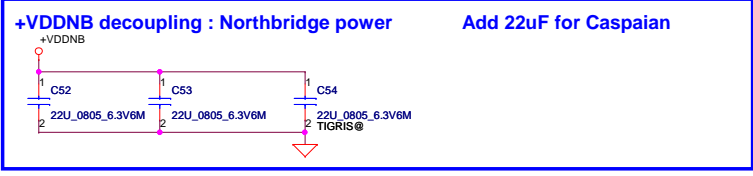
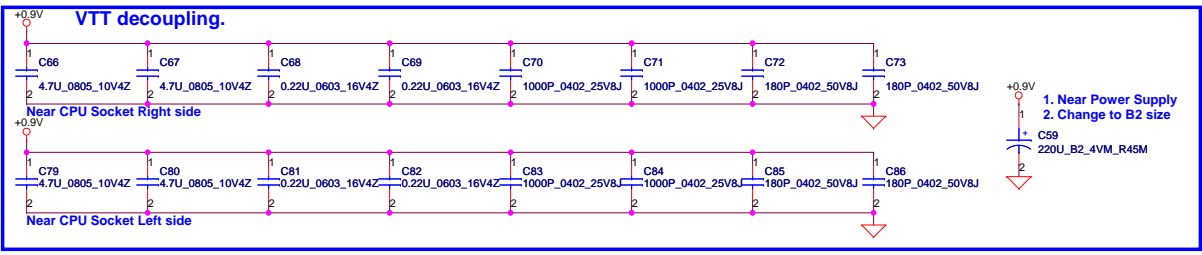
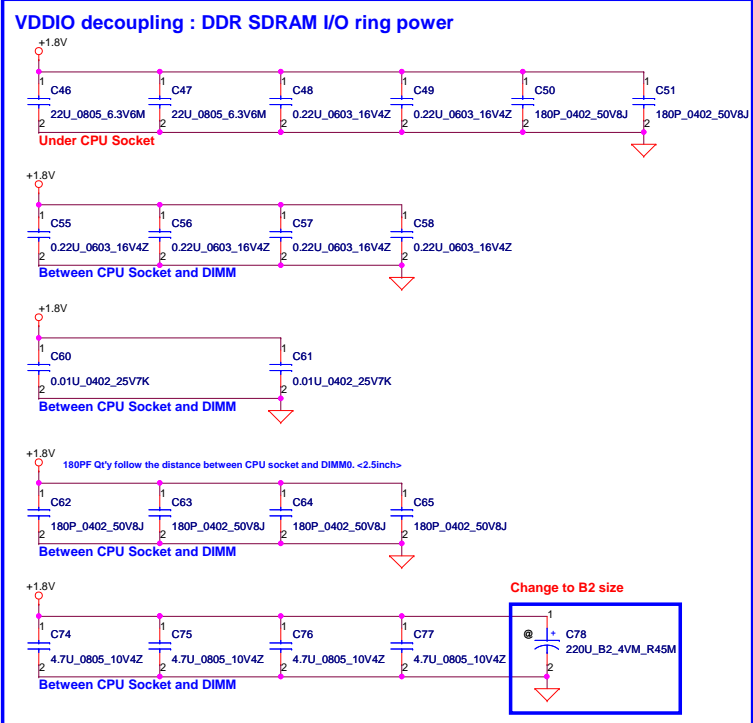
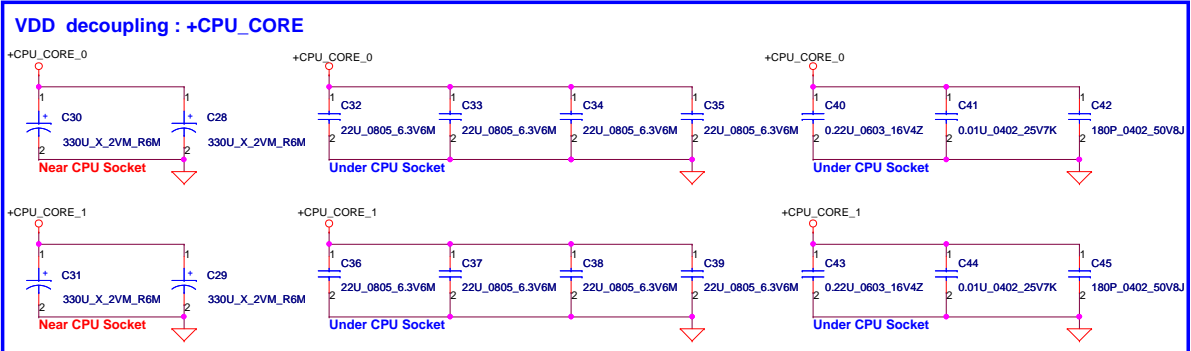
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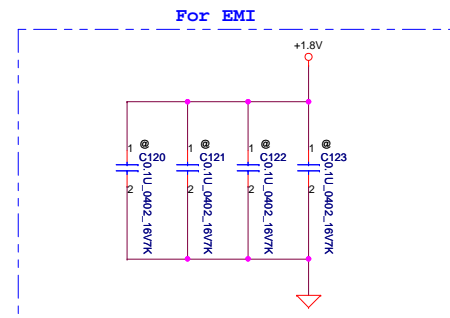
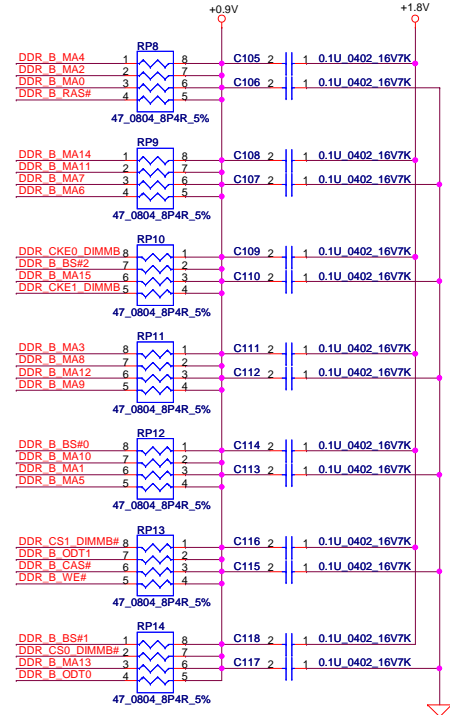
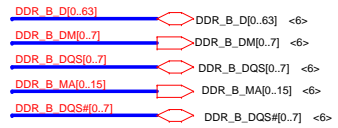
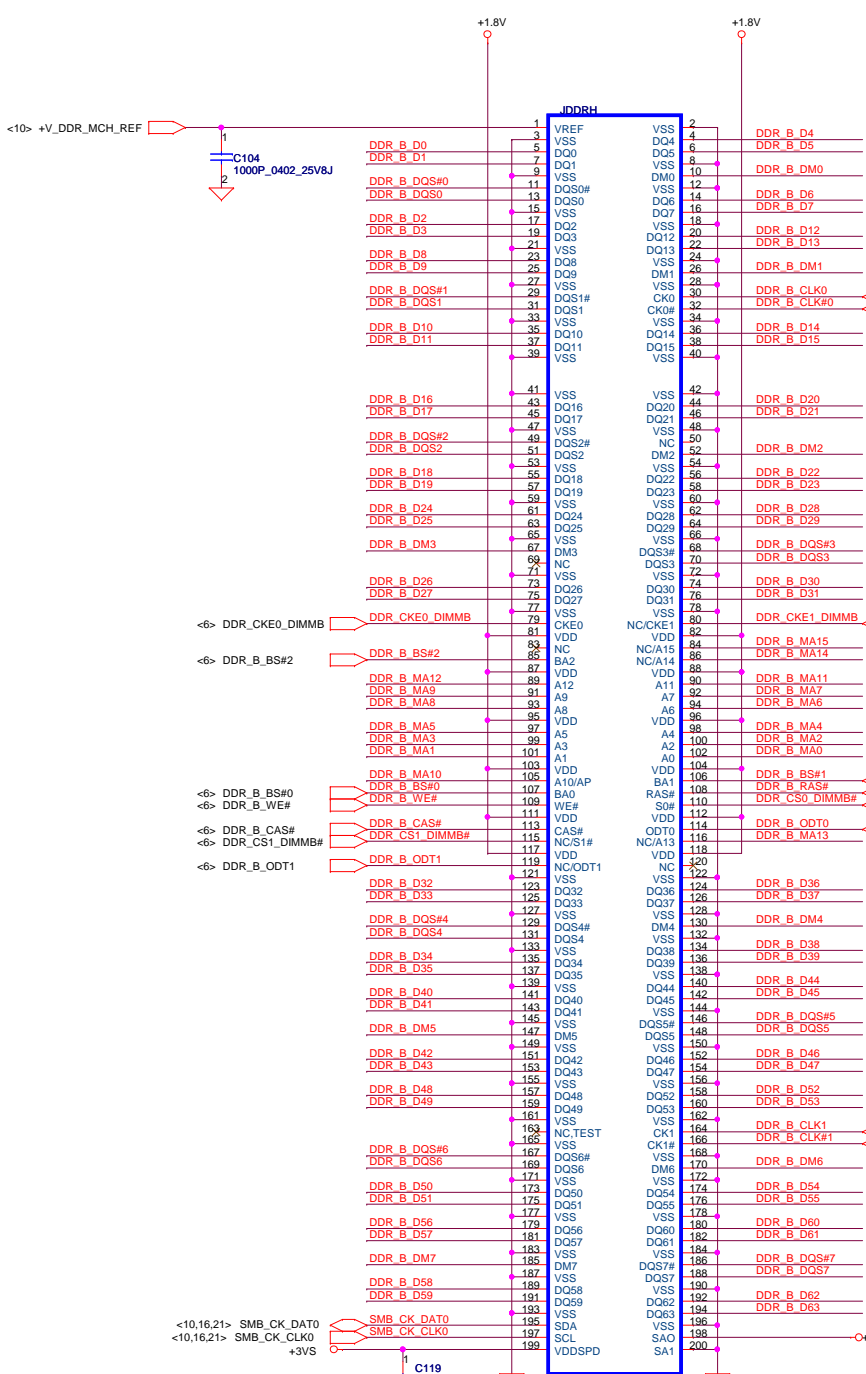
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AMD CPU SIG3 DDR2 I/F				Document Number
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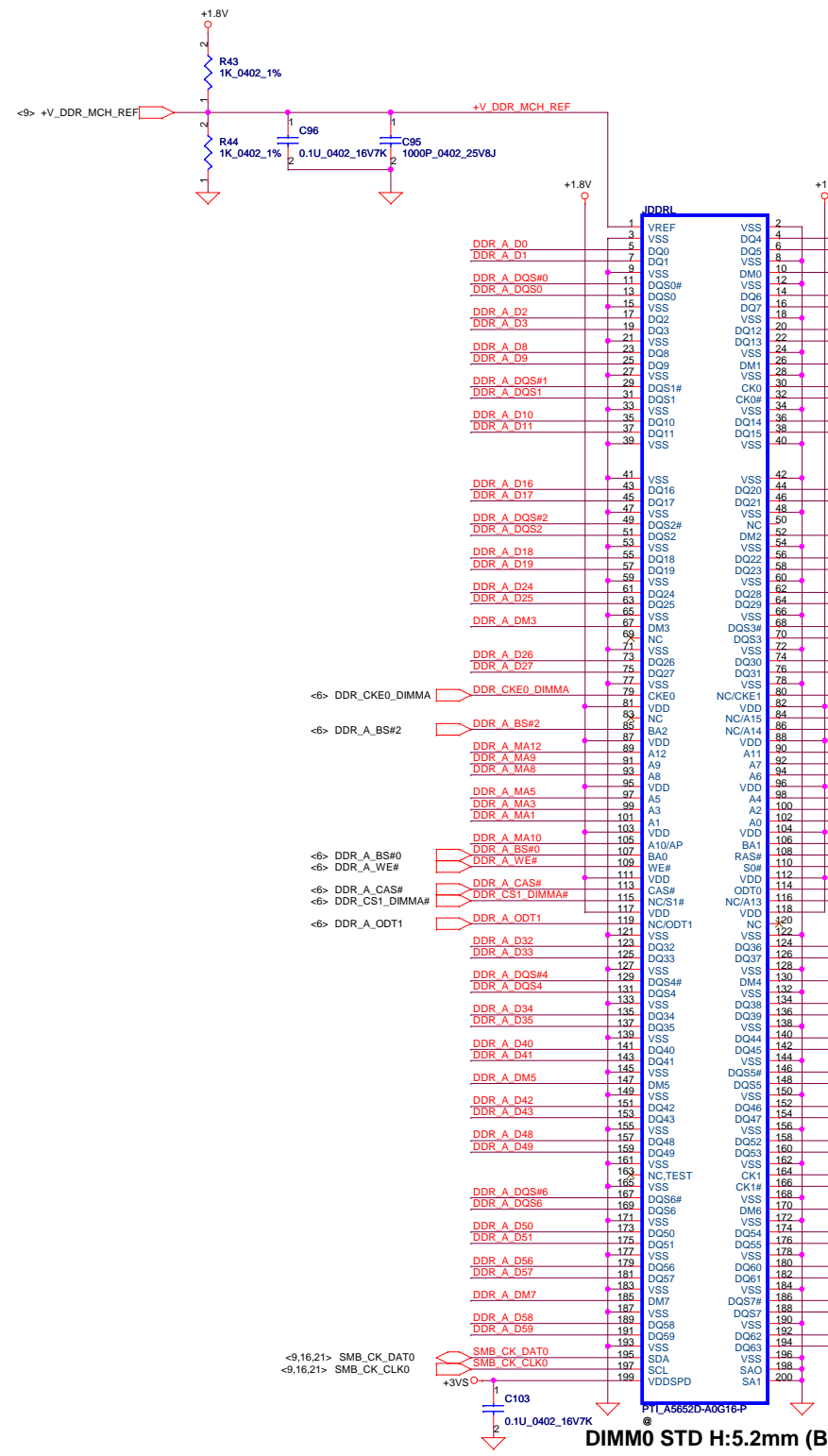


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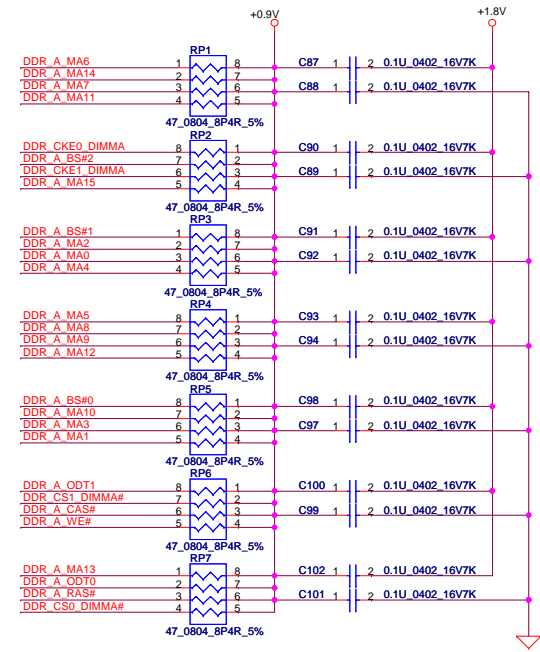


DIMM0 STD H:9.2mm (Bot)

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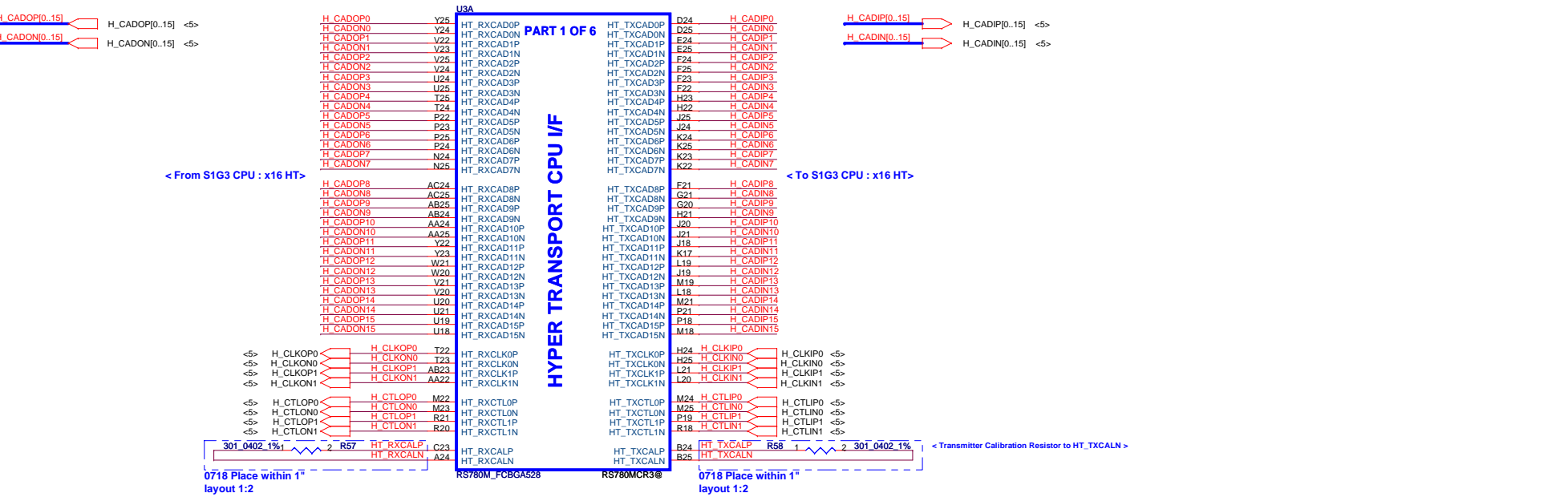
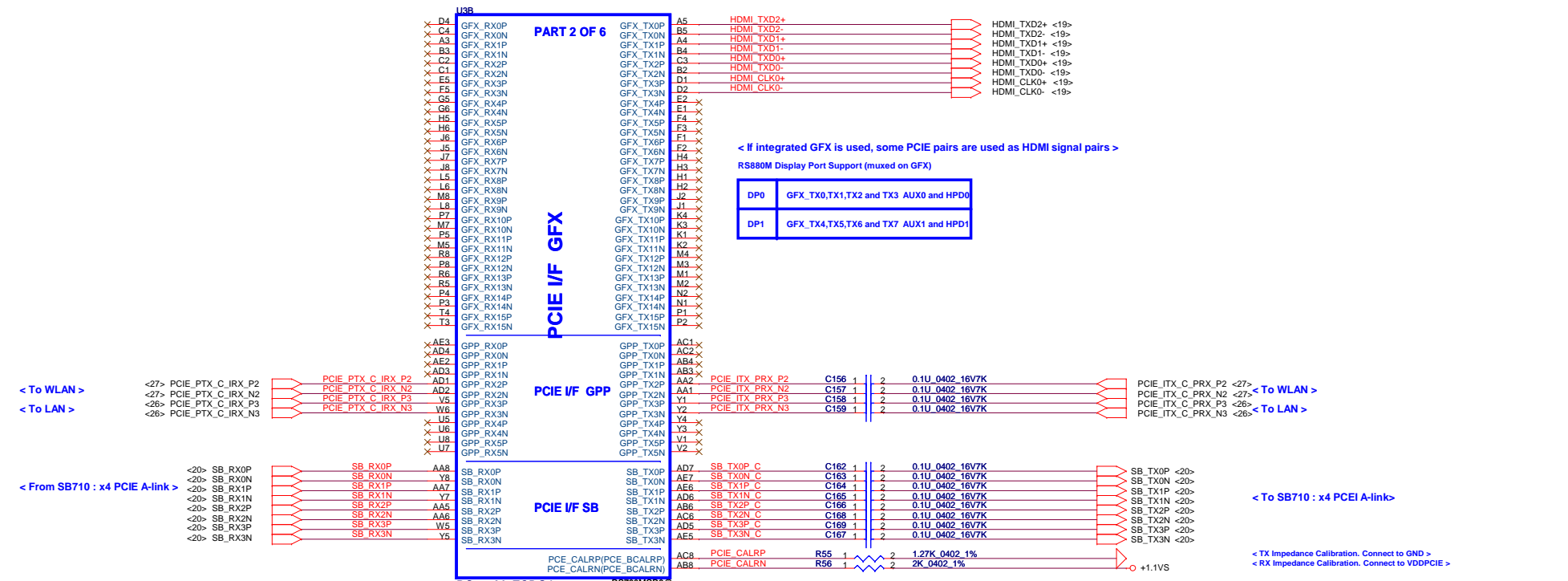
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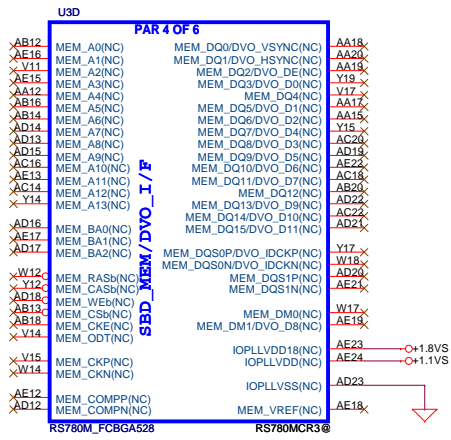


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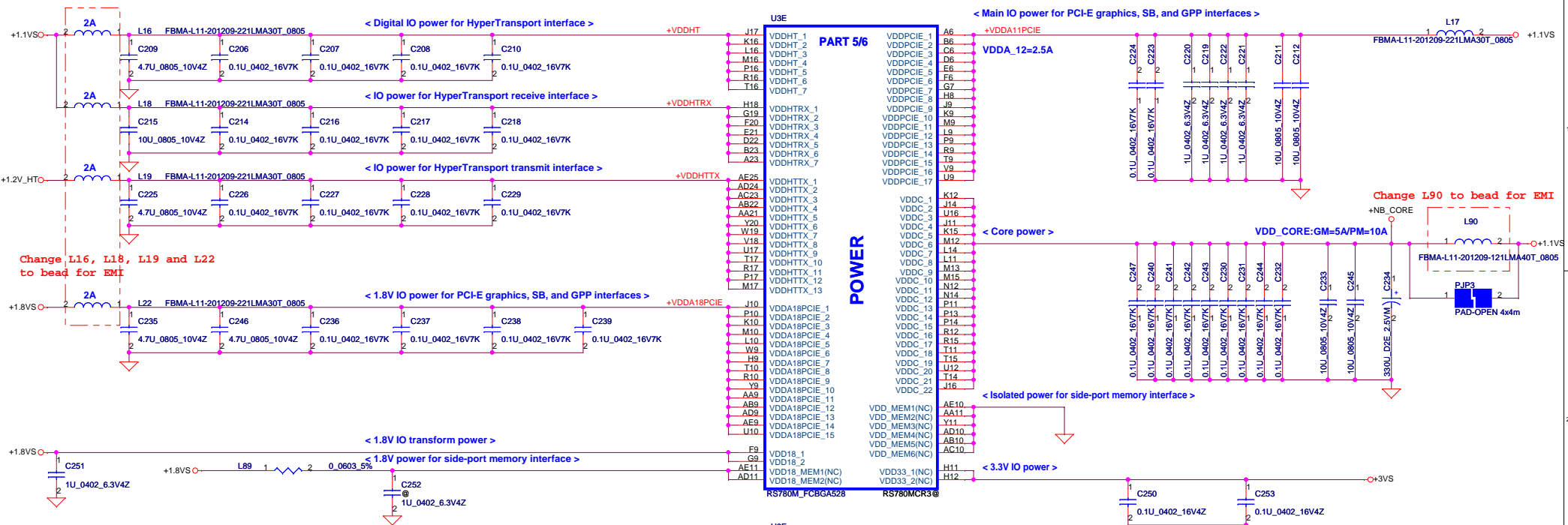
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DDR II SO-DIMM 1			
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DIMM0 STD H:5.2mm (Bot)





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U3E PART 5/6

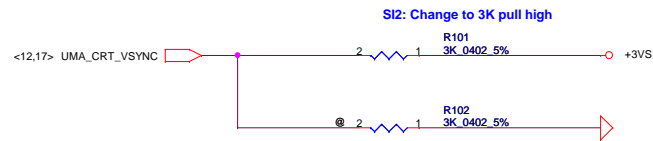
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VDDHT_96	VDDPCIE_96
VDDHT_97	VDDPCIE_97
VDDHT_98	VDDPCIE_98
VDDHT_99	VDDPCIE_99
VDDHT_100	VDDPCIE_100

U3F PART 6/6

VSSAHT1	VSSAPCIE1	A2
VSSAHT2	VSSAPCIE2	B1
VSSAHT3	VSSAPCIE3	D3
VSSAHT4	VSSAPCIE4	D5
VSSAHT5	VSSAPCIE5	E4
VSSAHT6	VSSAPCIE6	G1
VSSAHT7	VSSAPCIE7	G2
VSSAHT8	VSSAPCIE8	G4
VSSAHT9	VSSAPCIE9	H2
VSSAHT10	VSSAPCIE10	J4
VSSAHT11	VSSAPCIE11	R7
VSSAHT12	VSSAPCIE12	L1
VSSAHT13	VSSAPCIE13	L4
VSSAHT14	VSSAPCIE14	L2
VSSAHT15	VSSAPCIE15	L7
VSSAHT16	VSSAPCIE16	M6
VSSAHT17	VSSAPCIE17	N4
VSSAHT18	VSSAPCIE18	P6
VSSAHT19	VSSAPCIE19	R1
VSSAHT20	VSSAPCIE20	R2
VSSAHT21	VSSAPCIE21	R4
VSSAHT22	VSSAPCIE22	V7
VSSAHT23	VSSAPCIE23	U4
VSSAHT24	VSSAPCIE24	V8
VSSAHT25	VSSAPCIE25	V6
VSSAHT26	VSSAPCIE26	W1
VSSAHT27	VSSAPCIE27	W2
VSSAHT28	VSSAPCIE28	W4
VSSAHT29	VSSAPCIE29	W7
VSSAHT30	VSSAPCIE30	W8
VSSAHT31	VSSAPCIE31	Y6
VSSAHT32	VSSAPCIE32	AA4
VSSAHT33	VSSAPCIE33	AB5
VSSAHT34	VSSAPCIE34	AB1
VSSAHT35	VSSAPCIE35	AB7
VSSAHT36	VSSAPCIE36	AC3
VSSAHT37	VSSAPCIE37	AC4
VSSAHT38	VSSAPCIE38	AE1
VSSAHT39	VSSAPCIE39	AE4
VSSAHT40	VSSAPCIE40	AB2
VSS1	VSS10	AE14
VSS2	VSS11	D11
VSS3	VSS12	G8
VSS4	VSS13	E14
VSS5	VSS14	E15
VSS6	VSS15	J15
VSS7	VSS16	J12
VSS8	VSS17	K14
VSS9	VSS18	M11
VSS10	VSS19	L15

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			Rev 1.0

< RS780 DFT_GPIO5 mux at CRT_VSYNC pull High to 3K >



< DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

- 1 : Enable (RX780, RS780)
- 0 : Disable (RX780, RS780)

PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#

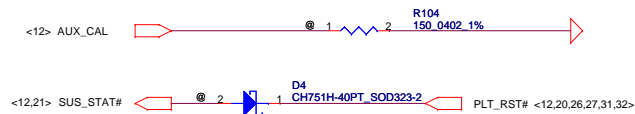
< RS780 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.

- 000 : 00001
- 001 : 00010
- 010 : 01011
- 011 : 00100
- 100 : 01010
- 101 : 01100
- 111 : 01011

< RS780 DFT_GPIO1 >



< DFT_GPIO1 : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

- 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
- 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

< RS780 use HSYNC to enable SIDE PORT (internal pull high) >



< DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb >

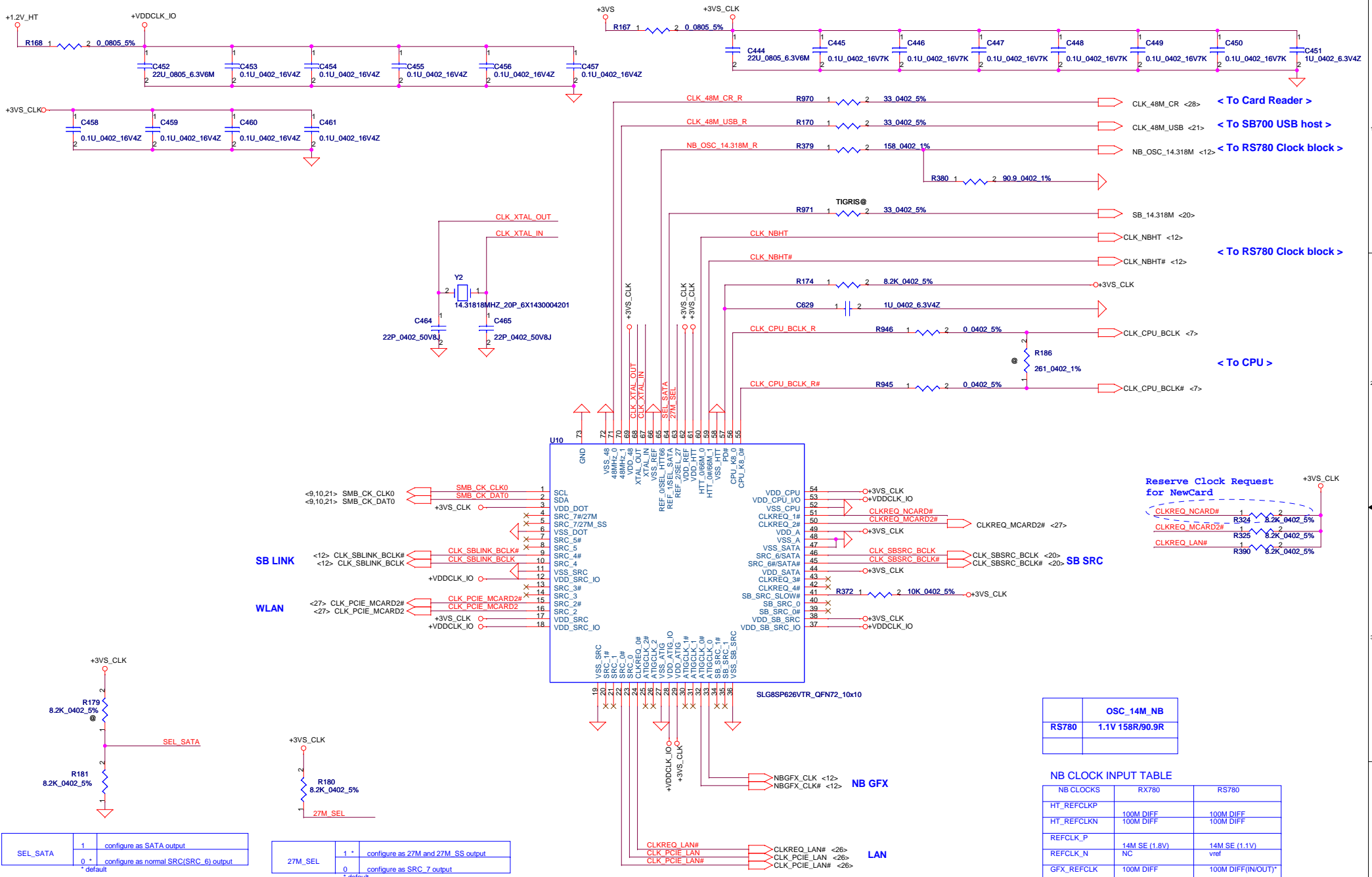
RX780: Enables the Test Debug Bus using PCIE bus

- 1 : Disable (Can still be enabled using nbcfg register access)
- 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)

- 1. Disable (RS780)
- 0 : Enable (RS780)

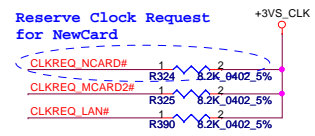
Security Classification	Compal Secret Data			Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Compal Electronics, Inc.	
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SEL_SATA	1	configure as SATA output
	0*	configure as normal SRC(SRC_6) output * default

27M_SEL	1*	configure as 27M and 27M_SS output
	0	configure as SRC_7 output * default

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output * default



	OSC_14M_NB
RS780	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

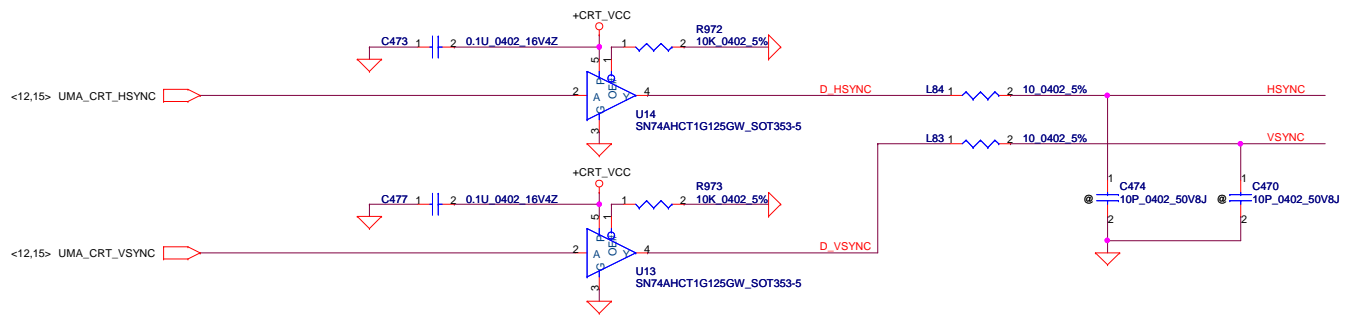
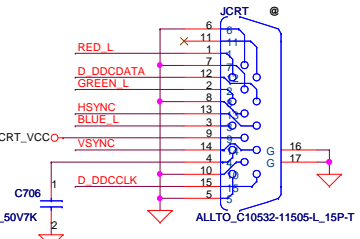
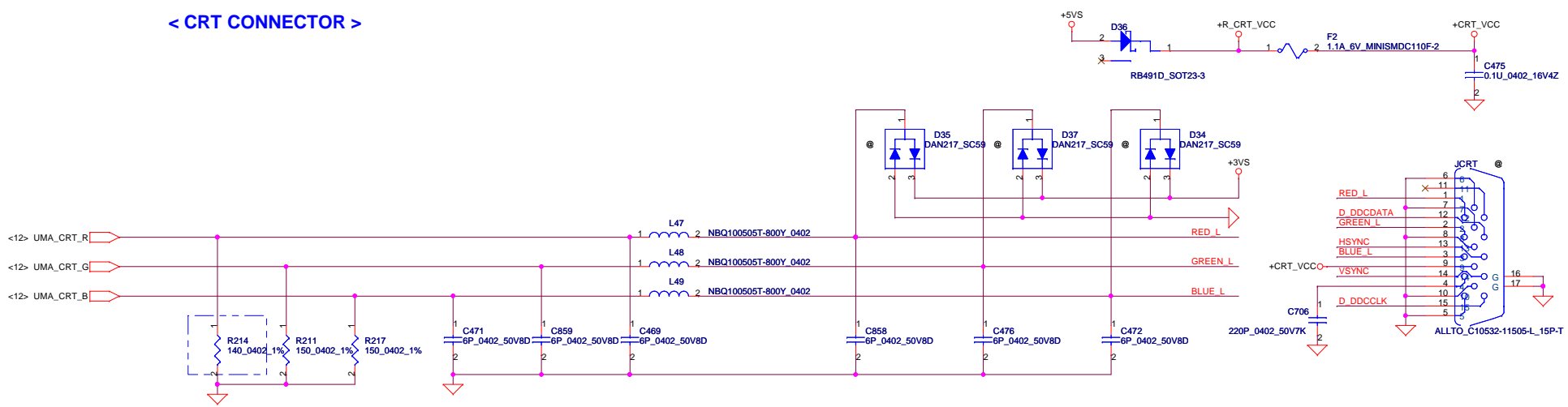
NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

Use voltage divider resistor R379 & R380 to pull low

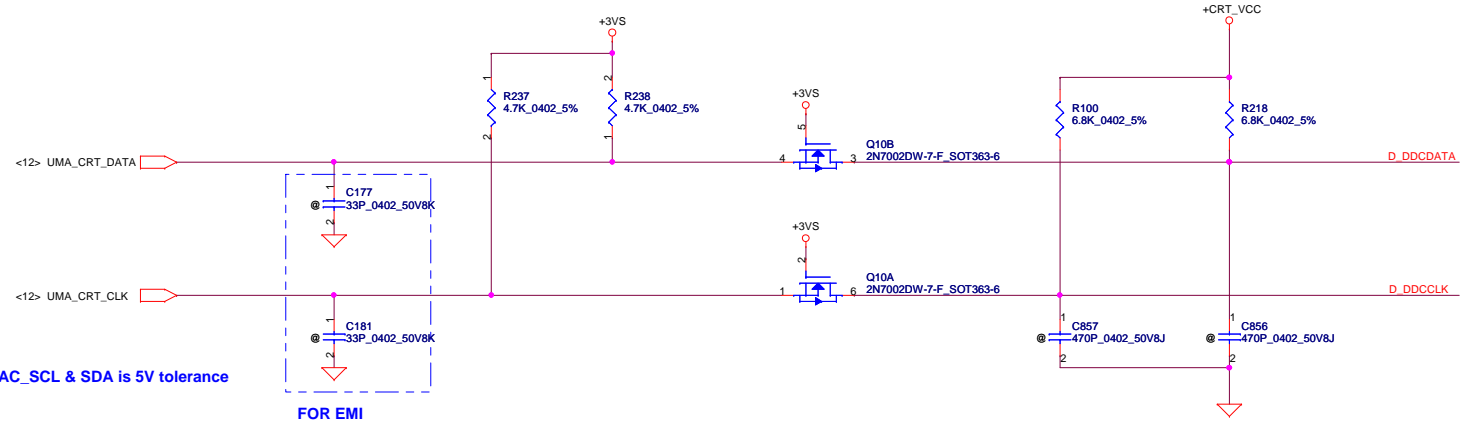
Security Classification	Compal Secret Data	
Issued Date	2009-02-12	Deciphered Date 2009-02-12
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Compal Electronics, Inc.		Clock Generator	
Title	Document Number	Rev	1.0
	LA-5831P	Date:	Wednesday, August 12, 2009
	Sheet	16	of 44

< CRT CONNECTOR >



< SYNC SIGNAL >



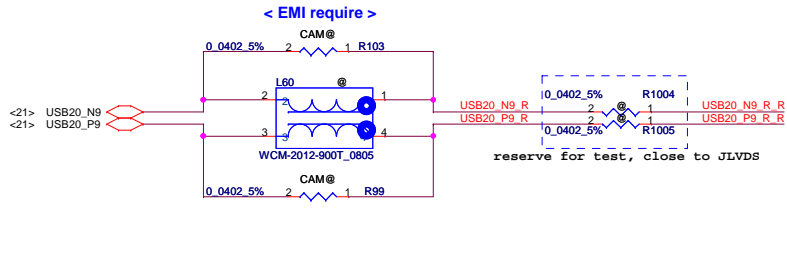
< Display Data Channel >

RS780 DAC_SCL & SDA is 5V tolerance

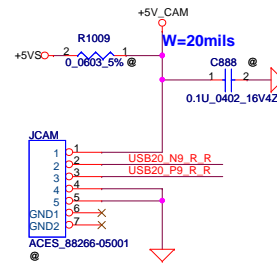
FOR EMI

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				Rev 1.0
				Sheet 17 of 44

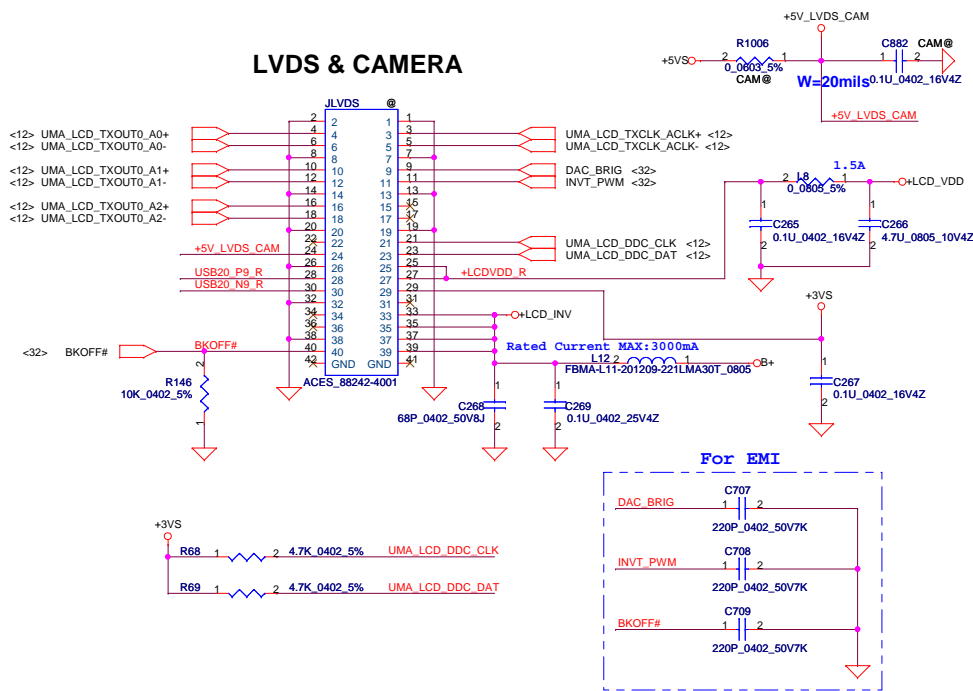
< Int. Camera, USB port 9 >



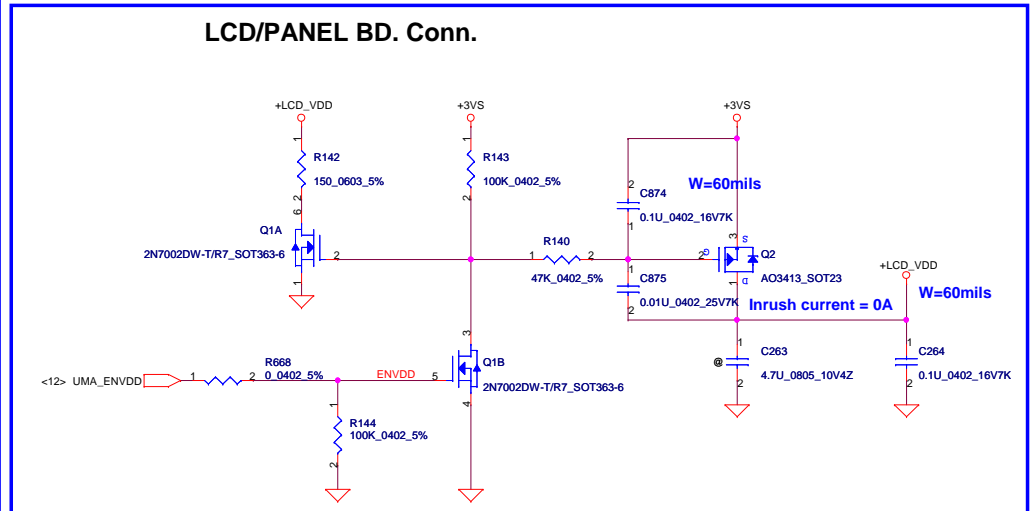
Int. Camera



LVDS & CAMERA

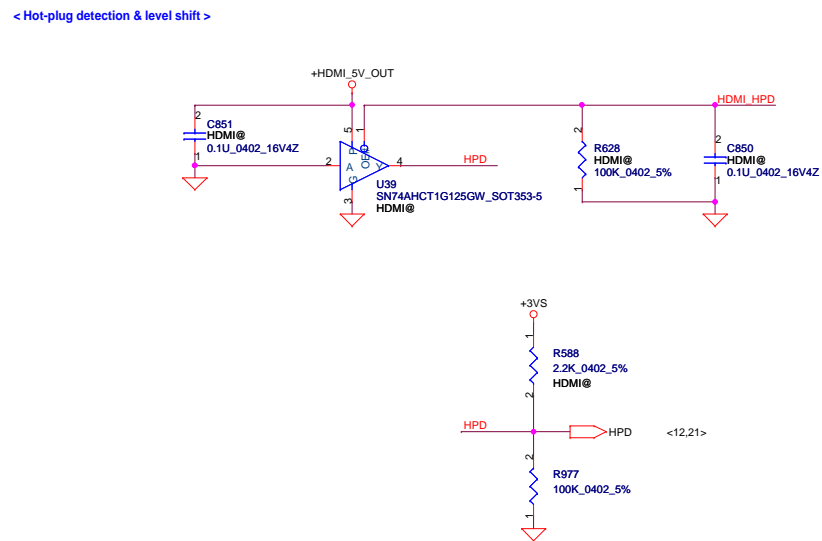
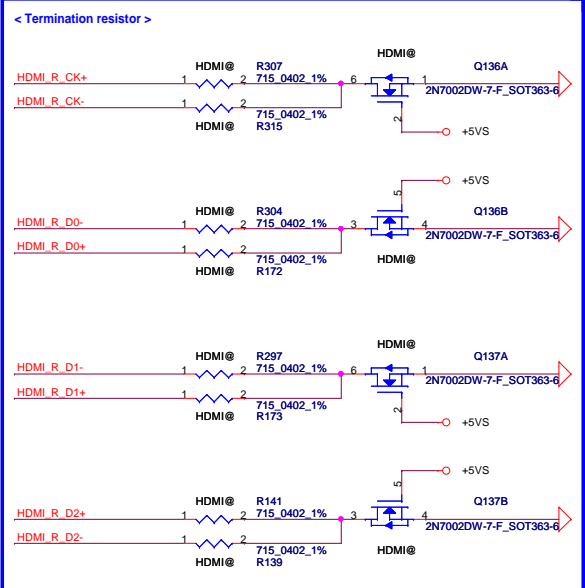
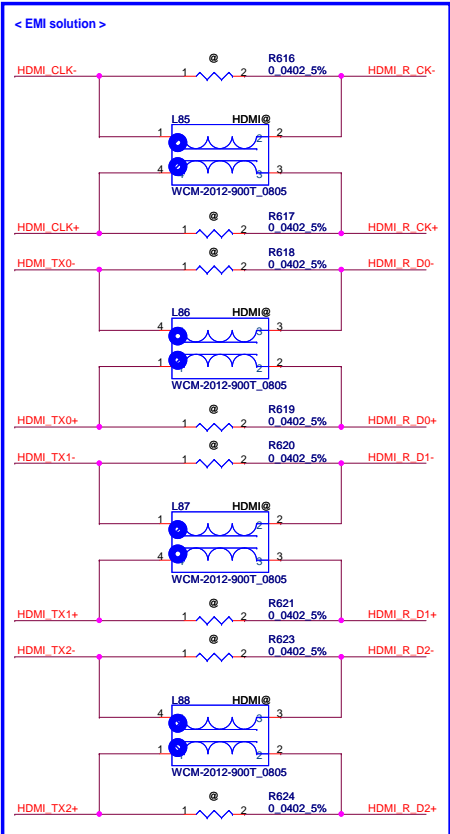
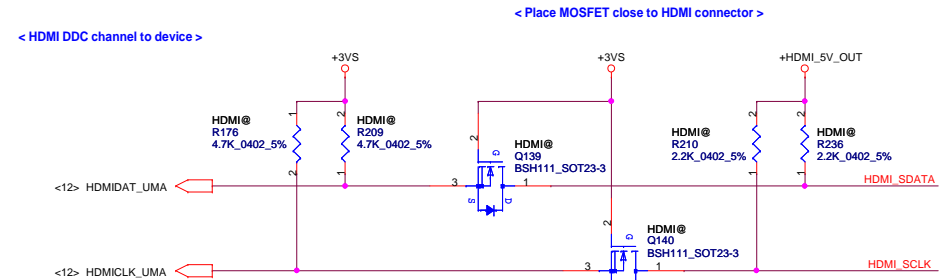
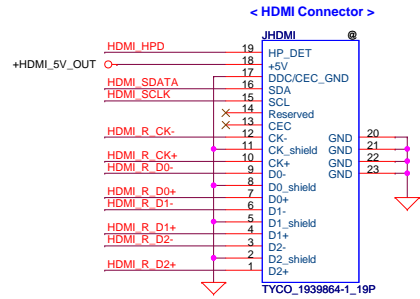
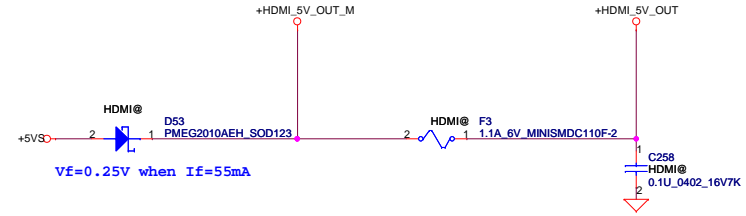


LCD/PANEL BD. Conn.

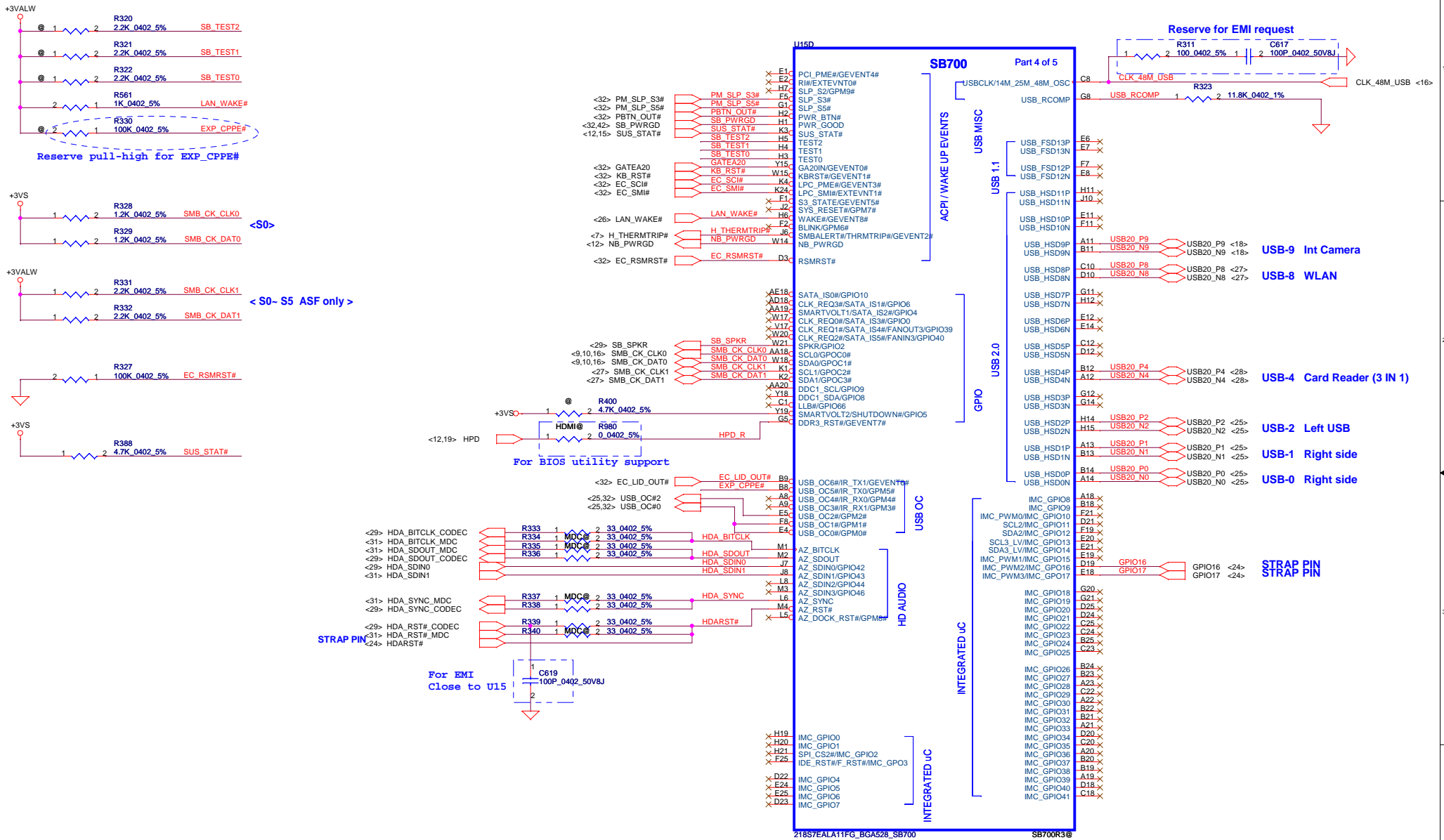


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<11>	HDMI_TXD0+	HDMI@	C189	1	2	0.1U_0402_16V7K	HDMI_TX0+
<11>	HDMI_TXD0-	HDMI@	C188	1	2	0.1U_0402_16V7K	HDMI_TX0-
<11>	HDMI_TXD1+	HDMI@	C190	1	2	0.1U_0402_16V7K	HDMI_TX1+
<11>	HDMI_TXD1-	HDMI@	C184	1	2	0.1U_0402_16V7K	HDMI_TX1-
<11>	HDMI_TXD2+	HDMI@	C187	1	2	0.1U_0402_16V7K	HDMI_TX2+
<11>	HDMI_TXD2-	HDMI@	C191	1	2	0.1U_0402_16V7K	HDMI_TX2-
<11>	HDMI_CLK0+	HDMI@	C185	1	2	0.1U_0402_16V7K	HDMI_CLK+
<11>	HDMI_CLK0-	HDMI@	C186	1	2	0.1U_0402_16V7K	HDMI_CLK-



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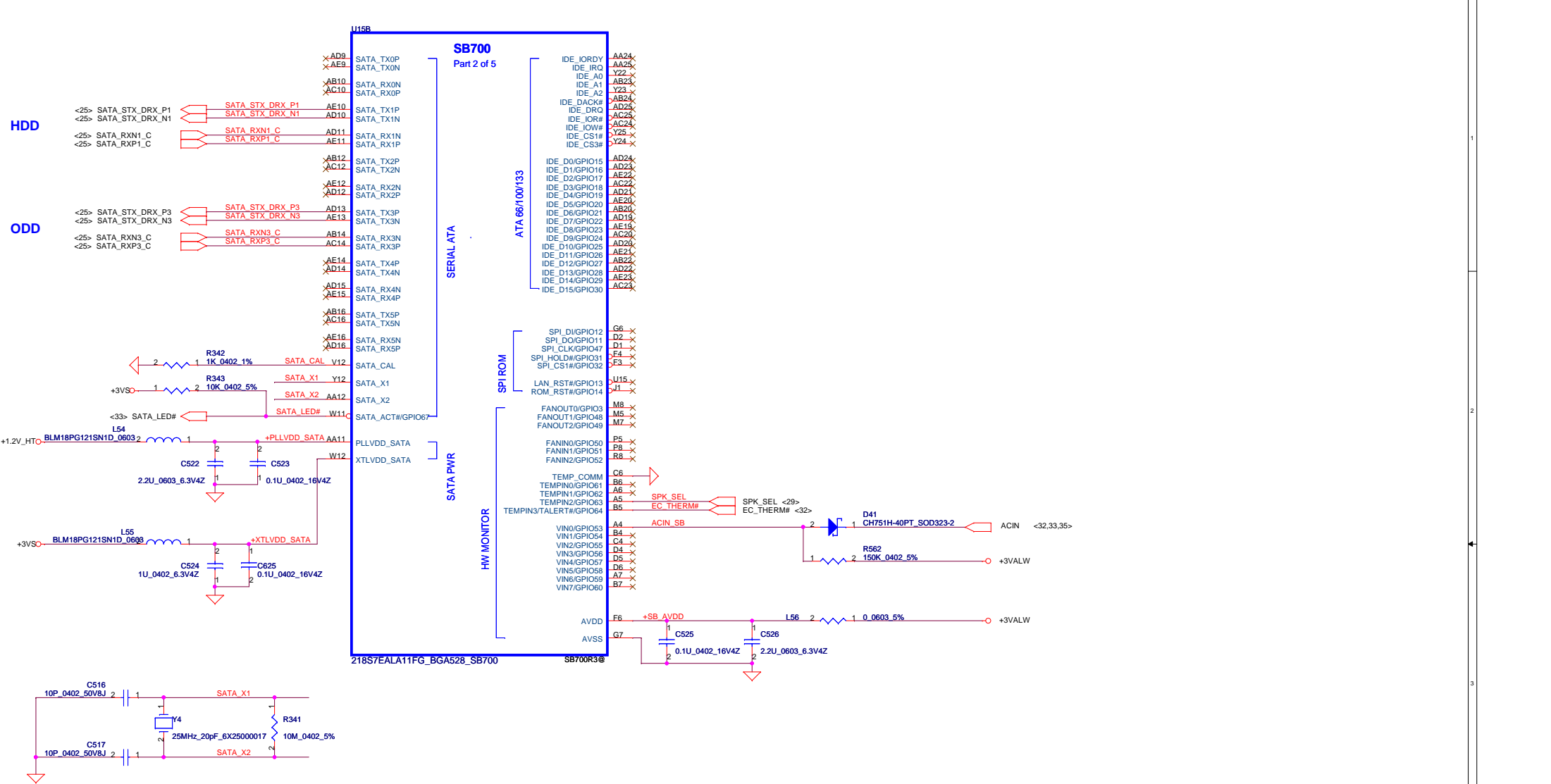


Security Classification	Compal Secret Data		Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	SB700 USB / AC97
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Date:	Wednesday, August 12, 2009	Sheet	21	of 44

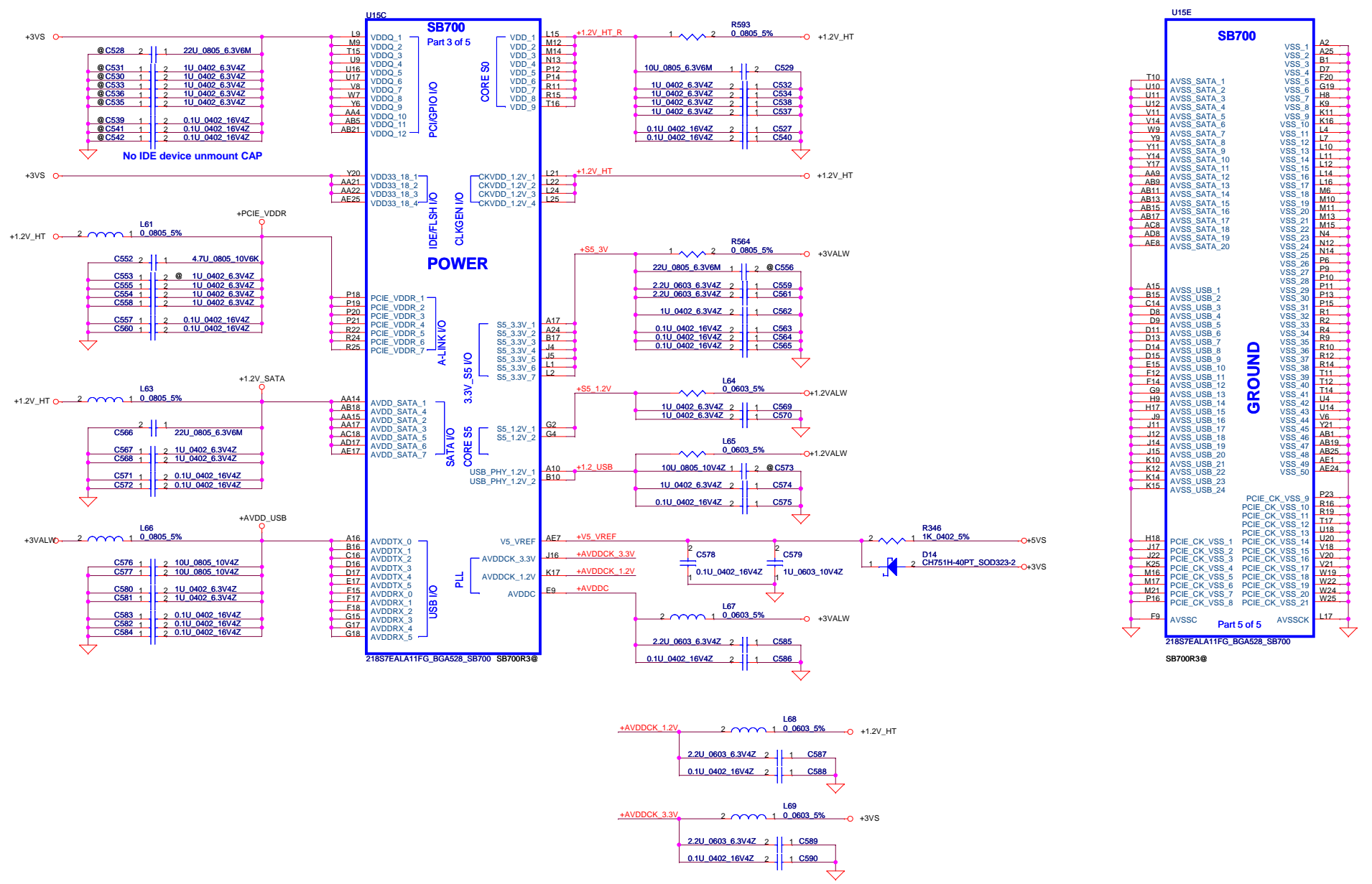
Compal Electronics, Inc.

SB700 USB / AC97

Document Number: LA-5831P
 Rev: 1.0



Security Classification	Compal Secret Data		Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	SB700 SATA / IDE / SPI
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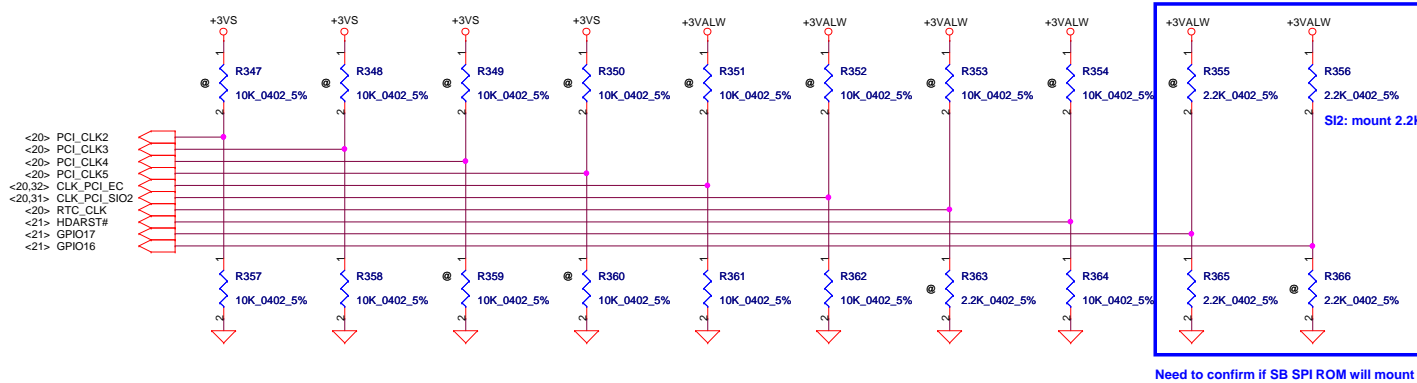


Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	SB700 Power / GND	
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

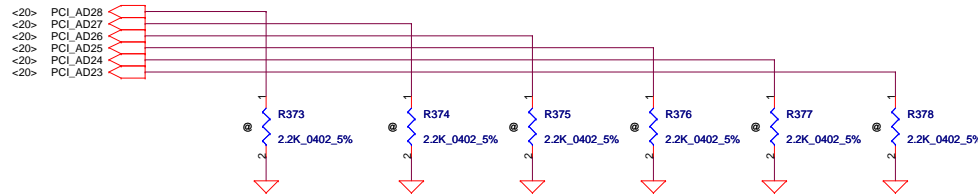
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



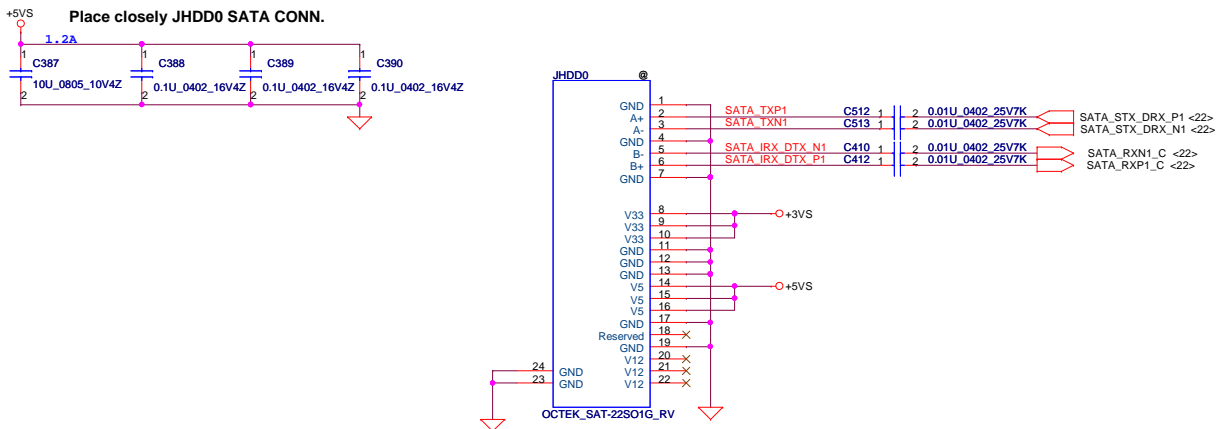
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

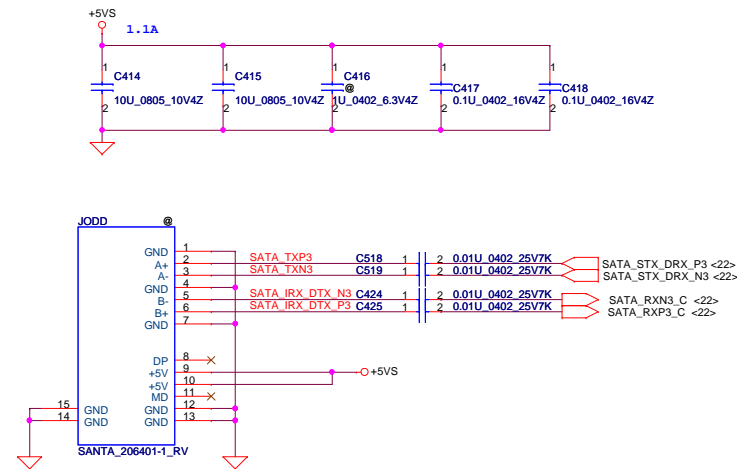
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



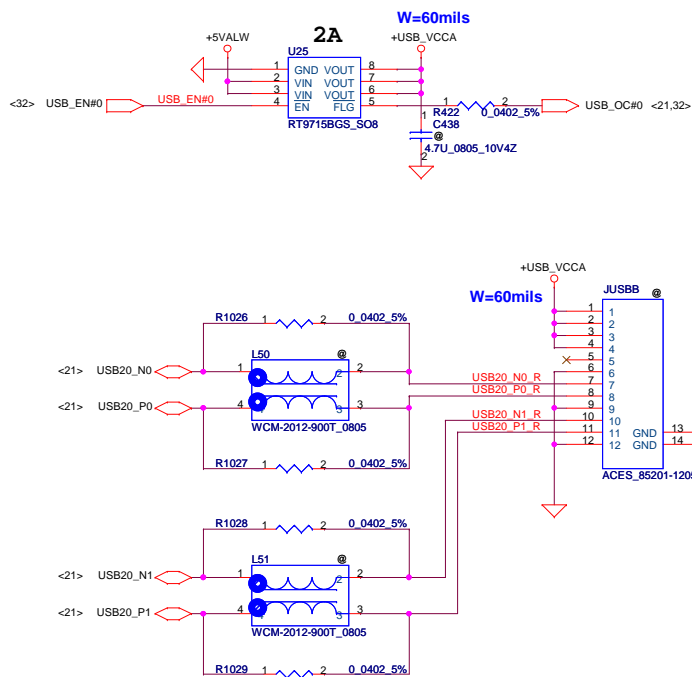
SATA HDD Conn.



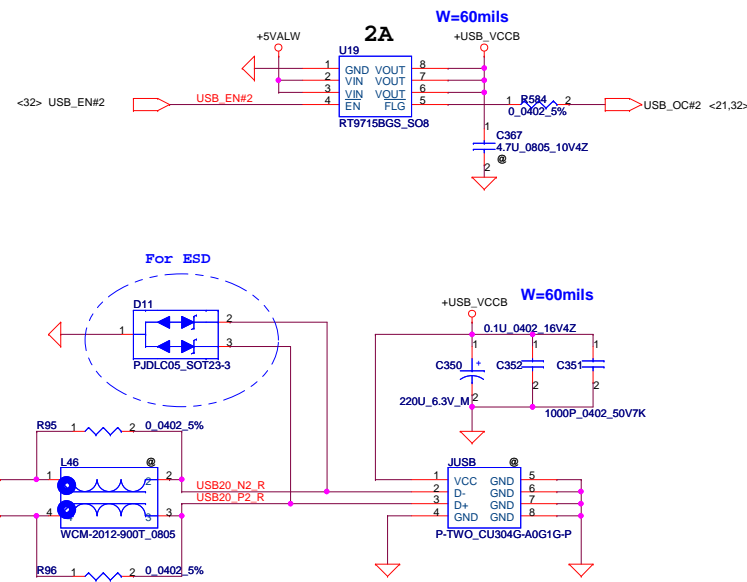
SATA ODD Conn



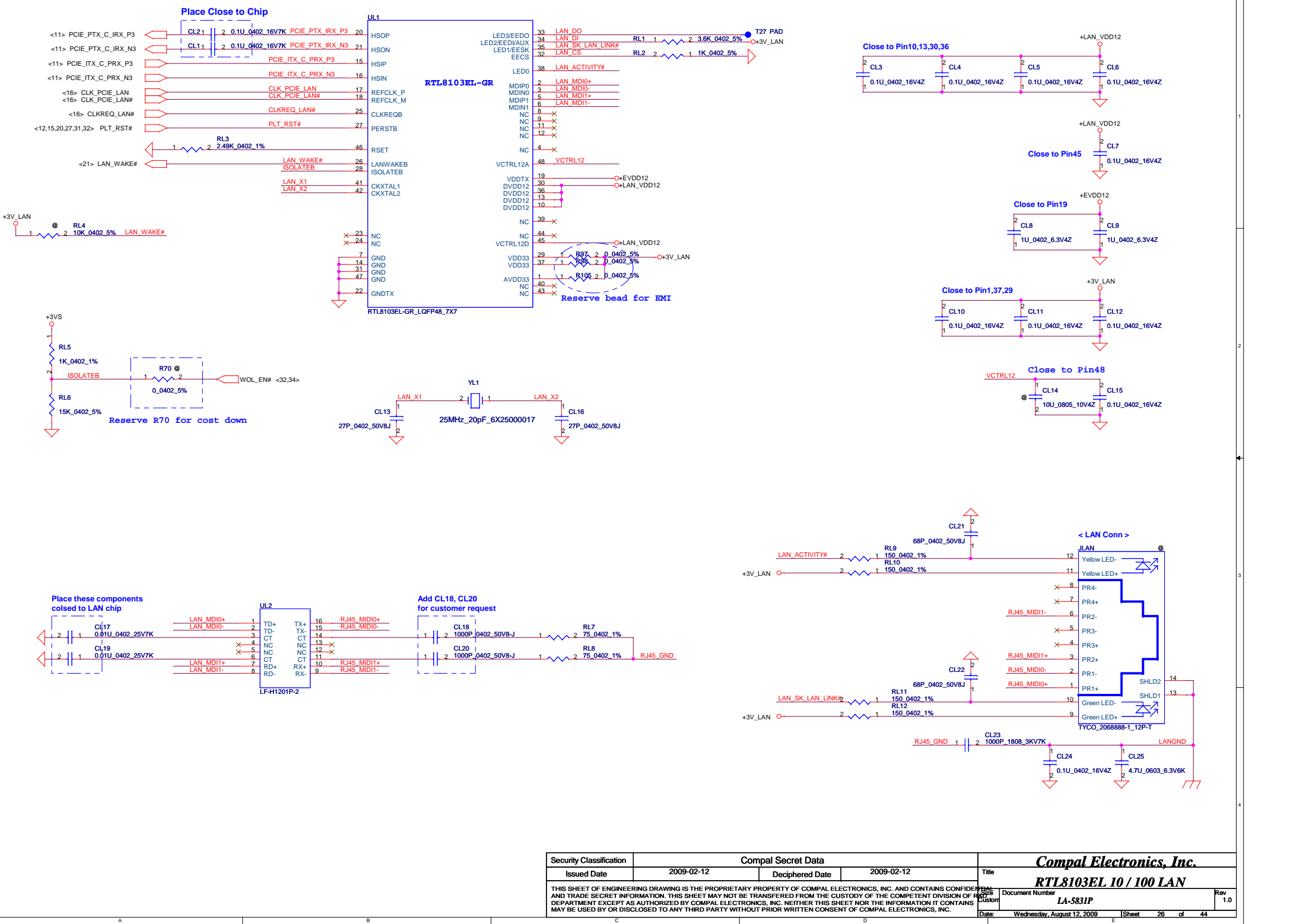
USB Right Board



USB Left Conn



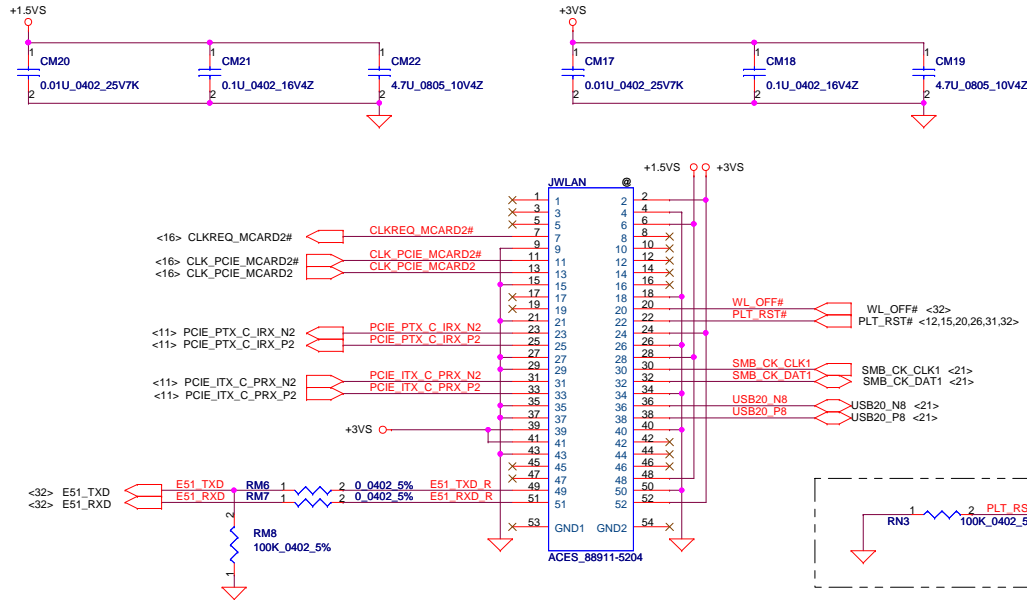
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	SATA HDD/ODD	
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RTL8103EL 10 / 100 LAN	
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< PCIe Mini Card for WLAN/ WiMAX >

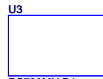


<NB & SB >

< R1 for customer BOM STRUCTURE >

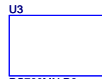
< R3 for mass production BOM STRUCTURE >

RS780MN



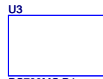
RS780MN R1
RS780MNR1@

RS780MN



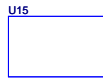
RS780MN R3
RS780MNR3@

RS780MC



RS780MC R1
RS780MCR1@

SB700



SB700R1
SB700R1@

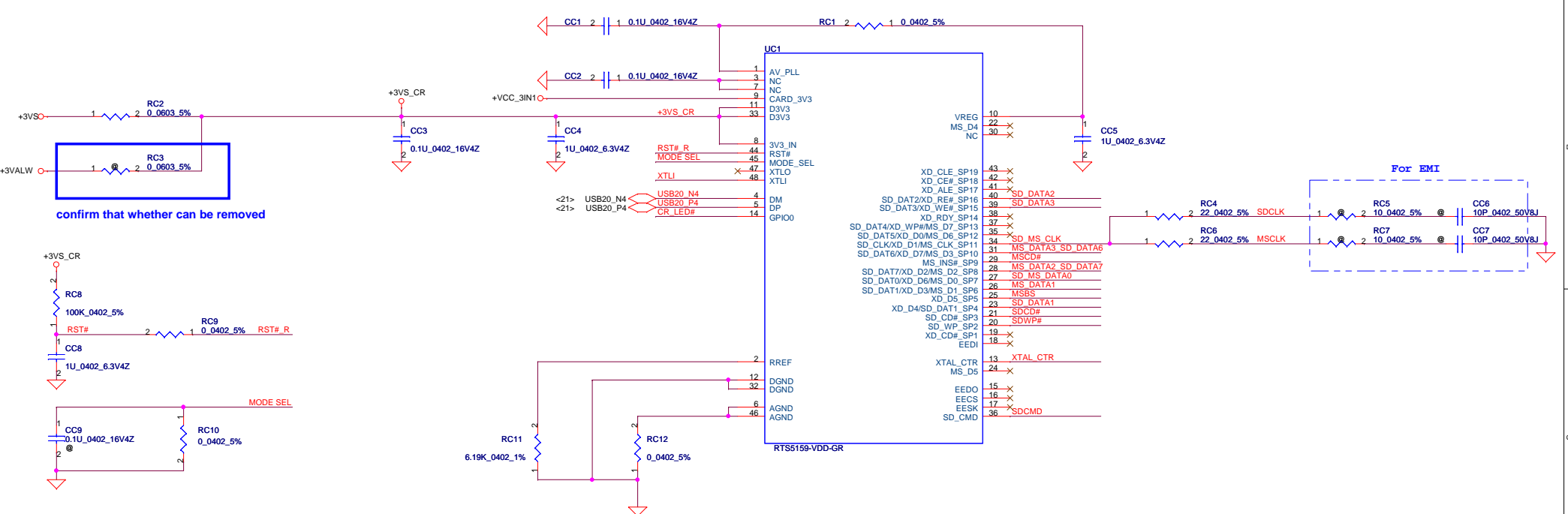
< PCB >

PCB

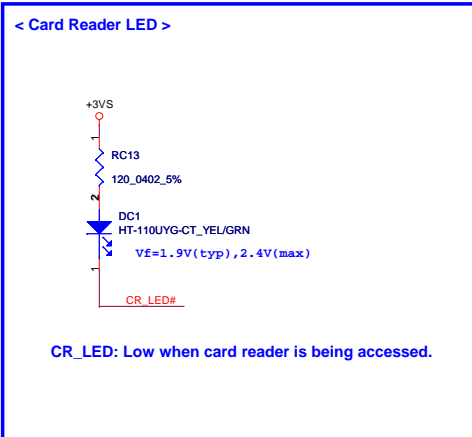


PCB 075 LA-5831P REV1 M/B

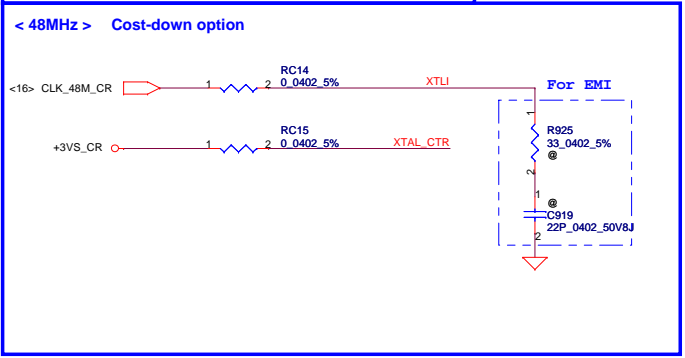
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Issued Date	2009-02-12	Deciphered Date	2009-02-12	Compal Electronics, Inc.
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Date: Wednesday, August 12, 2009				Rev 1.0
Sheet 27 of 44				



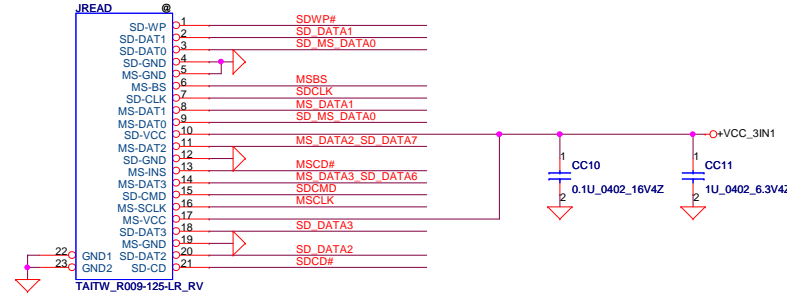
confirm that whether can be removed



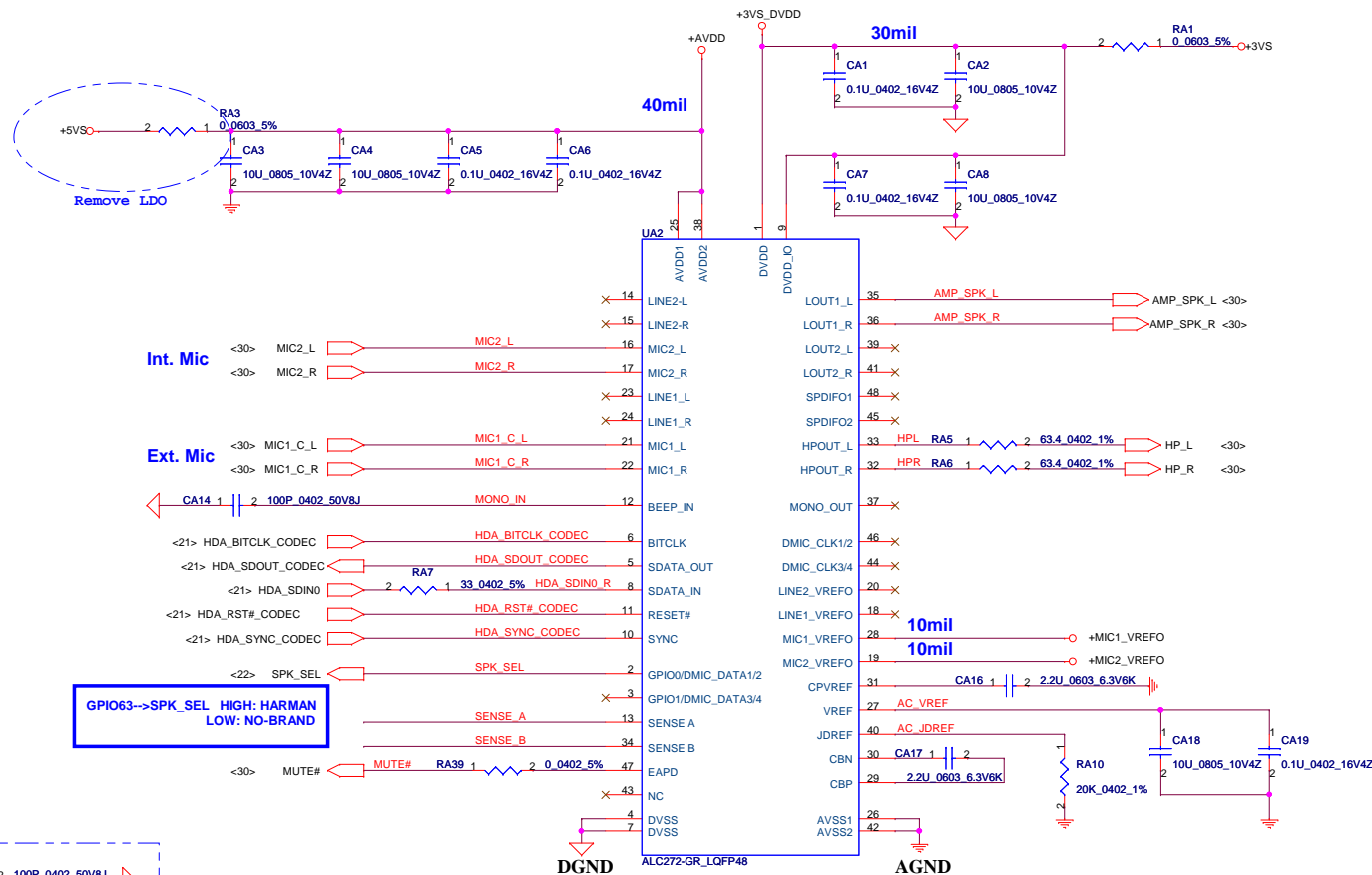
CR_LED: Low when card reader is being accessed.



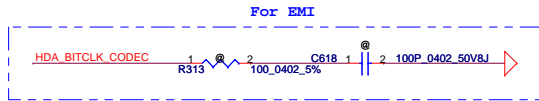
< 3 in 1 Card Reader >



R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

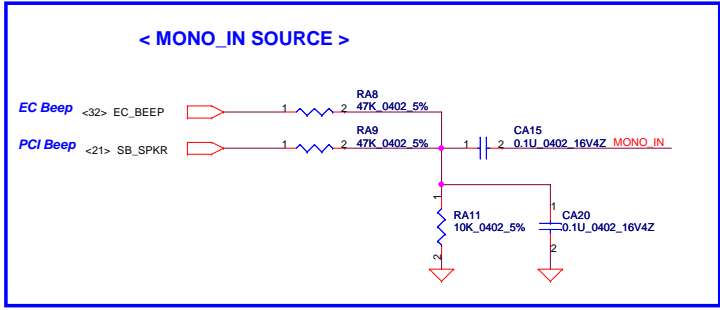
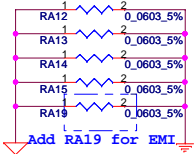


**GPIO63-->SPK_SEL HIGH: HARMAN
LOW: NO-BRAND**

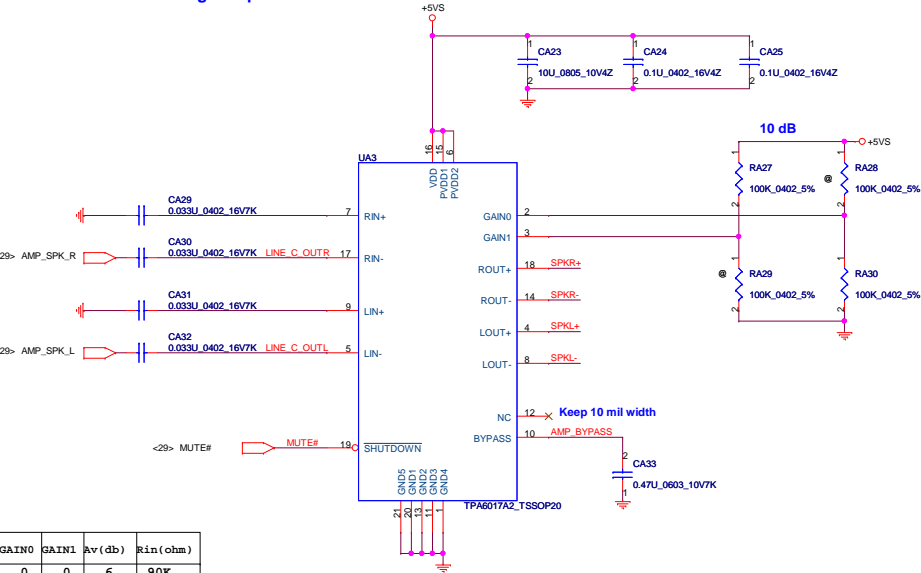


< SENSE_A & SENSE_B, place close to chip >

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	/
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	/
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	/
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	/
	5.1K	PORT-I (PIN 32, 33)	Headphone out

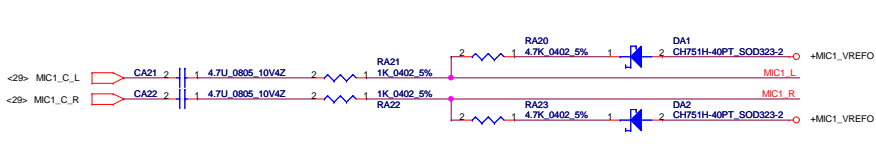


< TPA6017 Medium Range Amplifier >

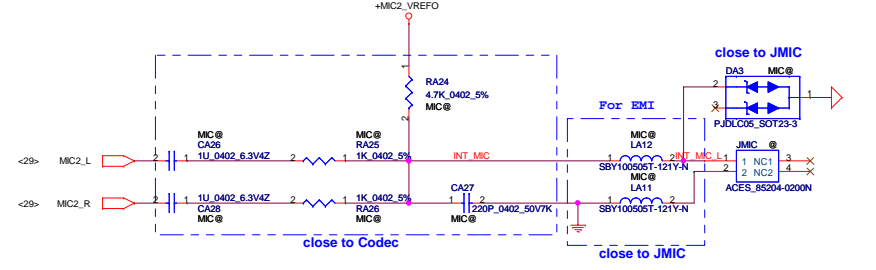


GAIN0	GAIN1	Av (db)	R.in (ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

< Ext. Mic >

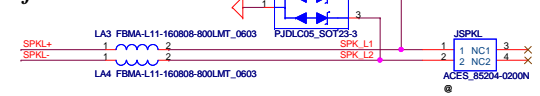


< Int. Mic >

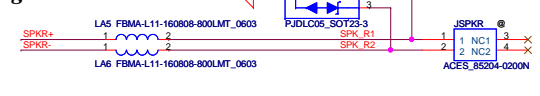


< Speaker Connector >

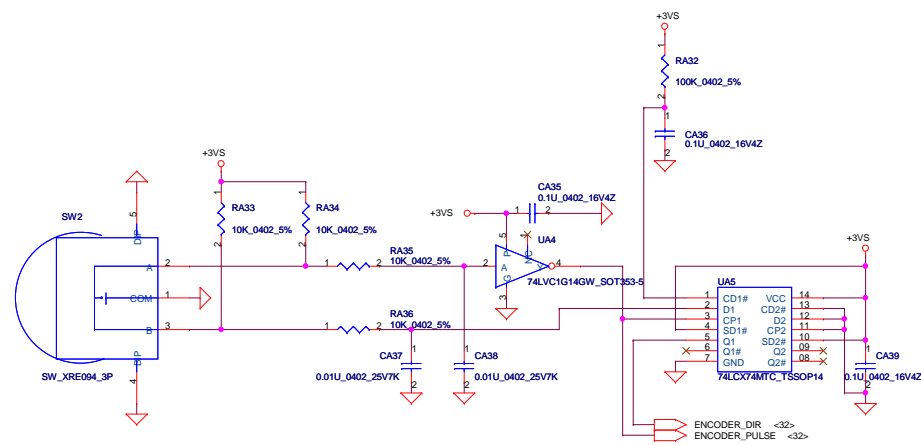
Left Connector



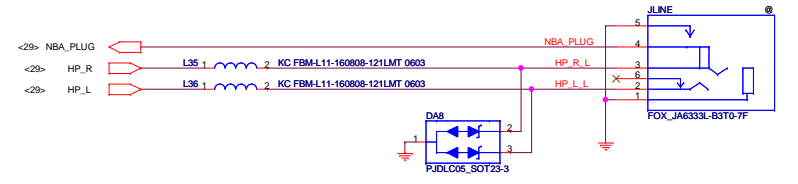
Right Connector



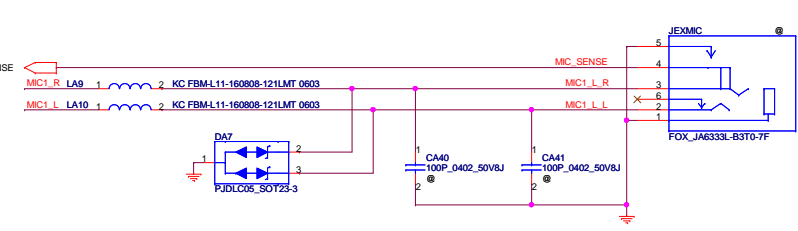
< Volume Control >



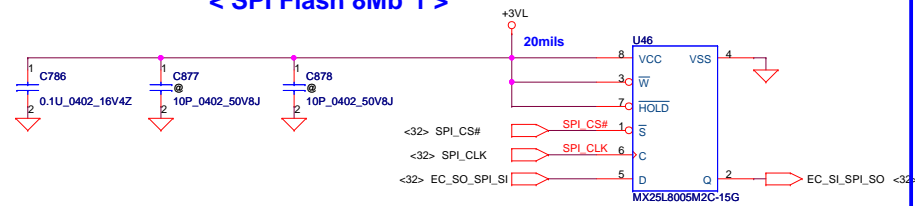
< HeadPhone JACK >



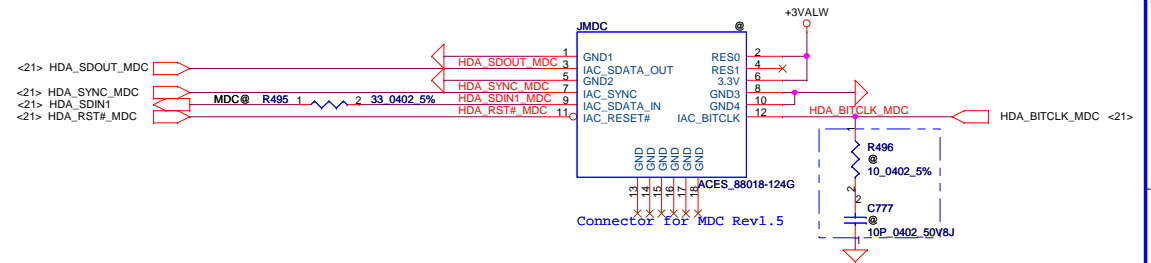
< Ext.MIC/LINE IN JACK >



< SPI Flash 8Mb*1 >

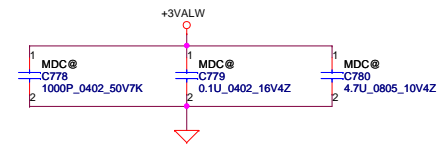
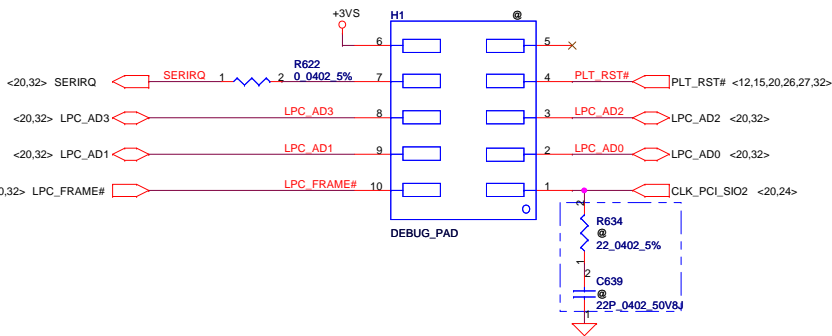


< MDC 1.5 Conn >

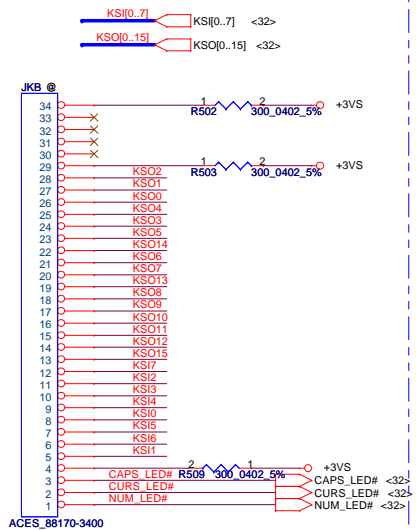


< LPC Debug Port >

Please place the PAD under DDR DIMM.



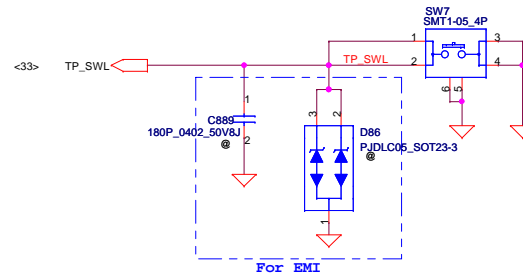
KEYBOARD CONN.



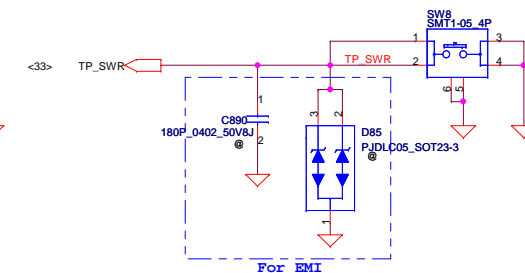
For EMI

KSO2	C725	100P_0402_50V8J
KSO1	C717	100P_0402_50V8J
KSO0	C721	100P_0402_50V8J
KSO4	C609	100P_0402_50V8J
KSO3	C724	100P_0402_50V8J
KSO5	C728	100P_0402_50V8J
KSO14	C730	100P_0402_50V8J
KSO6	C715	100P_0402_50V8J
KSO7	C732	100P_0402_50V8J
KSO13	C733	100P_0402_50V8J
KSO8	C740	100P_0402_50V8J
KSO9	C737	100P_0402_50V8J
KSO10	C729	100P_0402_50V8J
KSO11	C738	100P_0402_50V8J
KSO12	C718	100P_0402_50V8J
KSO15	C736	100P_0402_50V8J
KSI7	C716	100P_0402_50V8J
KSI2	C741	100P_0402_50V8J
KSI3	C726	100P_0402_50V8J
KSI4	C723	100P_0402_50V8J
KSI0	C723	100P_0402_50V8J
KSI5	C731	100P_0402_50V8J
KSI6	C739	100P_0402_50V8J
KSI6	C735	100P_0402_50V8J
KSI1	C734	100P_0402_50V8J
CAPS_LED#	C734	100P_0402_50V8J
CURS_LED#	C722	100P_0402_50V8J
CURS_LED#	C727	100P_0402_50V8J
NUM_LED#	C714	100P_0402_50V8J

Left switch

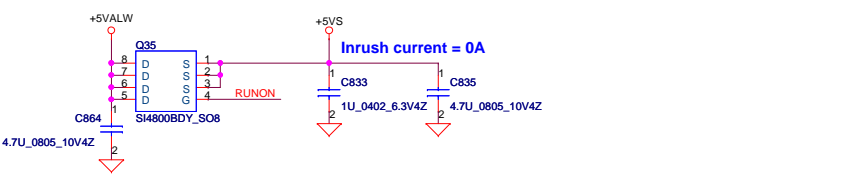


Right Switch

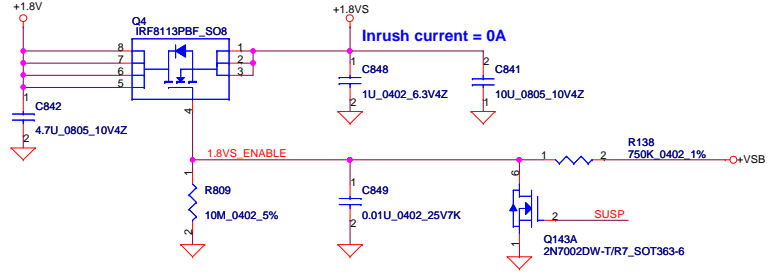


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Issued Date	2009-02-12	Deciphered Date	2009-02-12	SPI / LPC / MDC	
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File No.	Document Number	Rev	LA-5831P		
Date:	Wednesday, August 12, 2009	Sheet	31	of	44

< +5VALW TO +5VS >

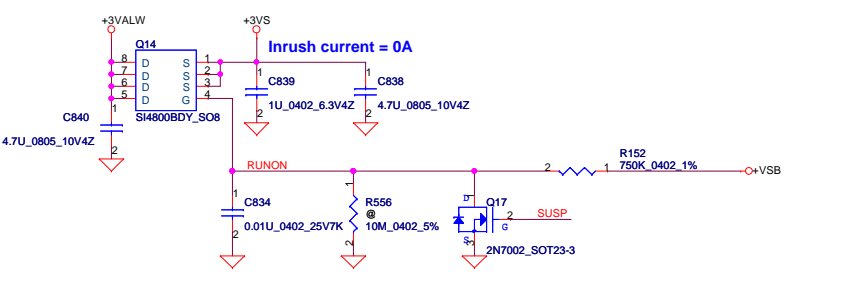


< close to PQ20, must EMI confirm > < +1.8V TO +1.8VS >

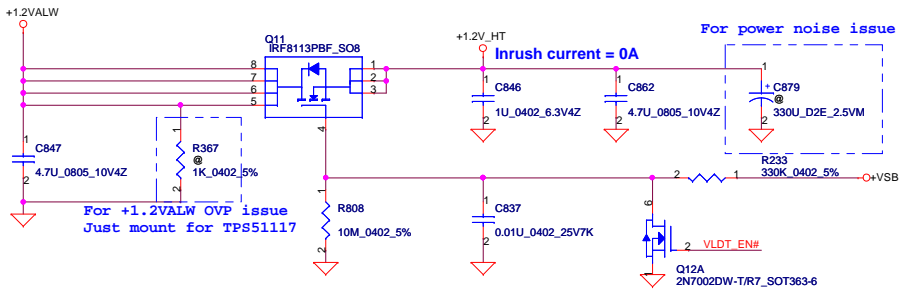


< +3VALW TO +3VS >

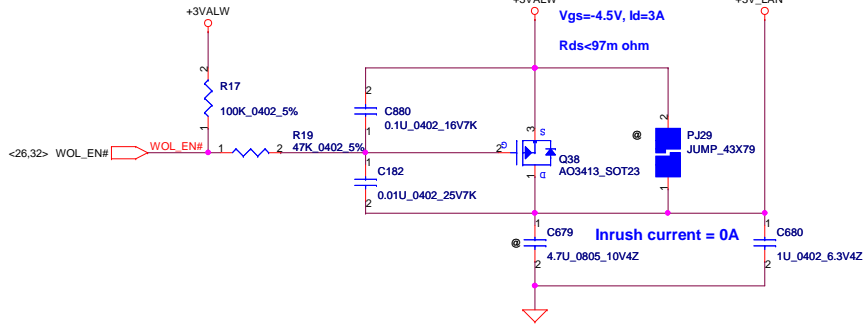
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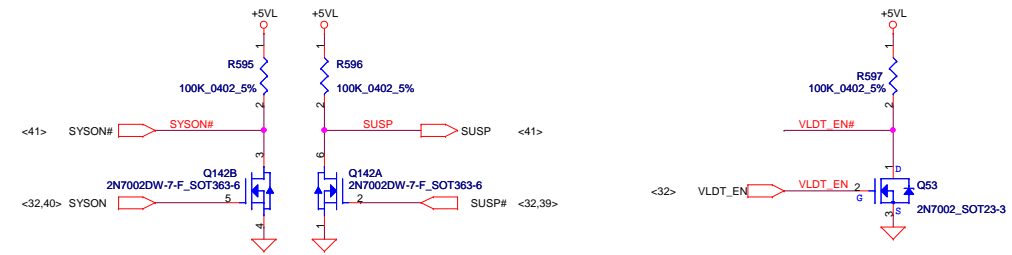
< +1.2VALW TO +1.2V_HT >



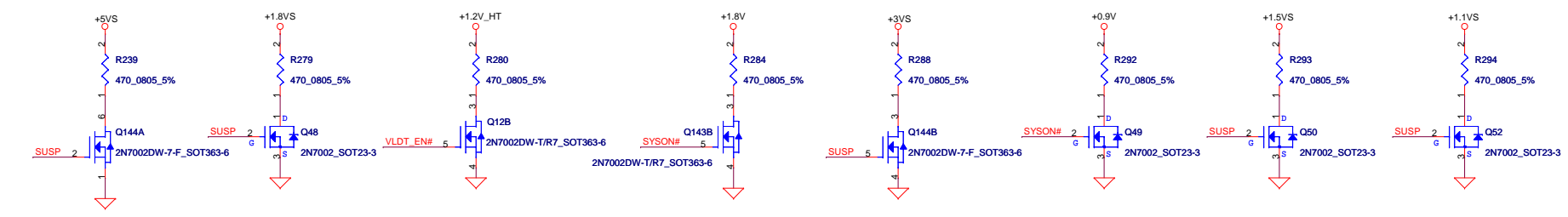
< +3VALW TO +3V_LAN >



< Inversion of SYSON#, SUSP#, VLDT_EN, EC_ON >

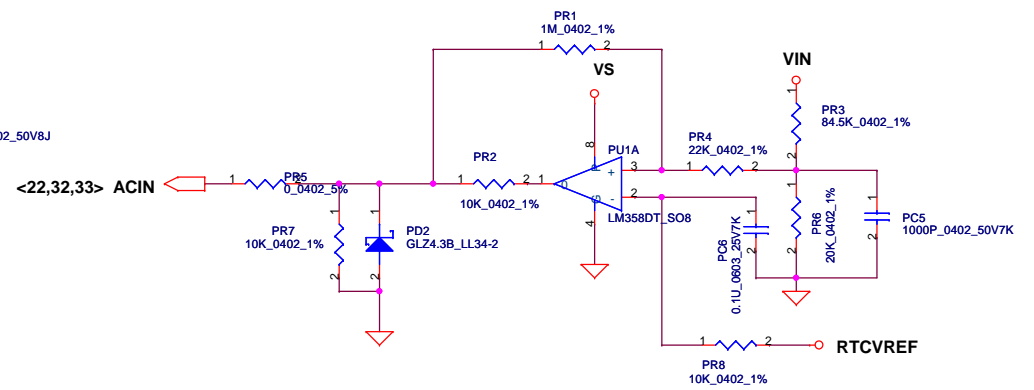
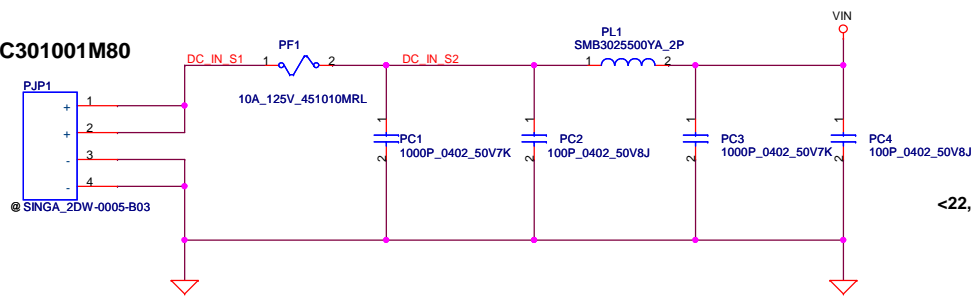


< Discharge circuit >

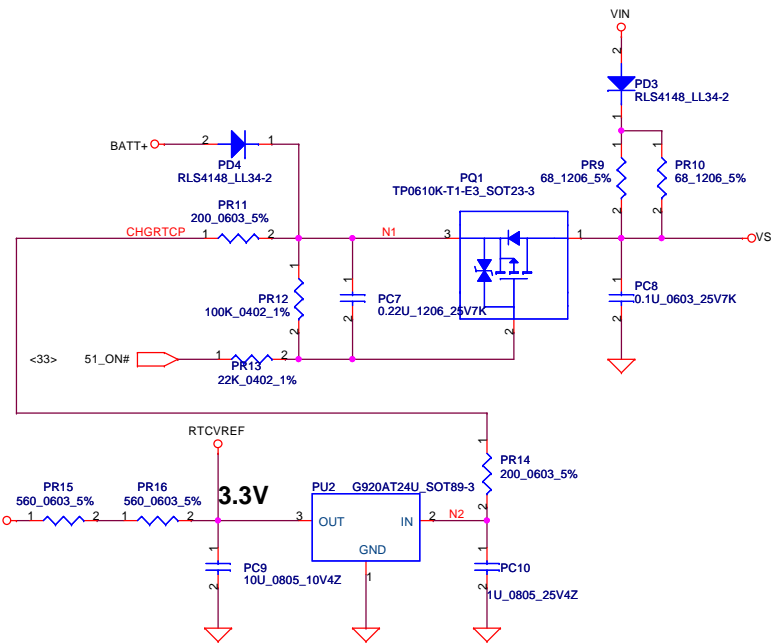


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				Rev 1.0
				Sheet 34 of 44

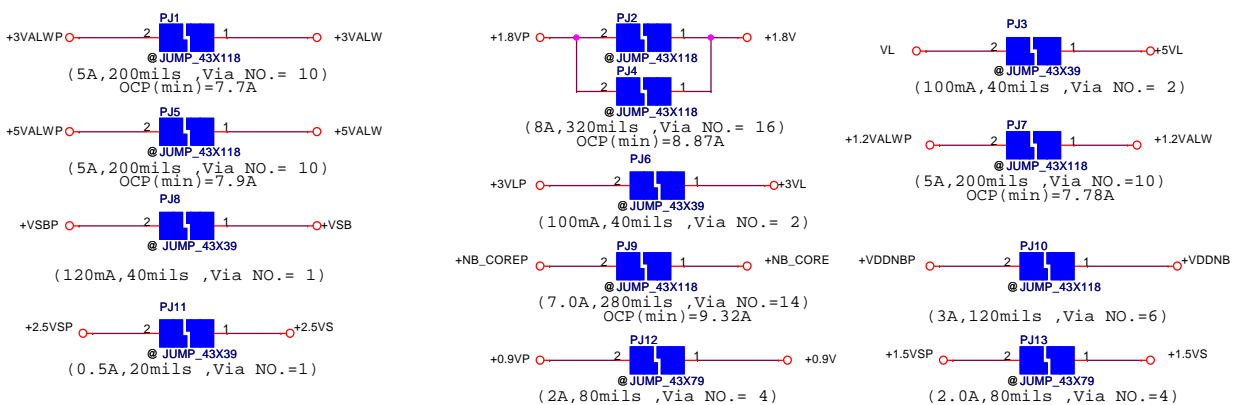
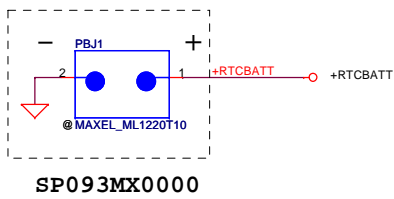
DC301001M80



Vin Detector		
High	18.384	17.901 17.430
Low	17.728	17.257 16.976

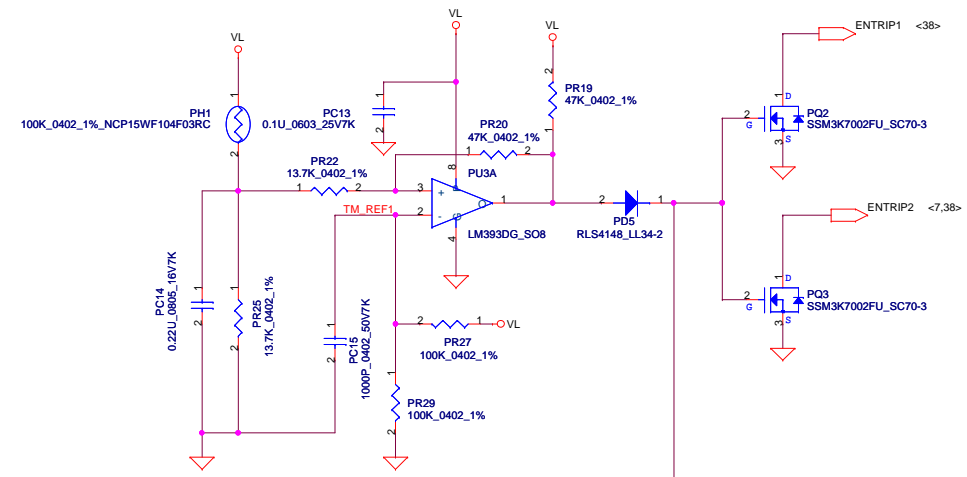
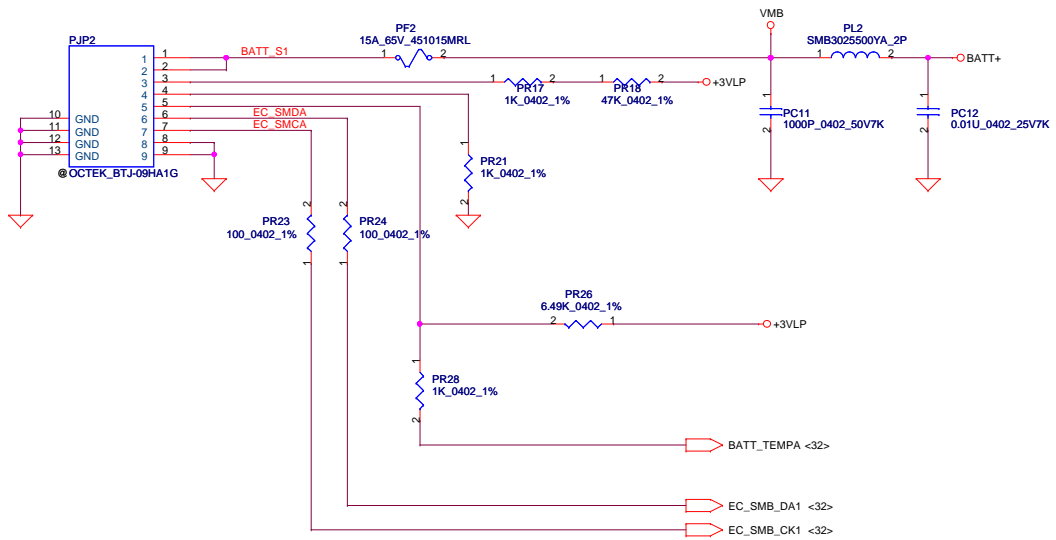


RTC Battery

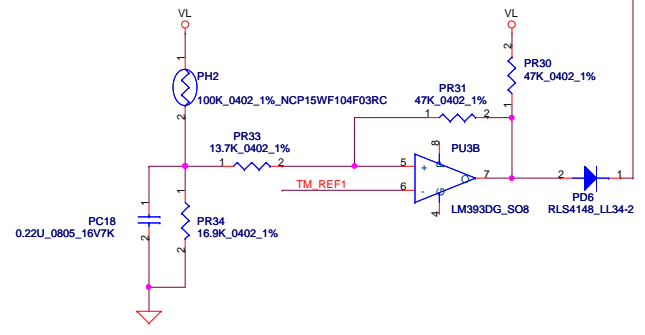
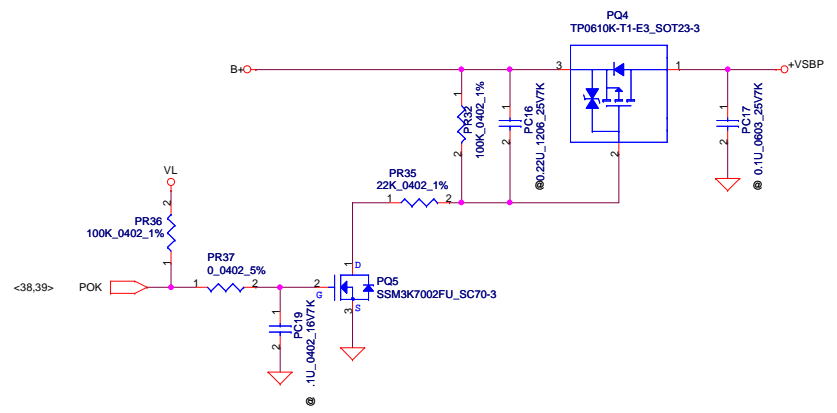


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Date:	Wednesday, August 12, 2009	Sheet	35 of 44	Rev 1.0

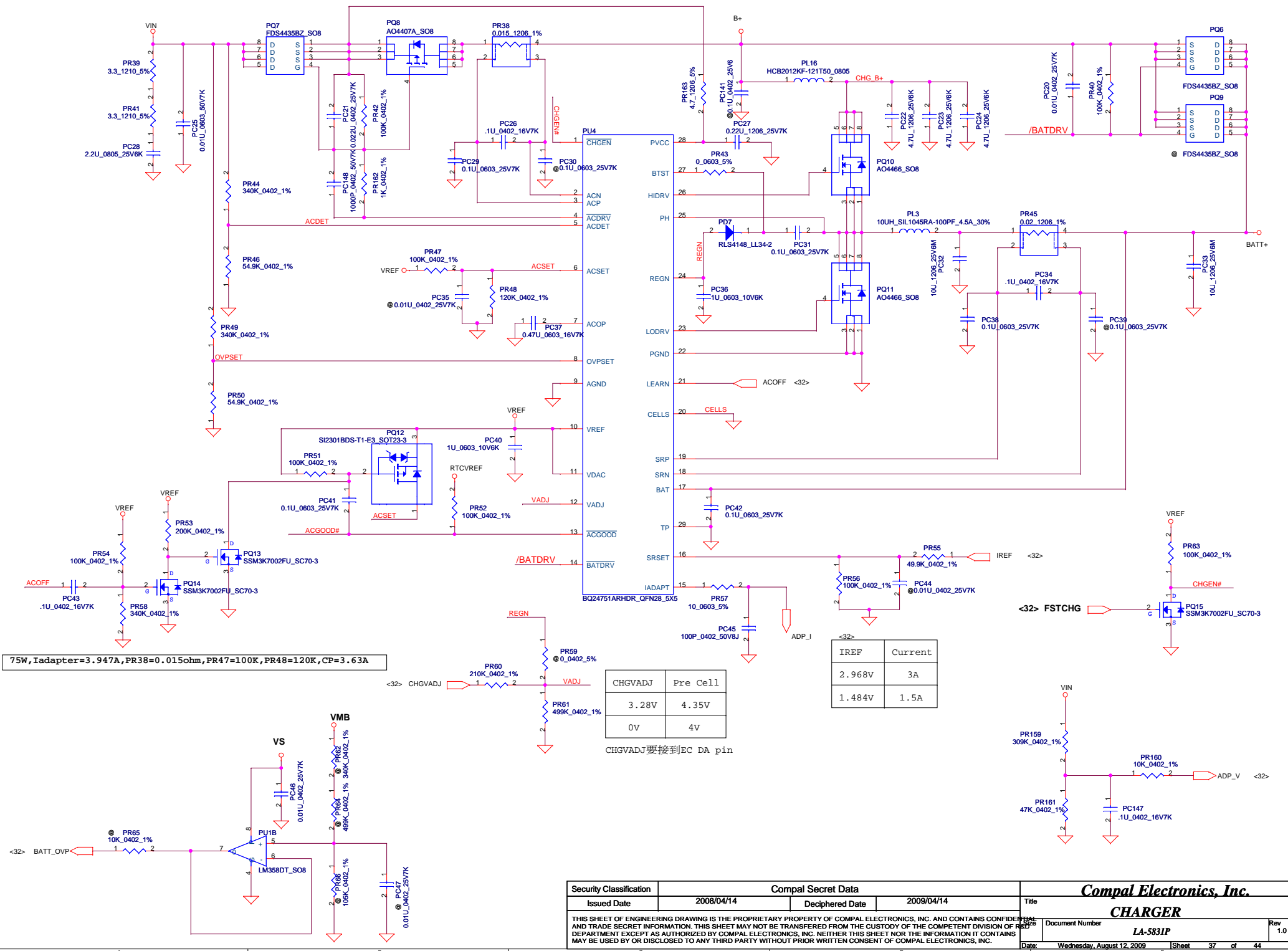
PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 92 degree C
 Recovery at 56 degree C



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75W, Iadapter=3.947A, PR38=0.015ohm, PR47=100K, PR48=120K, CP=3.63A

CHGVADJ	Pre Cell
3.28V	4.35V
0V	4V

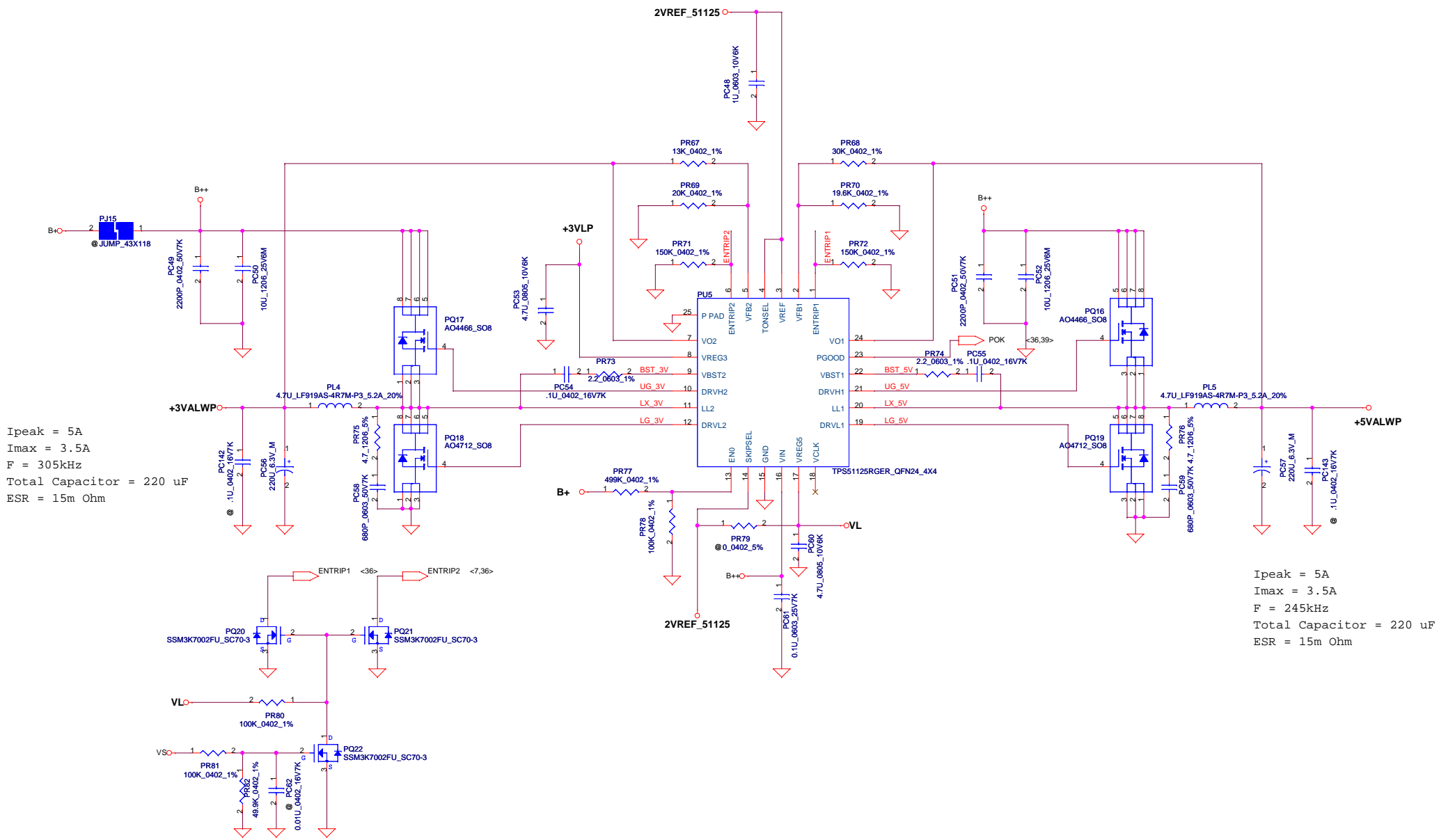
CHGVADJ要接到EC DA pin

IREF	Current
2.968V	3A
1.484V	1.5A

Security Classification	Compal Secret Data		Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	CHARGER
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Date: Wednesday, August 12, 2009				Sheet 37 of 44

Compal Electronics, Inc.

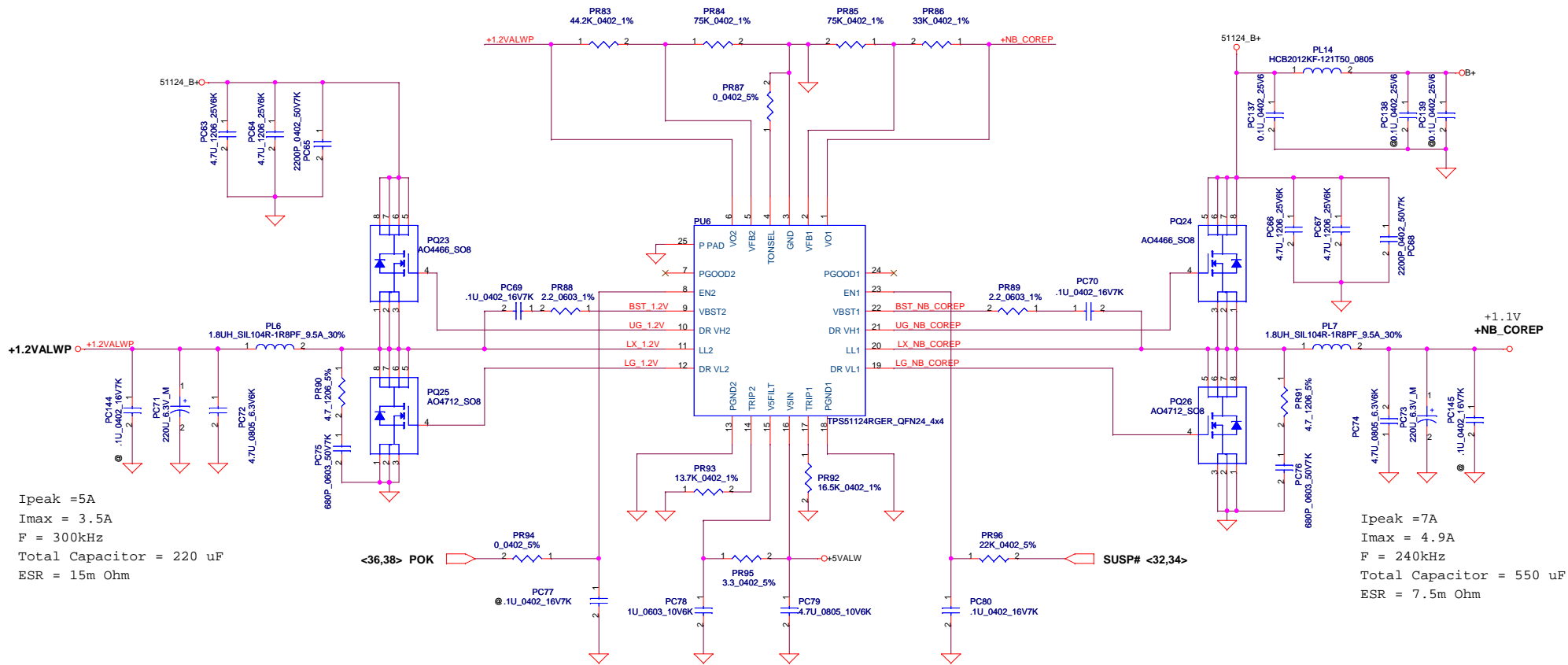
CHARGER



$I_{peak} = 5A$
 $I_{max} = 3.5A$
 $F = 305kHz$
 Total Capacitor = 220 uF
 ESR = 15m Ohm

$I_{peak} = 5A$
 $I_{max} = 3.5A$
 $F = 245kHz$
 Total Capacitor = 220 uF
 ESR = 15m Ohm

Security Classification	Compal Secret Data		Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	2008/04/14
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Date:	Wednesday, August 12, 2009	Sheet	38	of 44



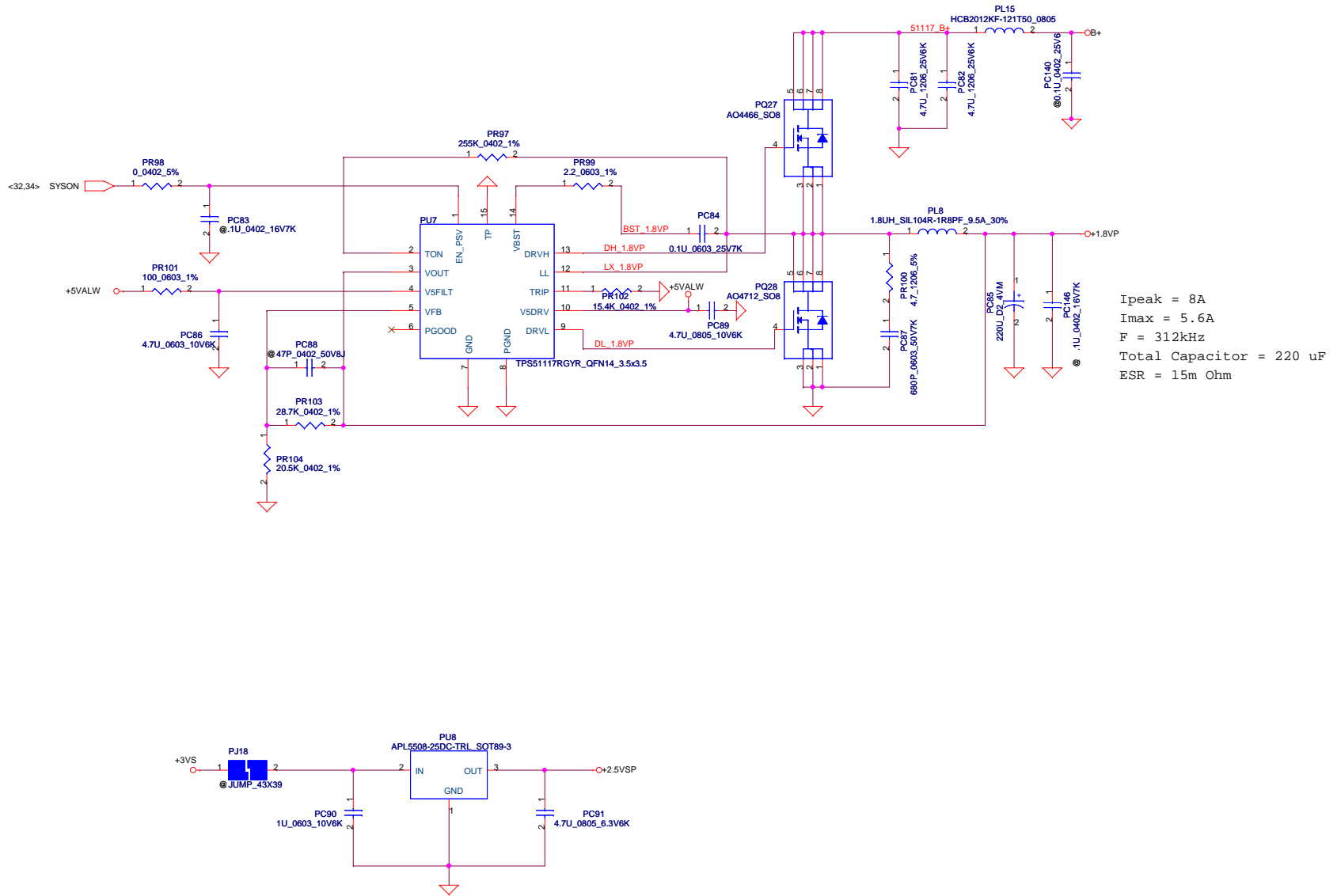
Ipeak = 5A
 Imax = 3.5A
 F = 300kHz
 Total Capacitor = 220 uF
 ESR = 15m Ohm

Ipeak = 7A
 Imax = 4.9A
 F = 240kHz
 Total Capacitor = 550 uF
 ESR = 7.5m Ohm

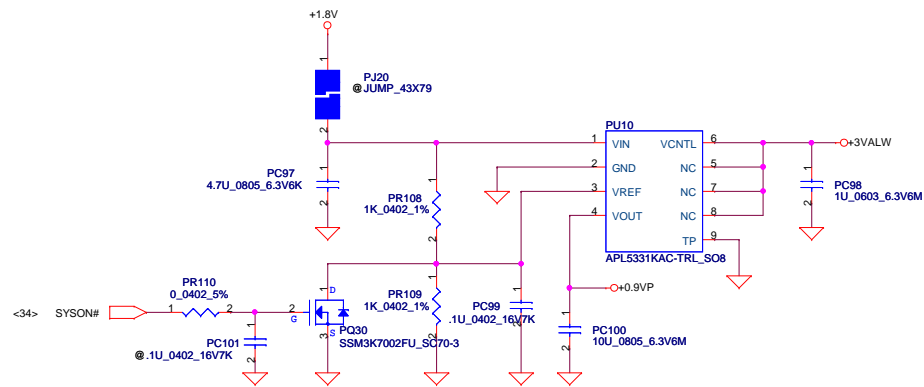
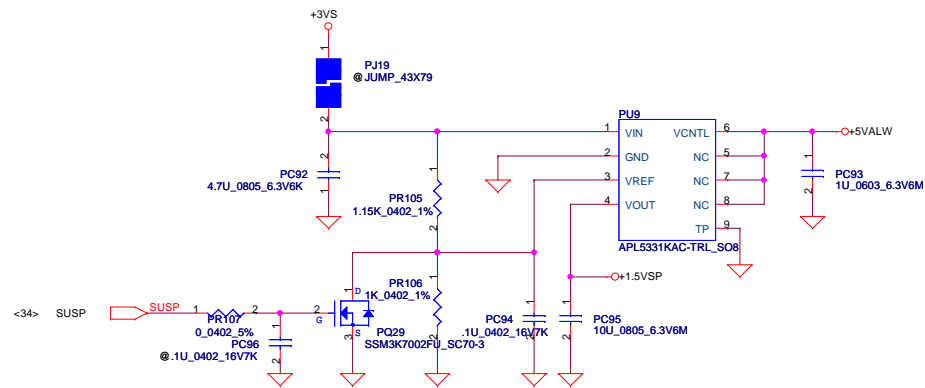
Security Classification	Compal Secret Data		Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Document Number
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				1.0
Date: Wednesday, August 12, 2009				Sheet 39 of 44

Compal Electronics, Inc.
NB COREP/1.2VALWP

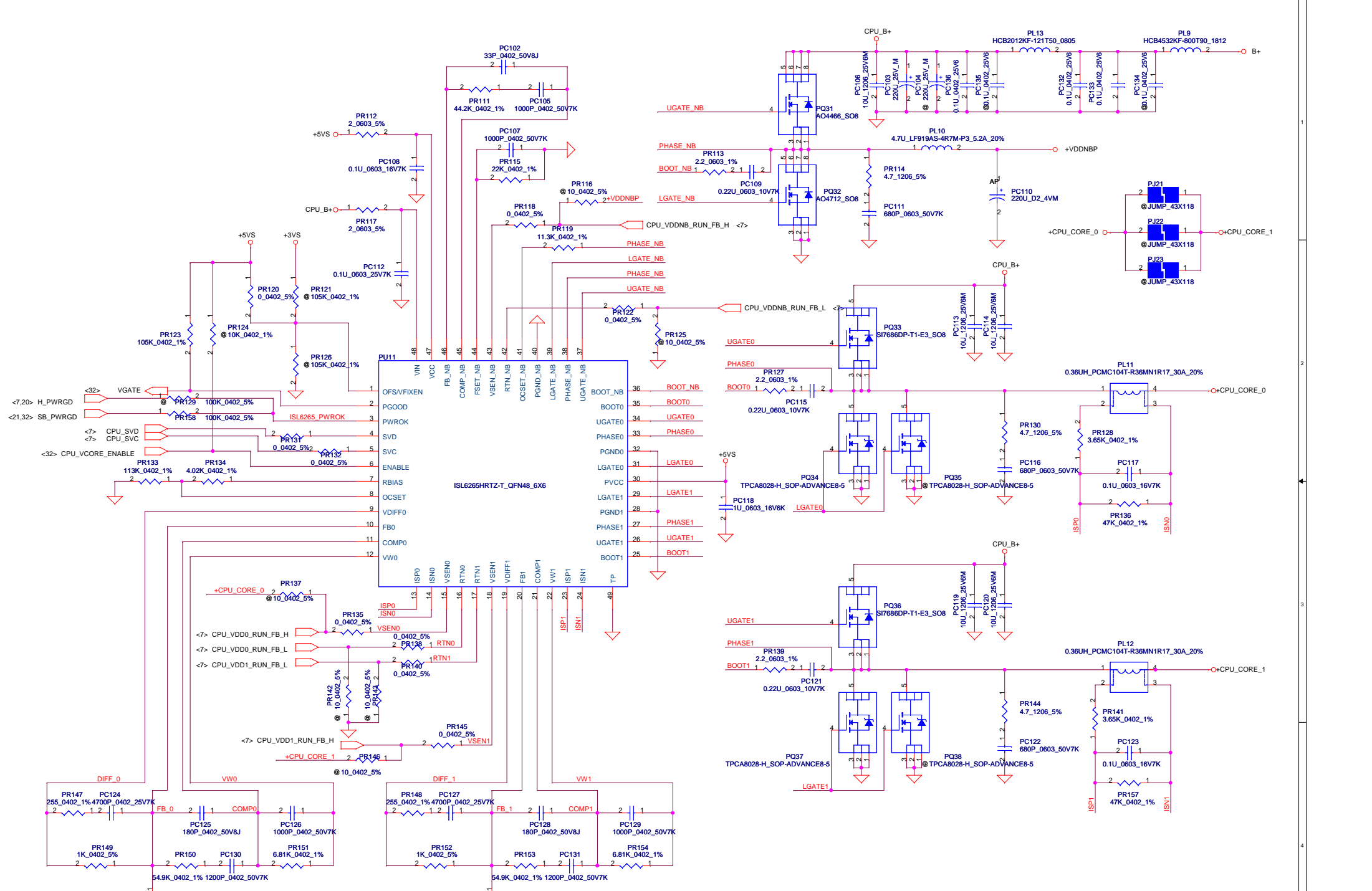
LA-5831P



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Issued Date	2008/04/14	Deciphered Date	2009/04/14	1.8VP/2.5VS	
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Security Classification	Compal Secret Data		Title	
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Date:	Wednesday, August 12, 2009	Sheet	41	of 44



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		+CPU CORE	
2008/04/14		2009/04/14		LA-583IP	
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				LA-583IP	1.0
				Date: Wednesday, August 12, 2009	Sheet 42 of 44

Version Change List (P. I. R. List) for Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
35-43	PVT		2009/07/20	Release			
39-40	Pre-MP	Change PL6,PL7,PL8	2009/07/30	POWER		Change PL6,PL7,PL8 footprint	
38	Pre-MP	Change PC56	2009/07/30	POWER		change to common circuit.	
36	Pre-MP	Change PH1,PH2	2009/08/4	POWER		change to common circuit.	
37	Pre-MP	Change PR38,PR45	2009/08/4	POWER		change to common circuit.	

Security Classification	Compal Secret Data			Title Compal Electronics, Inc.		
Issued Date	2009-02-12	Deciphered Date	2009-02-12	List History		
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				LA-5831P	1.0	
				Date: Wednesday, August 12, 2009	Sheet	43 of 44

HW4 Product Improvement Record (P.I.R.)

NEWAE LA-5831P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 1.0

GERBER-OUT DATE: 2009/08/07

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	7/21	25	Change JUSBB footprint back to E-T_6905-E12N-00R_12P	USB/B pin define reverse
2	7/27	25	Add D11	For ESD
3	7/27	9	Add C120-C123	For EMI
4	7/27	32	Add R344 and R345	For EC pin damage issue
5	7/30	26	Add R97, R98 and R105	Reserve bead for EMI
6	8/6	18	Add C707, C708 and C709	For EMI
7	8/6	30	Add LA11 and LA12	For EMI
8	8/6	32	Add R74 and C607	For EMI
9	8/6	31	Delete R518 and C606	For EMI
10	8/6	7	Add C124	For EMI

Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	PIR		
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