EE CHARACTERIZATION TP

NAND

PP9401 P4MM SM (PP) 1 FMI0_DQS — PLACE_SIDE=BOTTOM, PLACE_NEAR=U0652.D34:2MM — 6 12 53
PP9402 P4MM SM (PP) 1 FMI0_AD<3> — PLACE_SIDE=BOTTOM, PLACE_NEAR=U0652.C34:2MM — 6 12
PP9403 P4MM SM (PP) 1 FMI0_DQS — PLACE_NEAR=U0652.D34:2MM — 6 12 53

PP9410 P4MM SM (PP) 1 TP_TCKC_U1400 — 12
PP9411 P4MM SM (PP) 1 TP_TMSC_U1400 — 12
PP9412 P4MM SM (PP) 1 TP_U1400_RB0 — 12
PP9413 P4MM SM (PP) 1 TP_U1400_RB1 — 12

DWI

PP9405 P4MM SM (PP) 1 DWI_AP_DO — PLACE_SIDE=BOTTOM, PLACE_NEAR=U0100:2MM — 5 48

AUDIO

PP9406 P4MM SM (PP) 1 I2S0_CODEC_ASP_MCK — PLACE_NEAR=U1900:2MM — 5 15

PP9416 P4MM SM (PP) 1 I2S2_CODEC_XSP_LRCK — PLACE_NEAR=U1900:2MM — 5 15
PP9417 P4MM SM (PP) 1 I2S2_CODEC_XSP_DOUT — PLACE_NEAR=U1900:2MM — 5 15

PP9419 P4MM SM (PP) 1 I2S1_SPKAMP_MCK — PLACE_NEAR=U2040:2MM — 5 16
PP9420 P4MM SM (PP) 1 I2S1_SPKAMP_BCLK — PLACE_NEAR=U2040:2MM — 5 16
PP9421 P4MM SM (PP) 1 I2S1_SPKAMP_LRCK — PLACE_NEAR=U2040:2MM — 5 16
PP9422 P4MM SM (PP) 1 I2S1_SPKAMP_DOUT — PLACE_NEAR=U2040:2MM — 5 16
PP9423 P4MM SM (PP) 1 I2S1_SPKAMP_DIN — PLACE_SIDE=BOTTOM, PLACE_NEAR=U0652:2MM — 5 16

PP9424 P4MM SM (PP) 1 SPI2_CODEC_SCLK — PLACE_NEAR=U1900:2MM — 5 15
PP9425 P4MM SM (PP) 1 SPI2_CODEC_MOSI — PLACE_NEAR=U1900:2MM — 5 15
PP9426 P4MM SM (PP) 1 SPI2_CODEC_MISO — PLACE_SIDE=BOTTOM, PLACE_NEAR=U0652:2MM — 5 15

GRAPE

OSCAR

PP9428 P4MM SM (PP) 1 UART4_SOC2OSCAR_TXD — PLACE_SIDE=BOTTOM, PLACE_NEAR=U2400:2MM — 5 19
PP9429 P4MM SM (PP) 1 UART4_OSCAR2SOC_RXD — PLACE_SIDE=BOTTOM, PLACE_NEAR=U0652:2MM — 5 19

UART5

CAMERA

PP9440 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_CLK_P — PLACE_NEAR=U0652.AR33:3MM — 7 20 53
PP9441 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_CLK_N — PLACE_NEAR=U0652.AR34:3MM — 7 20 53
PP9442 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_DATA_P<0> — PLACE_NEAR=U0652.AT33:3MM — 7 20 53
PP9443 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_DATA_N<0> — PLACE_NEAR=U0652.AT34:3MM — 7 20 53
PP9444 P4MM SM (PP) 1 MIPI0C_CAM_REAR_CLK_P — PLACE_NEAR=U0652.AU25:3MM — 7 23 53
PP9445 P4MM SM (PP) 1 MIPI0C_CAM_REAR_CLK_N — PLACE_NEAR=U0652.AV25:3MM — 7 23 53
PP9446 P4MM SM (PP) 1 MIPI0C_CAM_REAR_DATA_P<0> — PLACE_NEAR=U0652.AU27:3MM — 7 23 53
PP9447 P4MM SM (PP) 1 MIPI0C_CAM_REAR_DATA_N<0> — PLACE_NEAR=U0652.AV27:3MM — 7 23 53

FOR FRANK (SEG)

PP9450 P4MM SM (PP) 1 PPVDD_SOC_SOC_SENSE — PLACE_NEAR=U0652.V31:1MM — 9
PP9451 P4MM SM (PP) 1 PPVDD_CPU_SOC_SENSE — PLACE_NEAR=U0652.AN30:1MM — 9

WIFI

PP9480 P4MM SM (PP) HSIC1_WLAN2SOC_DEVICE_RDY — 5 44
PP9481 P4MM SM (PP) HSIC1_WLAN2SOC_REMOTE_WAKE — 5 44
PP9482 P4MM SM (PP) PMU_GPIO_WLAN_HOST_WAKE — 44 48
PP9483 P4MM SM (PP) HSIC1_SOC2WLAN_HOST_RDY — 5 44

GPIO_BT_WAKE — FUNC_TEST=TRUE — 5 44

FOR HSIC CHARACTERIZATION

PP9460 P4MM SM (PP) 1 HSIC1_WLAN_DATA — PLACE_NEAR=U0652.AM33:3MM — 4 44 53
PP9462 P4MM SM (PP) 1 HSIC1_WLAN_DATA — PLACE_NEAR=U5800.13:3MM — 4 44 53
PP9463 P4MM SM (PP) 1 HSIC1_WLAN_STB — PLACE_NEAR=U5800.14:3MM — 4 44

PP9468 P4MM SM (PP) 1 UART1_BT2SOC_TX — PLACE_NEAR=U0652:3MM — 5 44
PP9469 P4MM SM (PP) 1 UART1_SOC2BT_TX — PLACE_NEAR=U5800:3MM — 5 44

PP9471 P4MM SM (PP) 1 UART2_WLAN2SOC_TX — PLACE_NEAR=U0652:3MM — 5 44
PP9472 P4MM SM (PP) 1 UART2_SOC2WLAN_TX — PLACE_NEAR=U5800:3MM — 5 44

BASEBAND

USB_BB_P — FUNC_TEST=TRUE — 11 24 52
USB_BB_N — FUNC_TEST=TRUE — 11 24 52

FOR HSIC CHARACTERIZATION

PP9465 P4MM SM (PP) 1 HSIC2_BB_STB — PLACE_NEAR=U0652.B27:3MM — 4 24 27
PP9466 P4MM SM (PP) 1 HSIC2_BB_DATA — PLACE_NEAR=U3400.C7:3MM — 4 24 27

PROX

HIGH SPEED, NO TEST

MIPI0C_CAM_REAR_CLK_P — NO_TEST=TRUE — 7 23 53
MIPI0C_CAM_REAR_CLK_N — NO_TEST=TRUE — 7 23 53
MIPI0C_CAM_REAR_DATA_P<0..3> — NO_TEST=TRUE — 7 23 53
MIPI0C_CAM_REAR_DATA_N<0..3> — NO_TEST=TRUE — 7 23 53
MIPI0C_CAM_REAR_CLK_FILT_P — NO_TEST=TRUE — 23
MIPI0C_CAM_REAR_CLK_FILT_N — NO_TEST=TRUE — 23
MIPI0C_CAM_REAR_DATA_FILT_P<0..3> — NO_TEST=TRUE — 23
MIPI0C_CAM_REAR_DATA_FILT_N<0..3> — NO_TEST=TRUE — 23
MIPI1C_CAM_FRONT_CLK_P — NO_TEST=TRUE — 7 20 53
MIPI1C_CAM_FRONT_CLK_N — NO_TEST=TRUE — 7 20 53
MIPI1C_CAM_FRONT_DATA_P<0> — NO_TEST=TRUE — 7 20 53
MIPI1C_CAM_FRONT_DATA_N<0> — NO_TEST=TRUE — 7 20 53
MIPI1C_CAM_FRONT_CLK_FILT_P — NO_TEST=TRUE — 20
MIPI1C_CAM_FRONT_CLK_FILT_N — NO_TEST=TRUE — 20
MIPI1C_CAM_FRONT_DATA_FILT_P<0> — NO_TEST=TRUE — 20
MIPI1C_CAM_FRONT_DATA_FILT_N<0> — NO_TEST=TRUE — 20

EDP_DATA_P<0..3> — NO_TEST=TRUE — 7 18
EDP_DATA_N<0..3> — NO_TEST=TRUE — 7 18
EDP_DATA_EMI_P<0..3> — NO_TEST=TRUE — 18
EDP_DATA_EMI_N<0..3> — NO_TEST=TRUE — 18
EDP_DATA_EMI_CONN_P<0..3> — NO_TEST=TRUE — 18
EDP_DATA_EMI_CONN_N<0..3> — NO_TEST=TRUE — 18

SYNC_MASTER=J72_MLB_C — SYNC_DATE=11/26/2012
PAGE TITLE: TEST: EE TP/PP
Apple Inc.
DRAWING NUMBER: 051-0886 — SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 94 OF 121
SHEET: 53 OF 54

POWER CONNECTIONS

BUCK0

52 46 PPVDD_CPU (MAKE_BASE=TRUE) = =PPVDD_CPU 9

BUCK1

52 46 PPVDD_GPU (MAKE_BASE=TRUE) = =PPVDD_GPU 9

BUCK2

52 46 PPVDD_SOC (MAKE_BASE=TRUE) = =PPVDD_SOC 9

BUCK3

52 47 46 PP1V8_S2R (MAKE_BASE=TRUE)
- =PP1V8_S2R_MISC 5 51
- =PP1V8_S2R_VDDIO_WLAN_BT 44
- =PP1V8_S2R_TRISTAR 11
- =PP1V8_S2R_DDR 8
- =PP1V8_S2R_GRAPE 13
- =PP1V8_S2R_EXT_SWITCH 50
- =PP1V8_S2R_REAR_CAMERA
- =PP1V8_S2R_MESA
- =PP1V8_S2R_VDD_CORE_GPS
- =PP1V8_S2R_VDD_IO_GPS

BUCK3_SW

52 50 46 PP1V8_SW1 (MAKE_BASE=TRUE)
- =PP1V8_AUDIO 15
- =PP1V8_DMIC 14
- =PP1V8_CAM_FRONT 20
- =PP1V8_CAM_REAR 23
- =PP1V8_PROX 22

52 50 PP1V8_EXT_SW (MAKE_BASE=TRUE)
- =PP1V8_VDDIO18_SOC 8 9
- =PP1V8_SOC 4 5 7 10 18
- =PP1V8_MIPI_SOC 7
- =PP1V8_EDP_SOC 7
- =PP1V8_NAND_SOC 6
- =PP1V8_NAND 12 48
- =PP1V8_PLL_SOC 4
- =PP1V8_SPKRAMP
- =PP1V8_EEPROM 51
- =PP1V8_BEACON

52 46 PP1V8_SW2 (MAKE_BASE=TRUE) = =PP1V8_GRAPE 13

46 PP1V8_S2R_SW3 (MAKE_BASE=TRUE)
- =PP1V8_S2R_GYRO 21
- =PP1V8_S2R_ACCEL 21
- =PP1V8_S2R_OSCAR 19
- PP1V8_S2R_SW3_COMP 52 54

54 52 PP1V8_S2R_SW3_COMP (MAKE_BASE=TRUE) = =PP1V8_S2R_COMP 21

PP1V8_S2R_SW3 SHOULD BE ON IN HIBERNATE
CURRENTLY POWERS OSCAR AND 1.8V RAIL ON SENSOR

BUCK4

52 47 46 PP1V2_S2R (MAKE_BASE=TRUE)
- =PP1V2_S2R_DDR 8
- =PP1V2_S2R_DDR_SOC 8
- =PP1V2_S2R_CAM_REAR

BUCK4_SW

52 46 PP1V2_SW1 (MAKE_BASE=TRUE)
- =PP1V2_VDDQ_DDR 8
- =PP1V2_VDDIOD_SOC 8
- =PP1V2_HSIC_SOC 4

52 46 PP1V2_S2R_SW2 (MAKE_BASE=TRUE) = =PP1V2_S2R_OSCAR 19

PP1V2_S2R_SW2 SHOULD BE ON IN HIBERNATE
PROVIDE 1.2V TO OSCAR

BUCK5

52 46 PPVDD_SRAM (MAKE_BASE=TRUE)
- =PPVDD_SRAM_CPU
- =PPVDD_SRAM_SOC 9

BUCK6

52 46 PP3V3_S2R (MAKE_BASE=TRUE)
- =PP3V3_S2R_SWITCH 48
- =PP3V3_S2R_WIFI_PA 44

52 48 PP3V3_SW (MAKE_BASE=TRUE)
- =PP3V3_EDP_PU
- =PP3V3_NAND 12
- =PP3V3_USB_SOC 4

LDO1

52 47 PP3V0_SPARE1 (MAKE_BASE=TRUE) = =PP3V0_SPARE1 49

LDO2

52 47 16 PP1V7_VA_VCP (MAKE_BASE=TRUE) = =PP1V7_VA_VCP 15 16

LDO3

LDO3 SHOULD BE ON IN HIBERNATE
COMPASS, ACCEL, GYRO, PROX ARE ON OSCAR
HALL EFFECT NEEDS TO BE ON IN HIBERNATE

52 47 PP3V0_S2R_SENSOR (MAKE_BASE=TRUE)
- =PP3V0_S2R_HALL 13
- =PP3V0_S2R_GYRO 21
- =PP3V0_S2R_ACCEL 21
- =PP3V0_S2R_COMP 21

LDO4

52 47 PP3V0_ALS (MAKE_BASE=TRUE)
- =PP3V0_ALS 20
- =PP3V0_PROX 22
- =PP3V0_HP_ALS
- =PP3V0_IO_ALS

SHOULD IO ALS POWER HERE?

LDO5

52 47 PP3V0_UVLO (MAKE_BASE=TRUE) = =PP3V0_UVLO 49

LDO6

52 47 PP3V3_ACC (MAKE_BASE=TRUE) = =PP3V3_ACC 11

LDO7

LDO7 SHOULD BE ON IN HIBERNATE

52 47 PP3V0_S2R_TRISTAR (MAKE_BASE=TRUE) = =PP3V0_S2R_TRISTAR 11

LDO8

47 NC_LDO8 (MAKE_BASE=TRUE) NO_TEST=TRUE = =NC_LDO8

LDO9

BACKUP RAIL. CAN BE BOOSTED TO MEET
1.1V MIN ON CAMERA IF NEEDED.

52 47 PP1V3_CAM (MAKE_BASE=TRUE)
- =PP1V3_CAM_FRONT
- =PP1V3_CAM_REAR 23

LDO10

52 47 PP1V0_SOC (MAKE_BASE=TRUE)
- =PP1V0_USB_SOC 4
- =PP1V0_MIPI_SOC 7
- =PP1V0_EDP_PAD_DVDD_SOC 7

LDO011

52 47 PP2V6_CAM_AF (MAKE_BASE=TRUE) = =PP2V6_CAM_REAR_AF 23

LDO013

52 47 PP2V9_CAM (MAKE_BASE=TRUE)
- =PP2V9_CAM_FRONT 20
- =PP2V9_CAM_REAR 23

VLCM1

47 PP5V25_GRAPE (MAKE_BASE=TRUE) = =PP5V25_GRAPE 13

CHARGER MAIN

52 49 48 47 46 PPVCC_MAIN (MAKE_BASE=TRUE)
- =PPVCC_MAIN_AUDIO 15 16
- =PPVCC_MAIN_LED 47
- =PPVCC_MAIN_DOCK 43
- =PPVCC_MAIN_DEV
- =PPVCC_MAIN_CPU 46
- =PPVCC_MAIN_GPU 46
- =PPVCC_MAIN_SOC 46
- =PPVCC_MAIN_GRAPE 13
- =PPVCC_MAIN_LCD 18
- =PPVCC_MAIN_NAVAJO
- =PPVCC_MAIN_VDD_LCM 47
- =PPVCC_MAIN_WLAN 44
- =PPVCC_MAIN_GPS

BATTERY

52 46 PPBATT_VCC (MAKE_BASE=TRUE)
- =PPBATT_POS_CONN 45
- =PPBATT_VCC_BB 24 25 33 34 35 36 37 38
- =PPBATT_AUDIO

USB POWER INPUT

52 46 PPVBUS_USB_DCIN (MAKE_BASE=TRUE) = =PPVBUS_USB_EMI 43

ON_BUF

52 47 PP1V8_ALWAYS (MAKE_BASE=TRUE) = =PP1V8_ALWAYS 5

BACKLIGHT BOOST

52 47 PPLED_OUT_A (MAKE_BASE=TRUE) = =PPLED_REG_A 18

SYNC_MASTER=J72_MLB_C SYNC_DATE=11/26/2012

PAGE TITLE: POWER: ALIASES

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DRAWING NUMBER: 051-0886 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 121 OF 121
SHEET: 54 OF 54