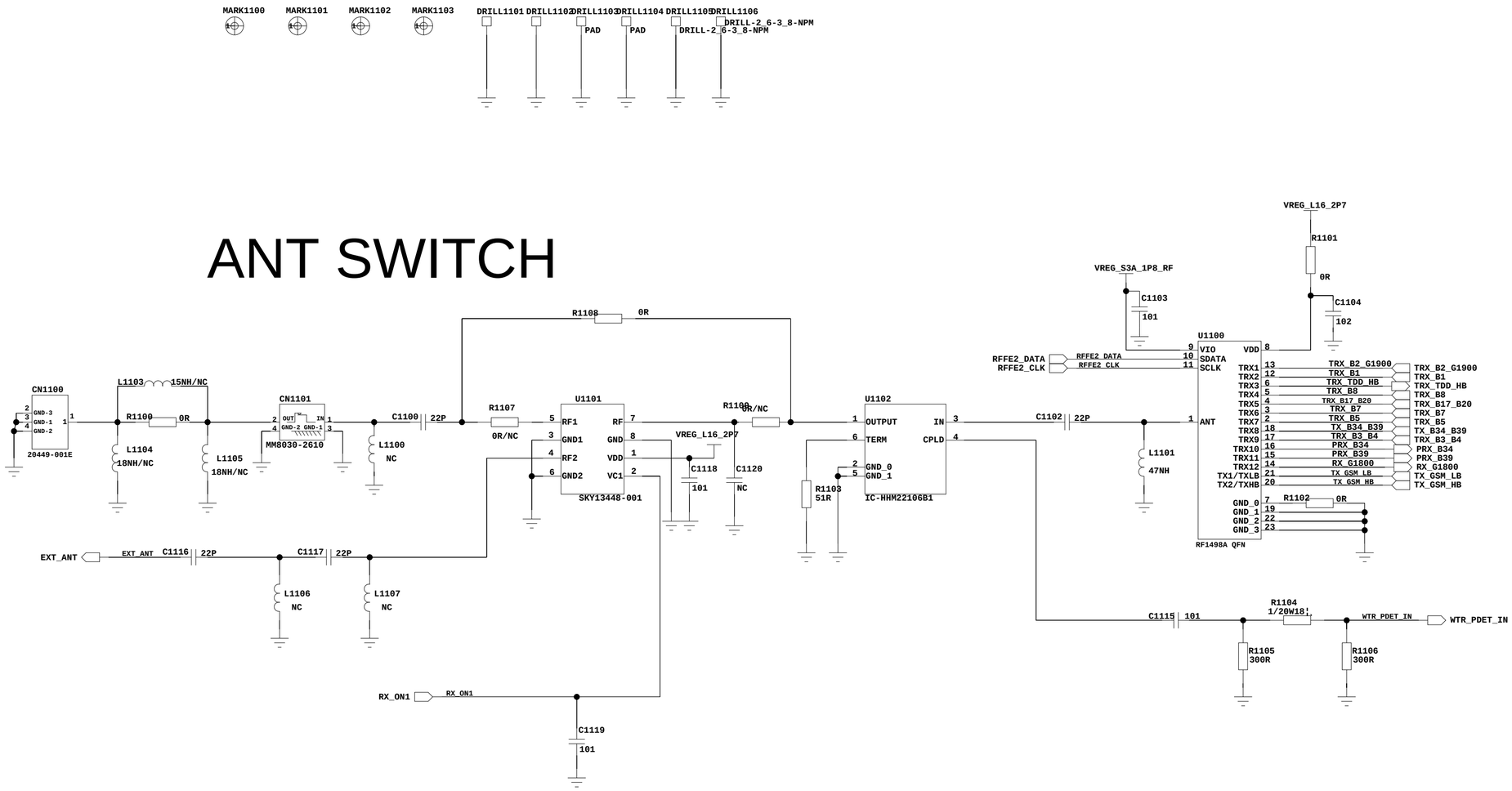

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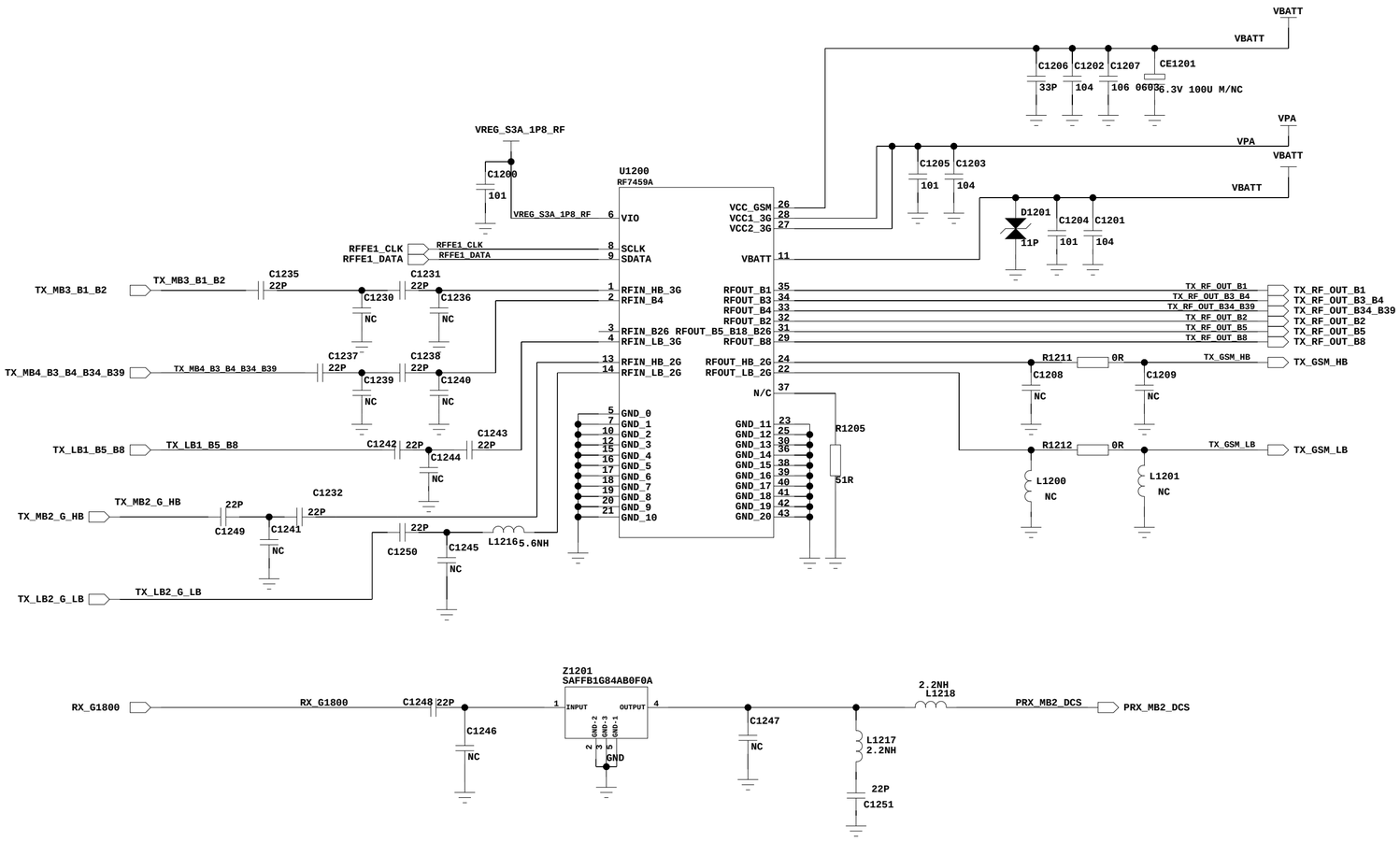
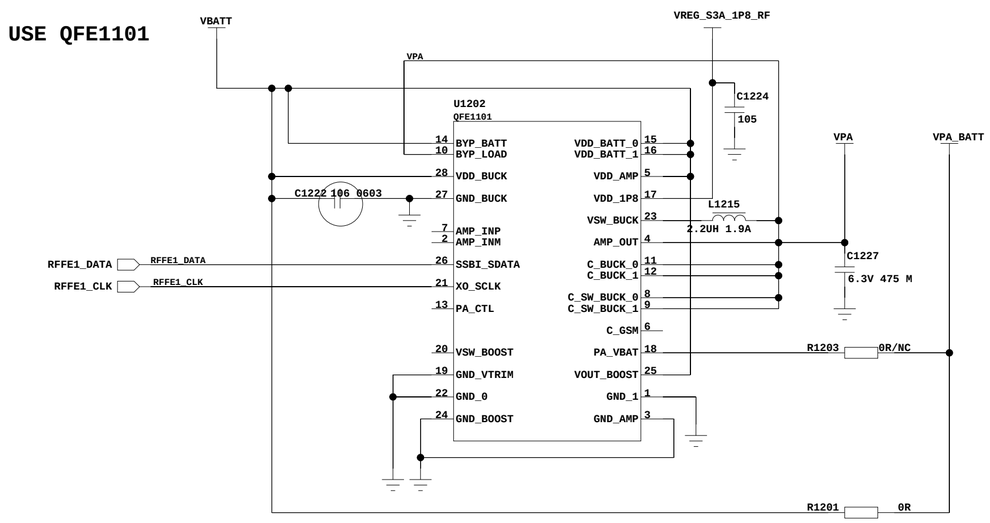
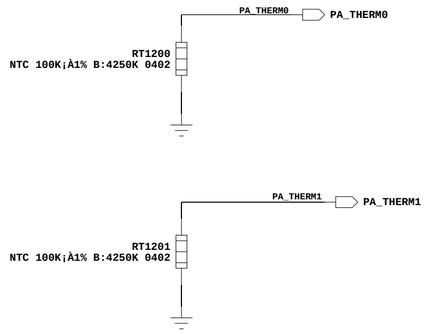
Drawn By			Draw No: Schematic1	
Checked By			Sheet 1_ANT_SWICTH of 20	Ver:
Standard By				
Approved By				

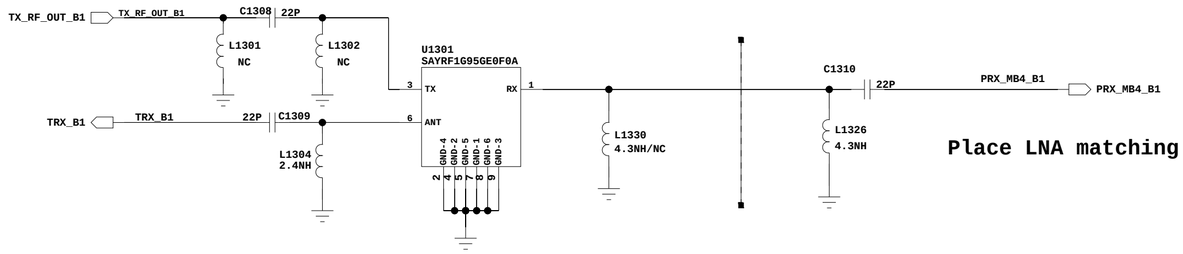






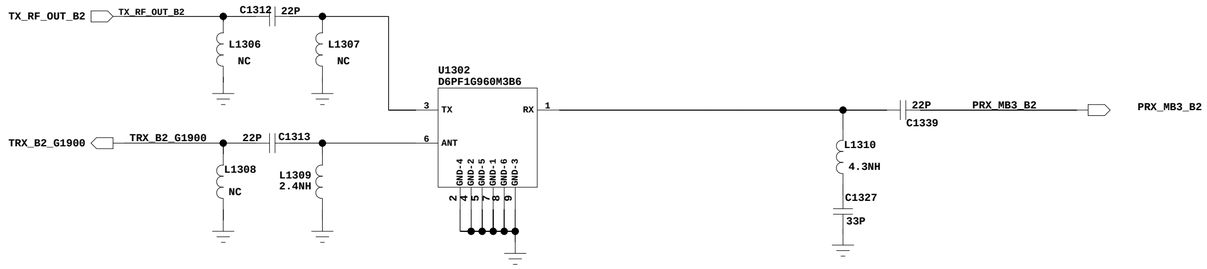
	Sign	Date	Type:	
Drawn By			Draw No: 213007-SA	
Checked By			Sheet 2_GSM_TX_POWER of 2	Ver:
Standard By			oppo	
Approved By				

B1 TRX

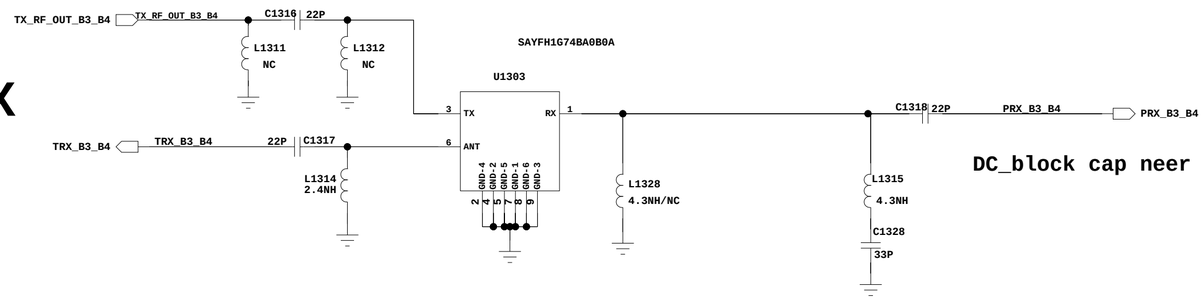


Place LNA matching components close to WTR1625

B2 TRX

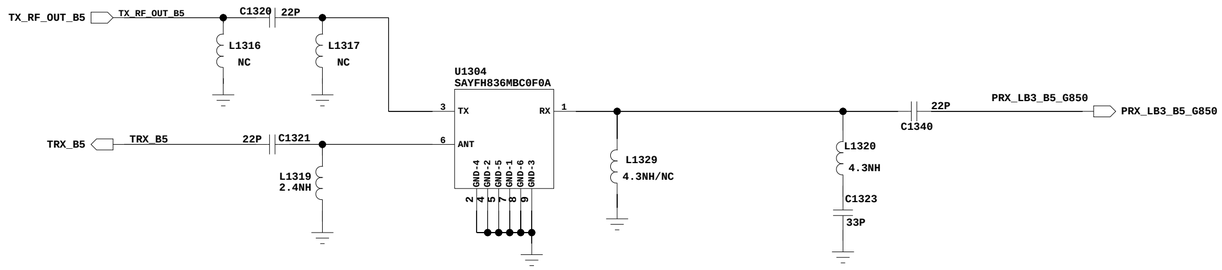


B3/B4 TRX

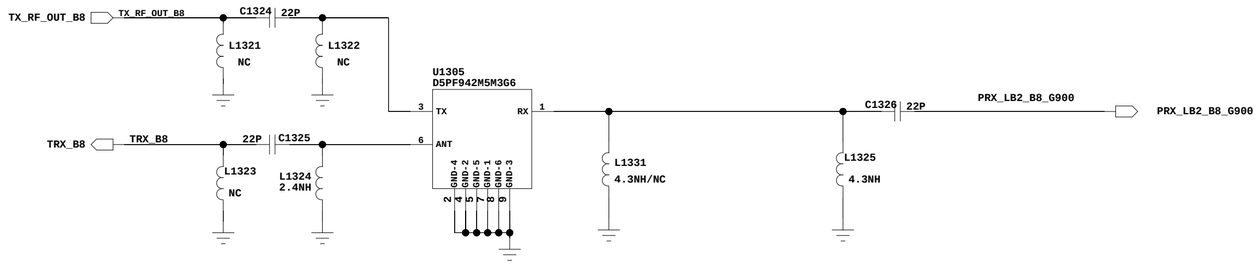


DC_block cap neer in sky13350

B5 TRX



B8 TRX



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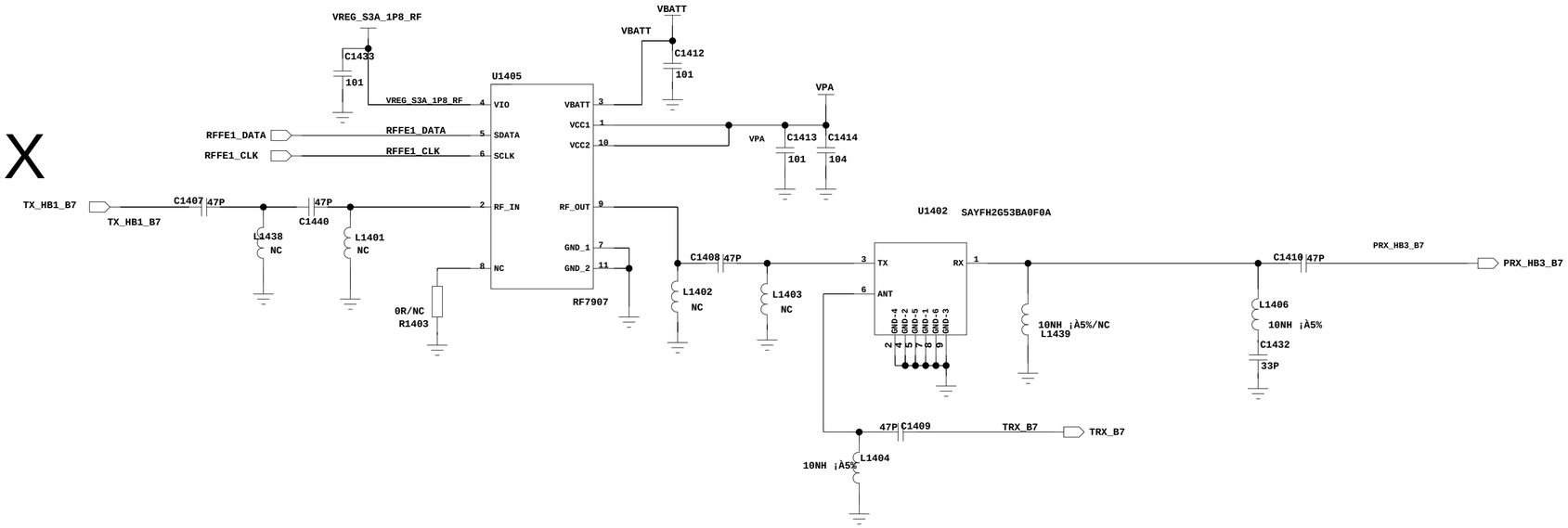
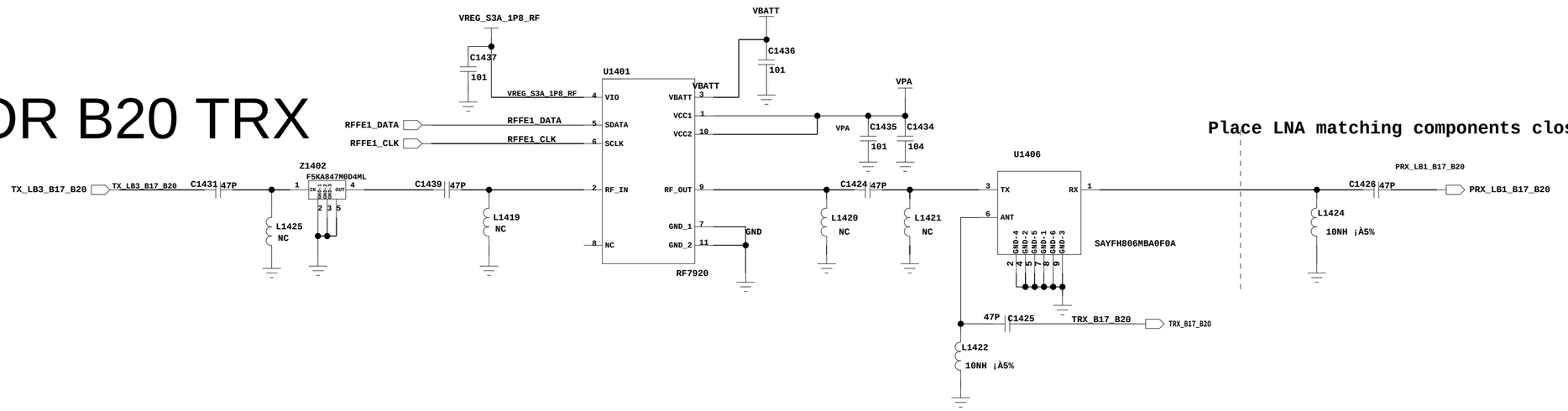
Drawn By			Draw No: 212025-SA	
Checked By			Sheet 8_SIM_JTAG of 23	Ver:
Standard By			oppo	
Approved By				

B7 TRX

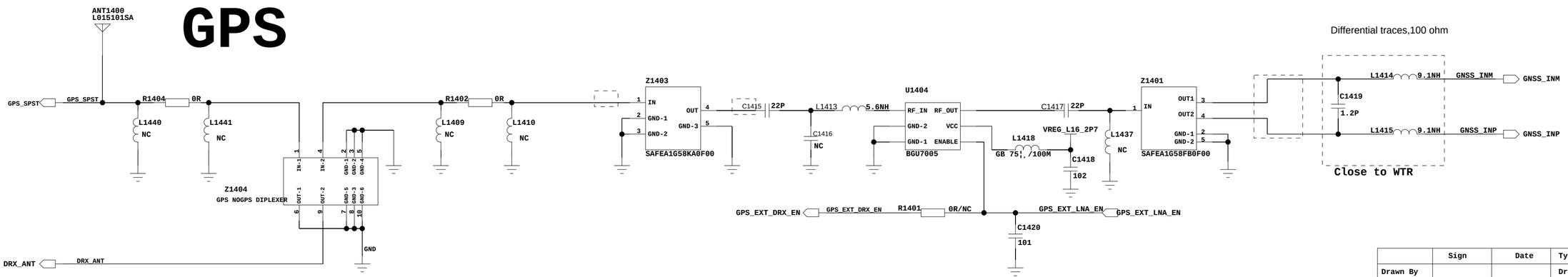


B17 OR B20 TRX



Place LNA matching components close to WTR1625

GPS



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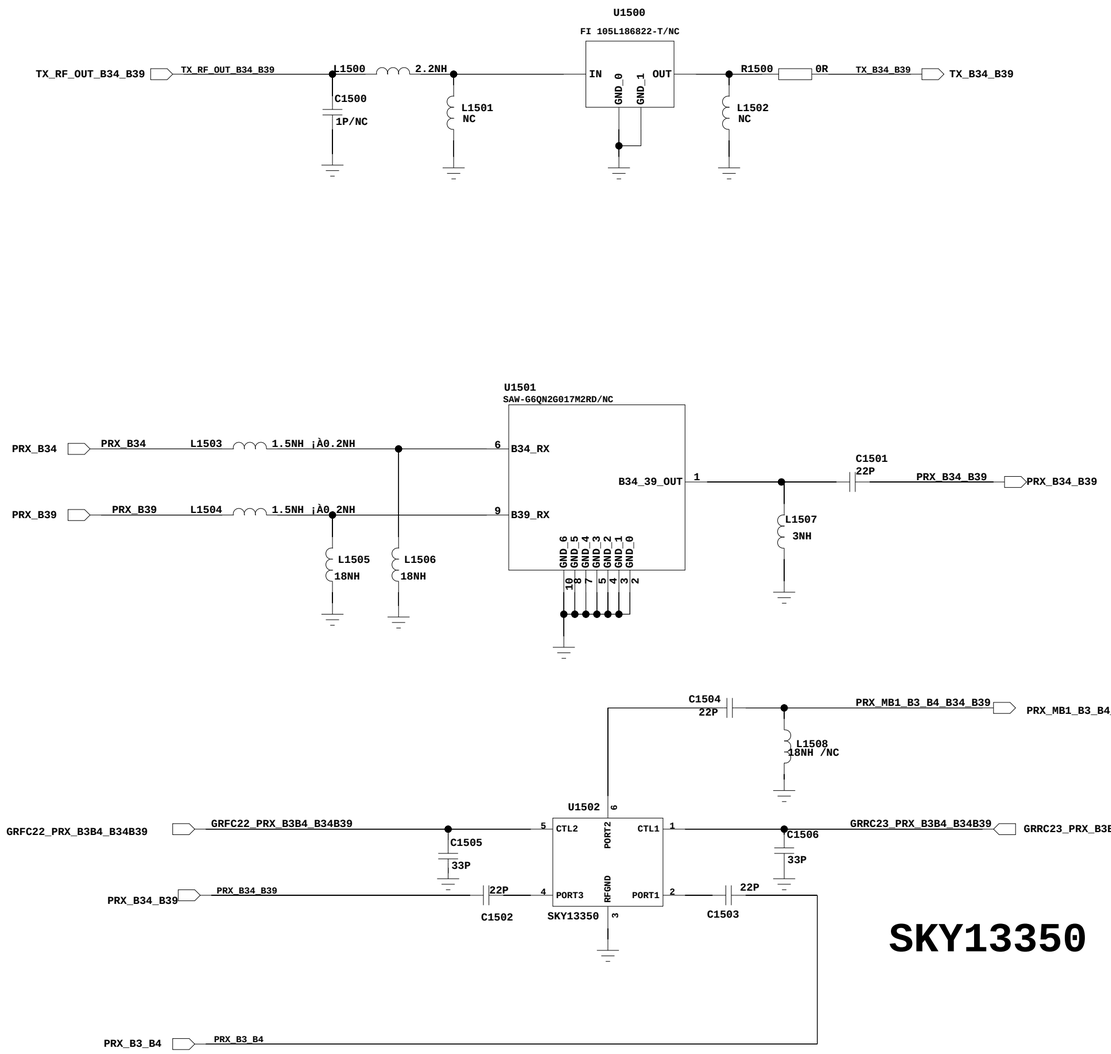
Drawn By			Draw No: Schematic1
Checked By			Sheet of Ver:
Standard By			3_WCDMA_B5_DCDC
Approved By			

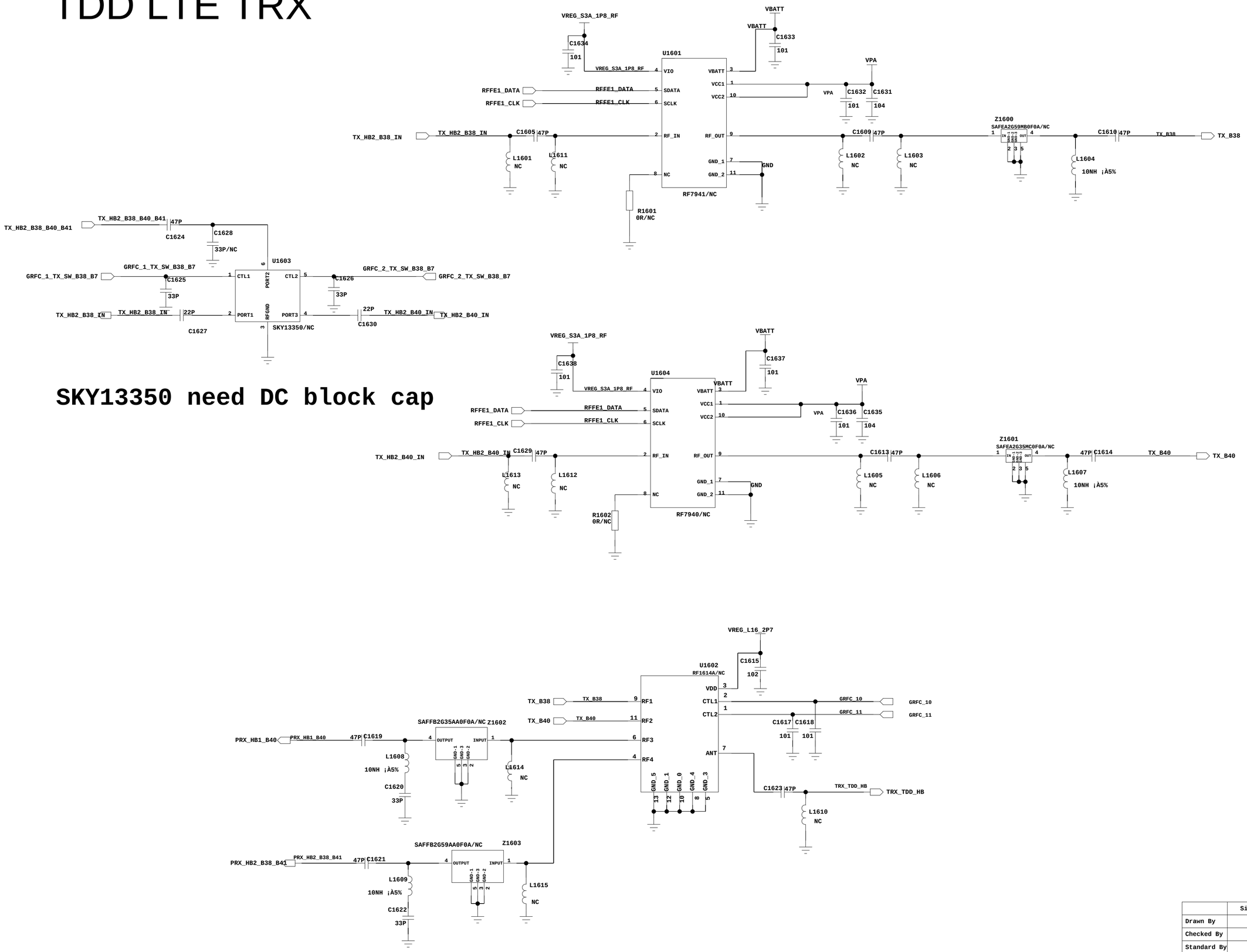


CTL1	CTL2	
1	0	port2 to port1
0	1	port2 to port3

SKY13350 need DC block cap

	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet 6 of 6	Ver:
Standard By			oppo	
Approved By				

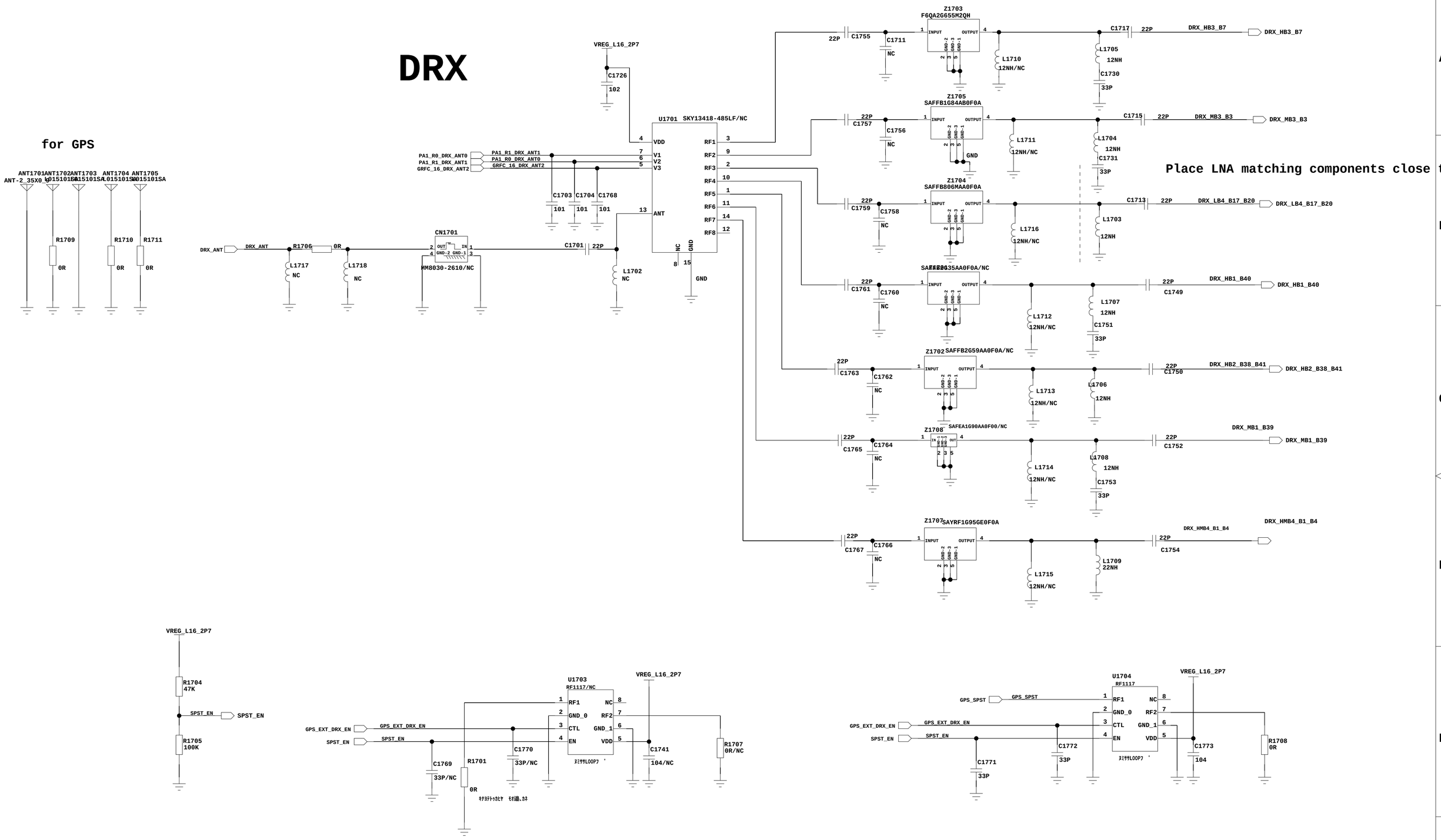
TDD LTE TRX



SKY13350 need DC block cap

	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 30 of 28 Ver:
Standard By			oppo
Approved By			

DRX



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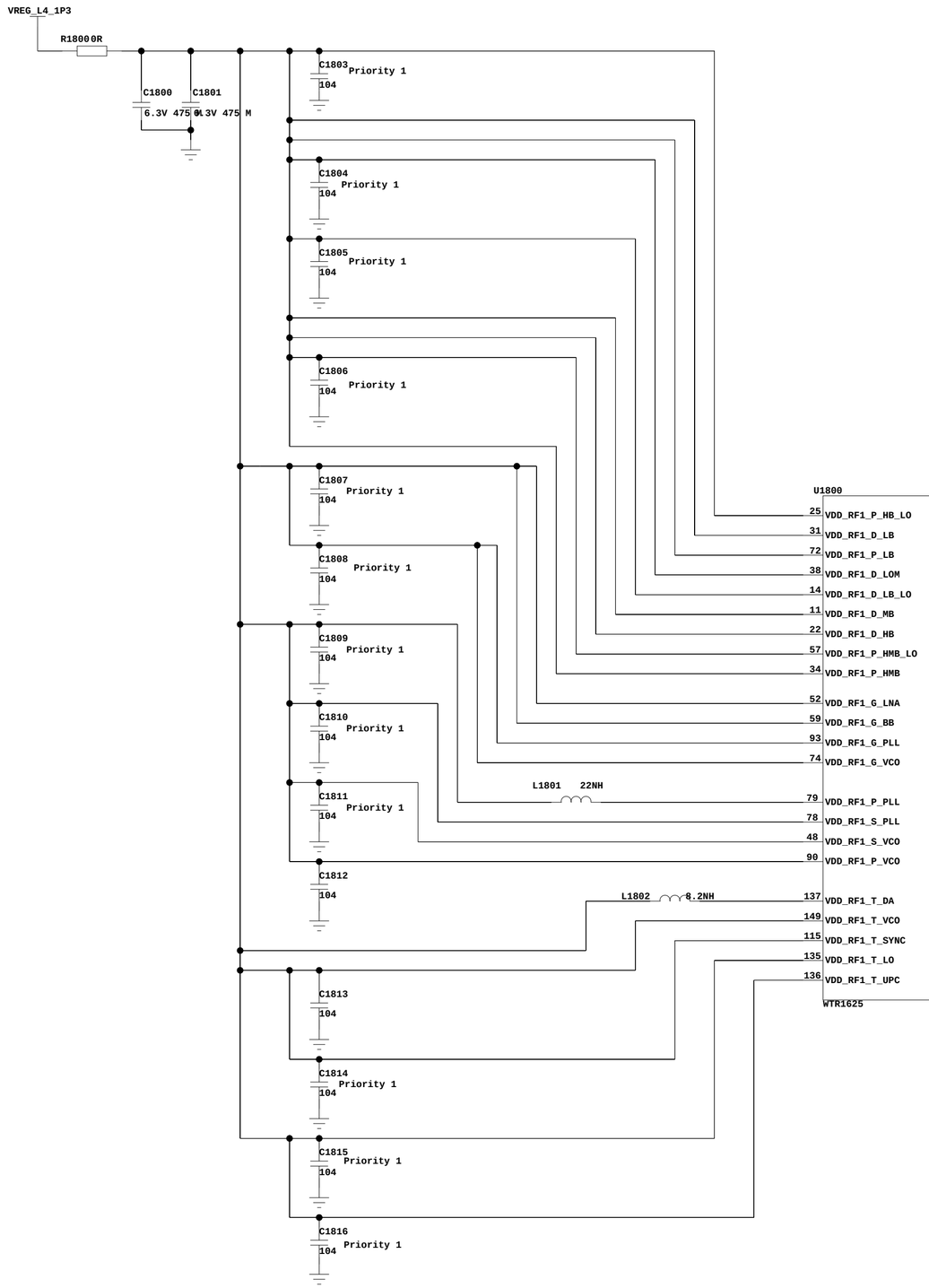
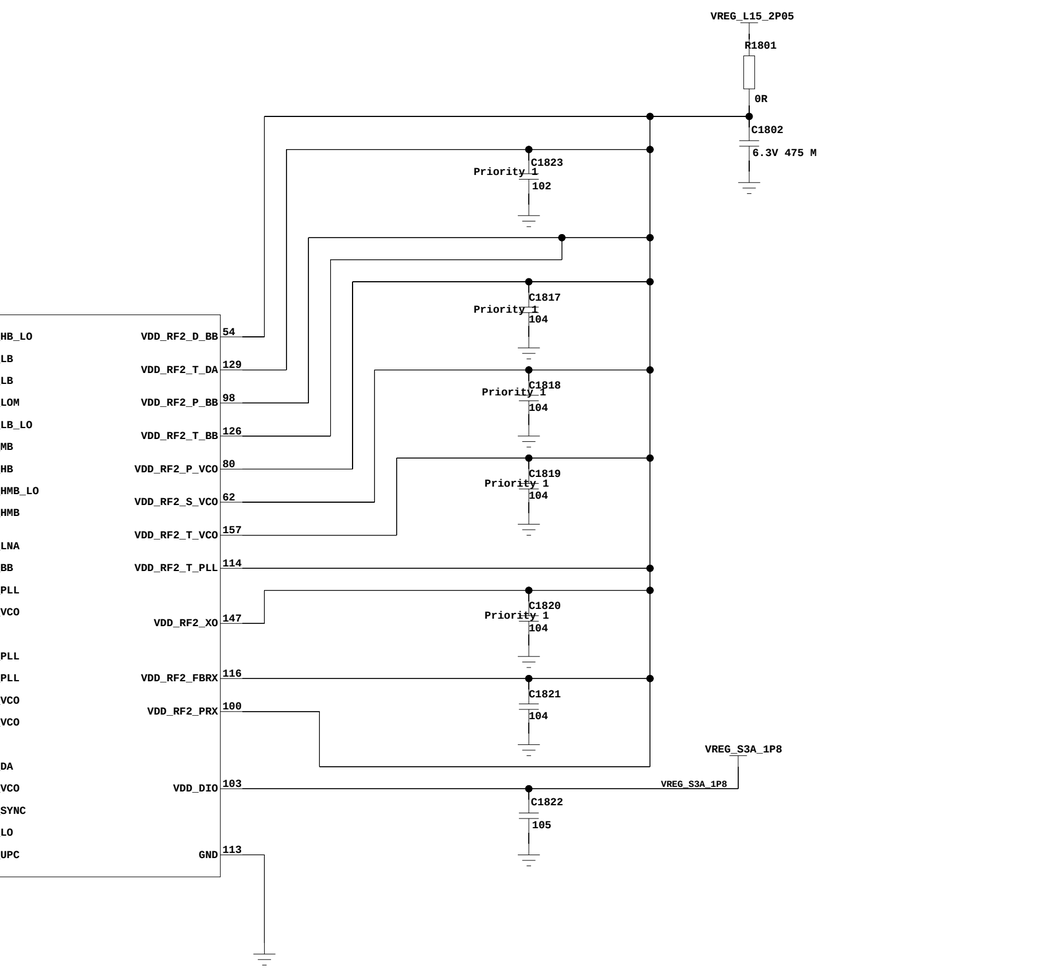
Drawn By			Draw No: Schematic1
Checked By			Sheet 10 of 10 Ver:
Standard By			oppo
Approved By			

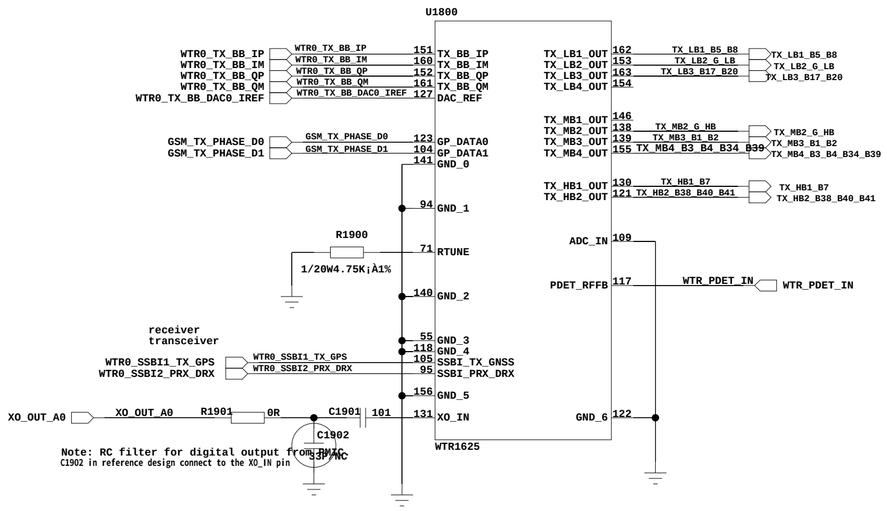
WTR POWER DISTRIBUTION 1.3V

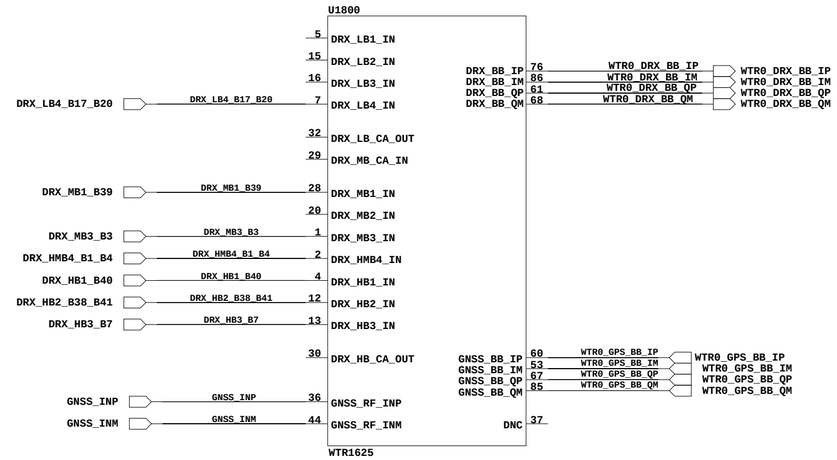


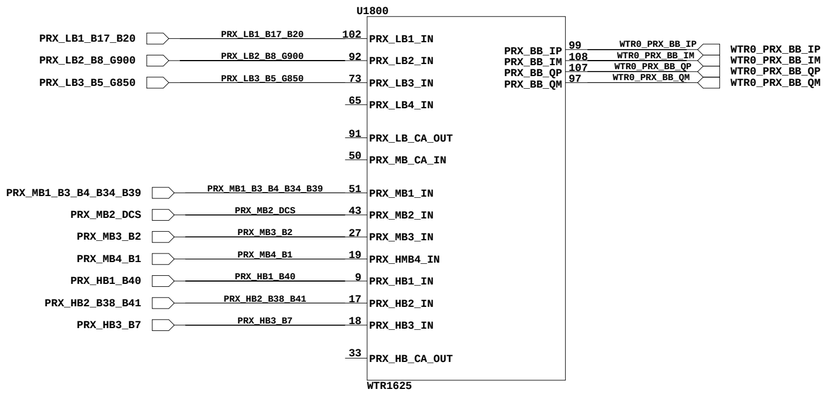
WTR POWER DISTRIBUTION 2.05V(Rev.B)

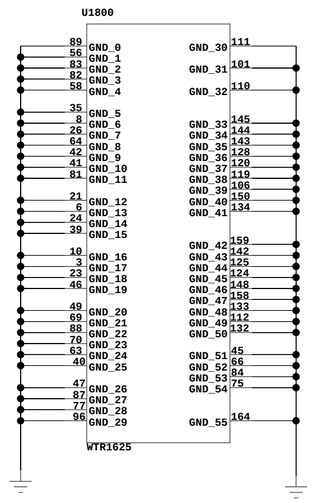


	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet of Ver:
Standard By			6_WTR1605L_POWER
Approved By			oppo



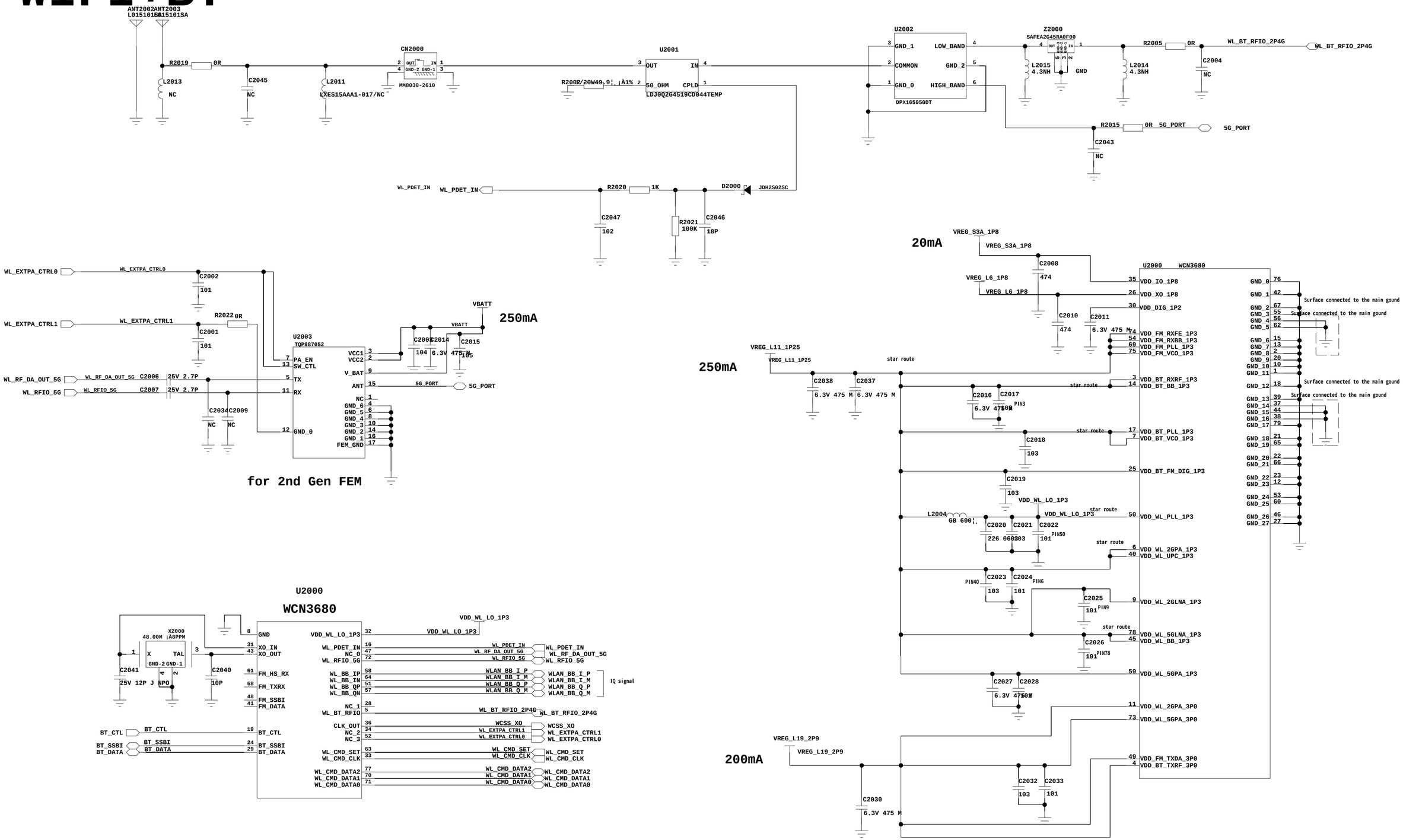






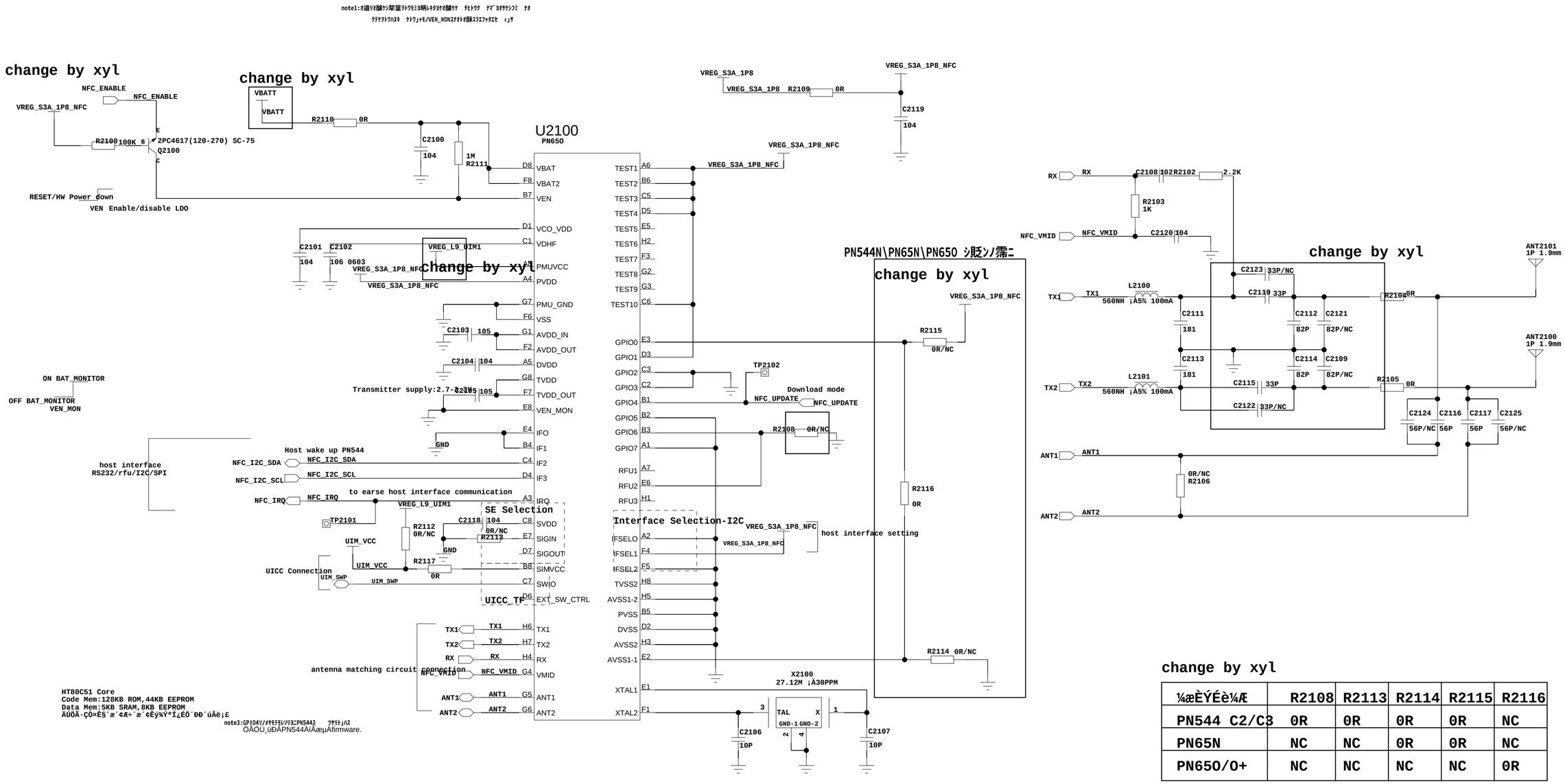
	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet of 7_WTR1605L_RF Ver:
Standard By			oppo
Approved By			

WIFI+BT



If 2.4 GHz WLAN spurs are observed around 2.6 to 2.7 GHz, replace R1612 with 20 nH inductor.

	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 12 of 12 Ver:
Standard By			oppo
Approved By			



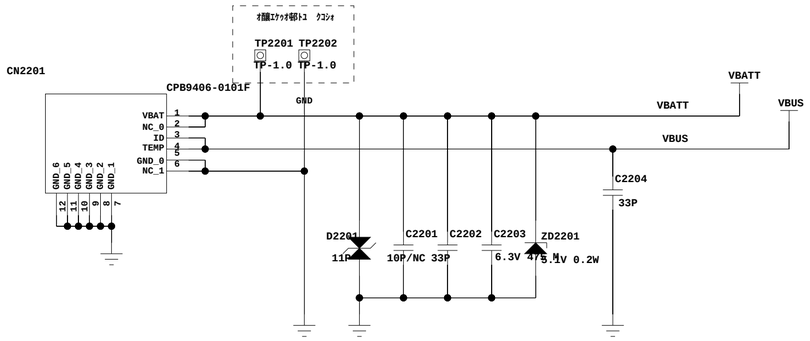
HT80C51 Core
Code Mem:128KB ROM,44KB EEPROM
Data Mem:5KB SRAM,8KB EEPROM
note3:ÔÒÃÒÙ¸üÐÀPN544ÀïÃæµÅfirmware.

change by xyl

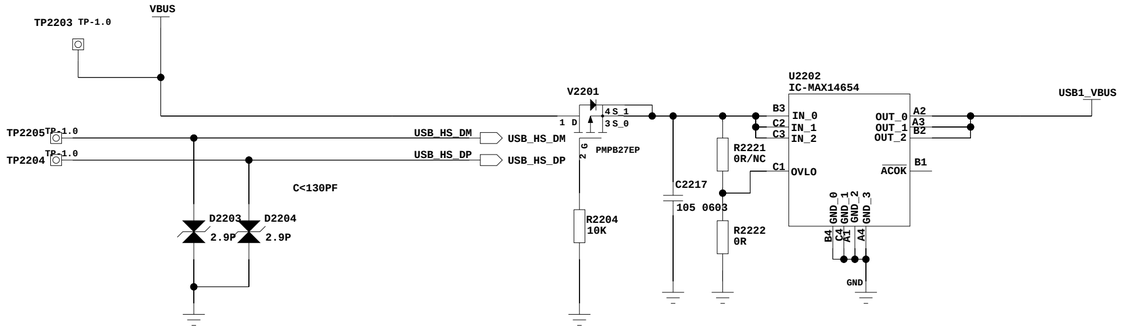
¼æÈÝÉè¼Æ	R2108	R2113	R2114	R2115	R2116
PN544 C2/C3	0R	0R	0R	0R	NC
PN65N	NC	NC	0R	0R	NC
PN65O/O+	NC	NC	NC	NC	0R

	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 11 of 11 Ver:
Standard By			oppo
Approved By			

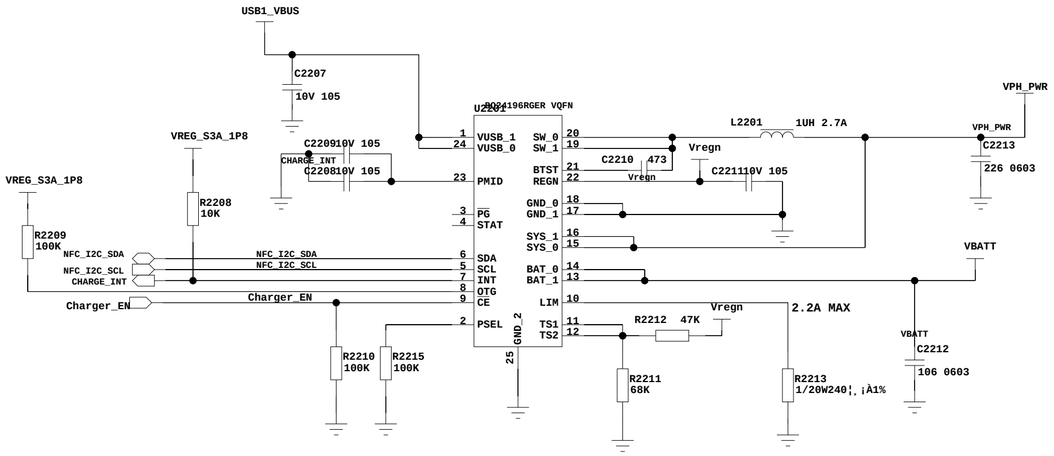
Battery Connector

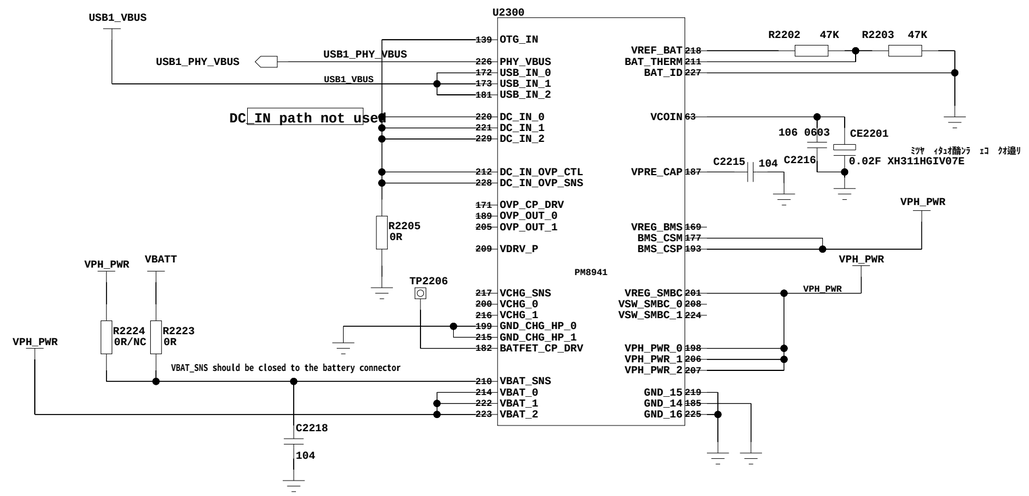


USB OVP



Circuit of Charge



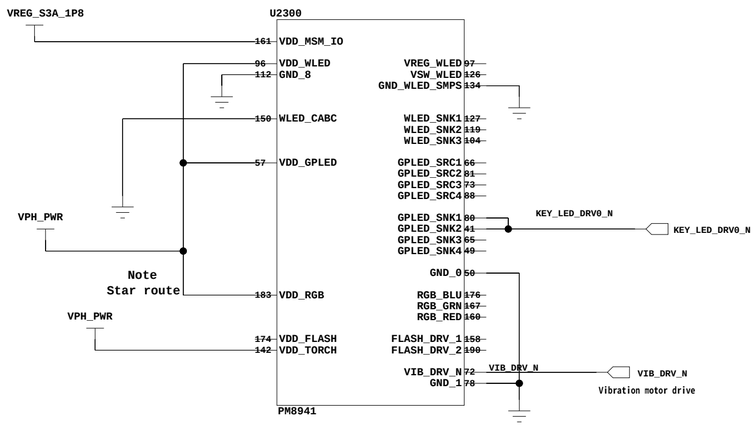


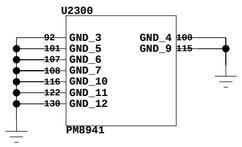
NOTE 1

C2216 of 10uF is required on VCOIN pin to support SMPL upto 2sec.
Connect pin 185 of PM8941 to GND directly using a dedicated via

	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet 20 of 20	Ver:
Standard By			oppo	
Approved By				

PM8941 LED AND GROUND

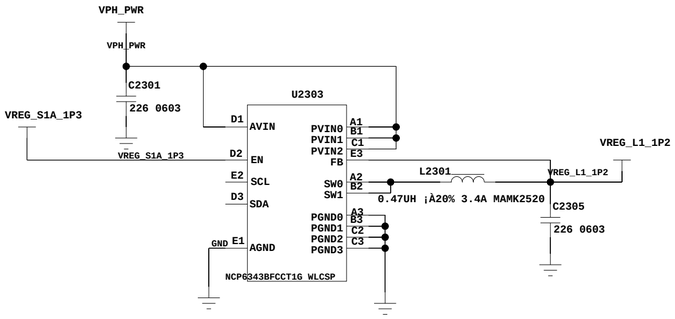




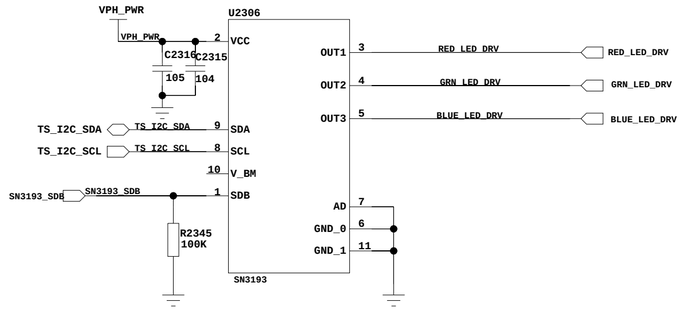
BHELPER

NOTE:Bhelper LDO aids S2A to provide current to the load in this scenario.

LDO1 helper 才酊キ



RGB LED DRIVER



	Sign	Date	Type:	
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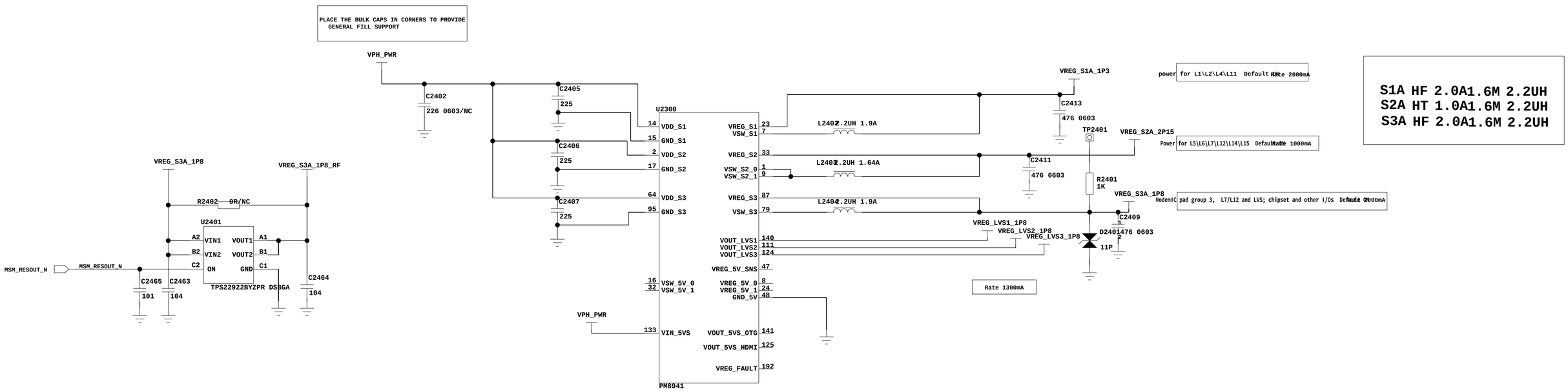
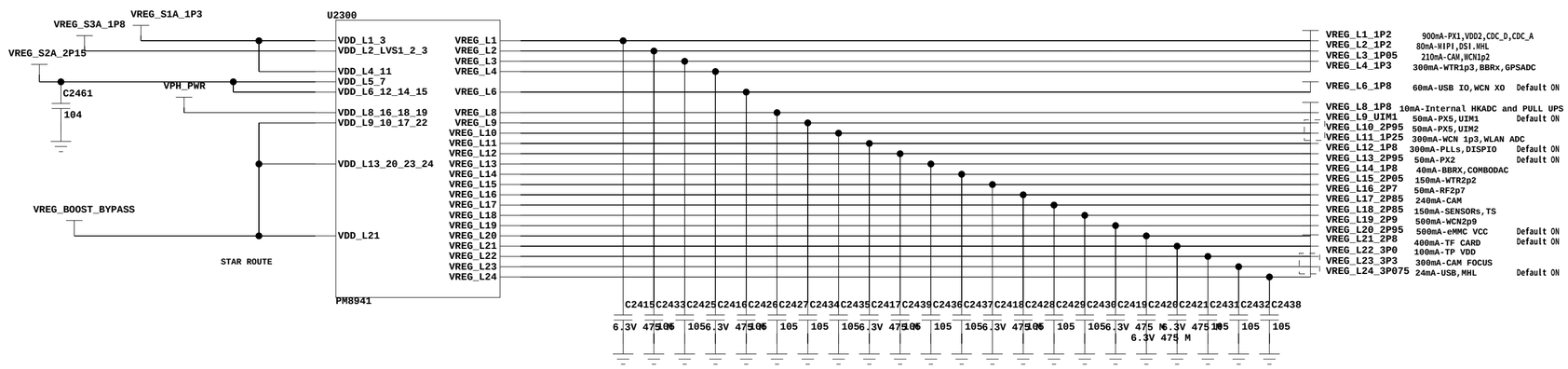
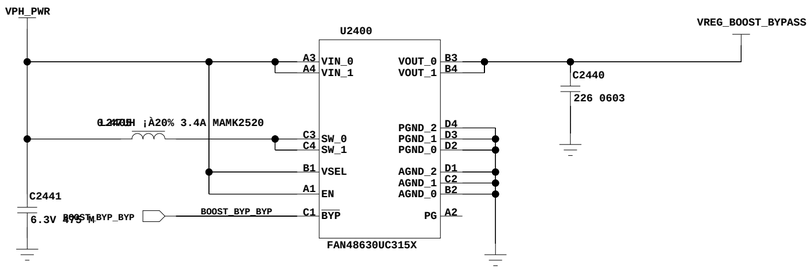
Checked By			Sheet 7 of 7	Ver:
Standard By			oppo	
Approved By				





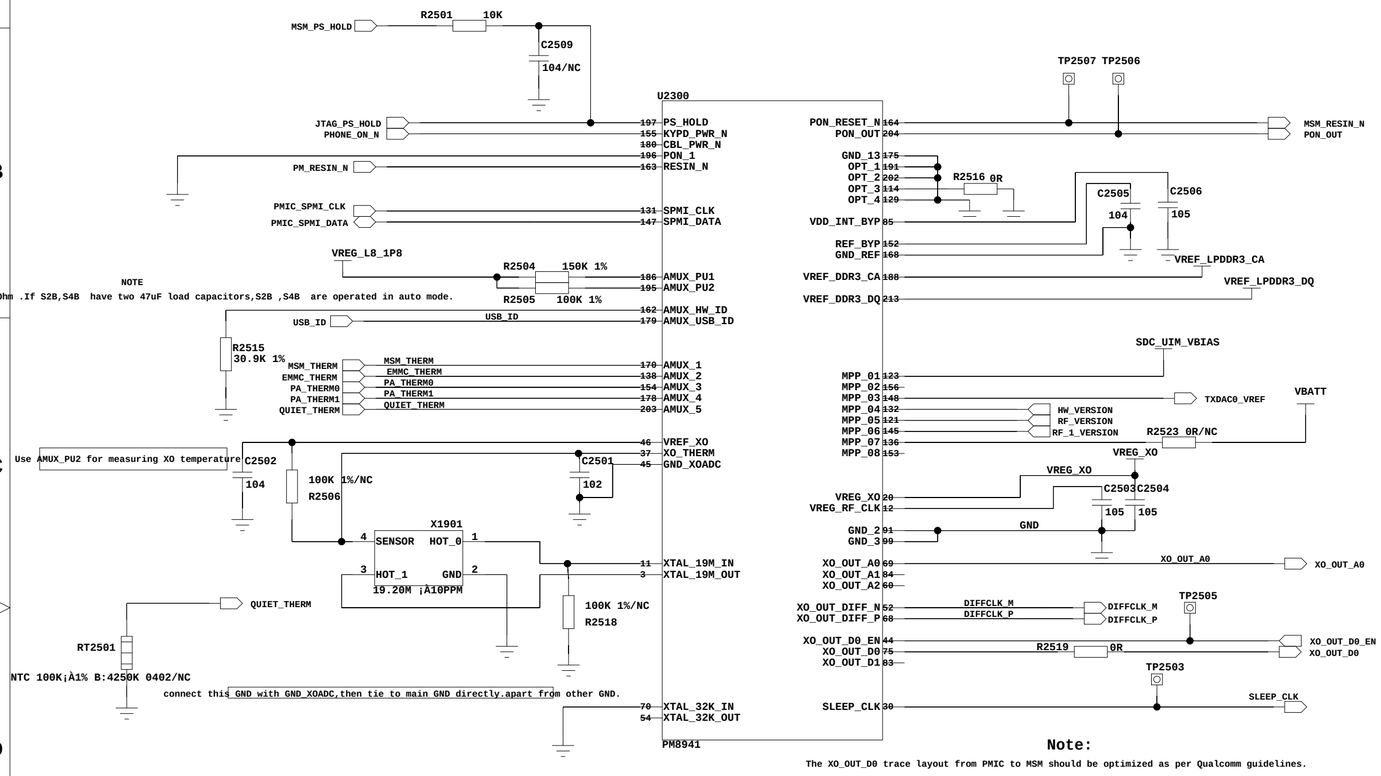


NOTE:BOOST/BYPASS is required for reliable operation of high voltage LDOs at high battery curren

EN	BYP_N	VSEL	VOUT
0	X	X	Boost bypass disabled
1	1	0	For VIN < 3.15V,Vout=3.15V(boost mode) For Vin >=3.15V,Vout=VIN (bypass mode)
1	1	1	For Vin<3.3V,Vout=3.3V(boost mode) For Vin>=3.3V,Vout=Vin(bypass mode)
1	0	X	Vout=Vin (forced bypass mode)

	Sign	Date	Type:
Drawn By			Draw No: 213007-SA
Checked By			Sheet of Ver
Standard By			14_PM8941LDOS1MPS
Approved By			oppo

PM8941 : AMUX, CLK AND MPPS

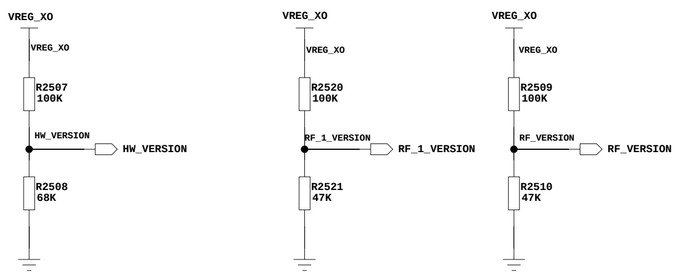


Note:

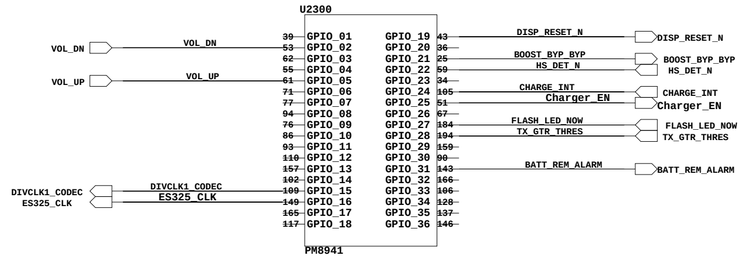
The XO_OUT_D0 trace layout from PMIC to MSM should be optimized as per Qualcomm guidelines.

HW_VERSION

	EVB	EVT	DVT
ﾉﾏﾀｭｵ釋 R2507	100K	100K	100K
ﾏﾂﾀｭｵ釋 R2508	47K	100K	200K
ｷﾖﾑｹﾖｵ	0.576V	0.9V	1.2V



PM8941 : GPIOS



reset circuit

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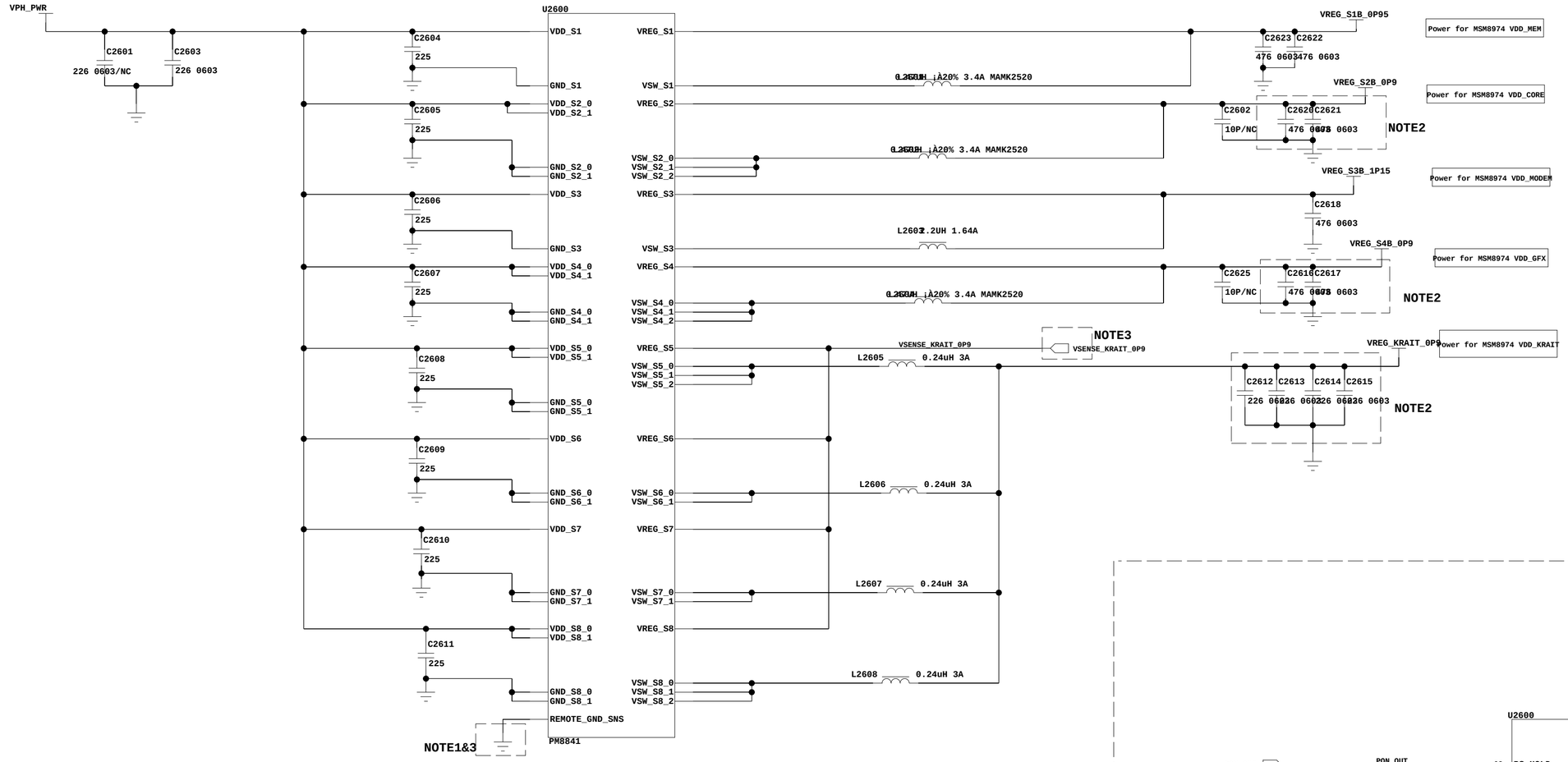
	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 15 of 15 Ver:
Standard By			oppo
Approved By			

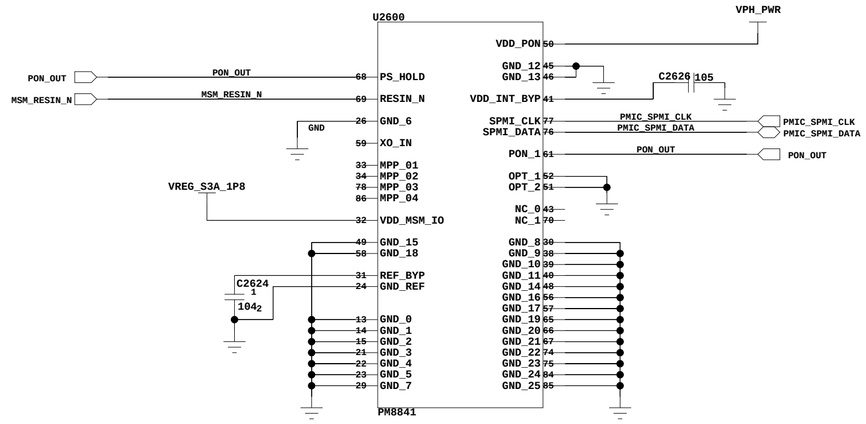


S1B	HF	2.0A	4.8M	0.47UH
S2B	FT	3.0A	3.2M	0.47UH
S3B	HF	1.0A	1.6M	2.2UH
S4B	FT	3.0A	3.2M	0.47UH
S5B¡ªS8B	FT	3.0A	6.4M	0.24UH

NOTE1: connect REMOTE_GND_SNS ground to the gnd near the MSM wihth single trace.

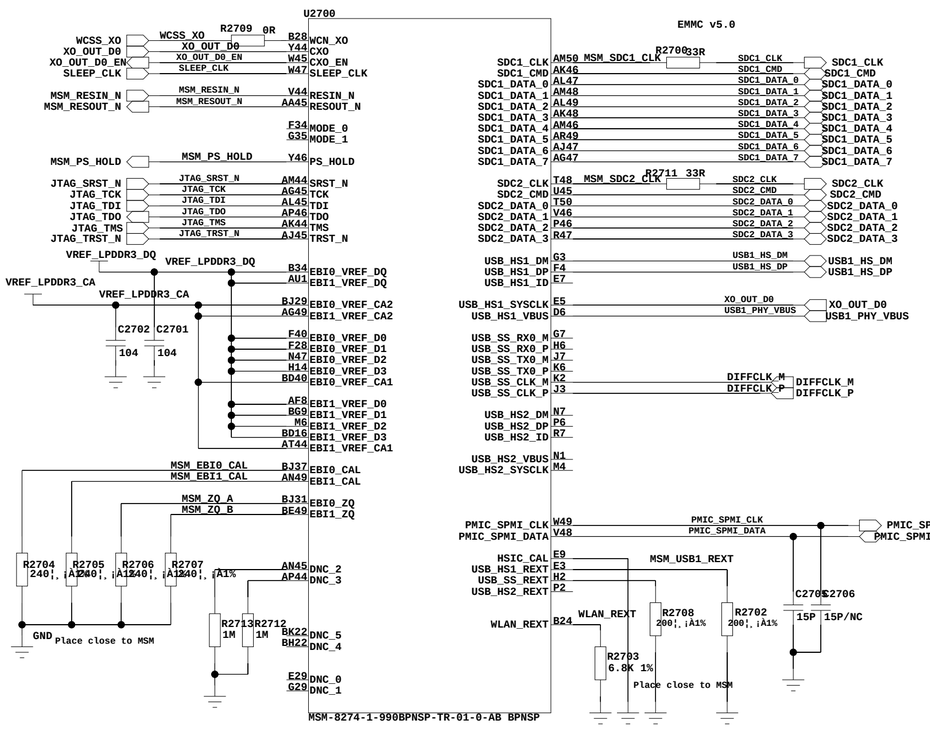
NOTE2: Place S2B,S4B,S5B,S6B,S7B,S8B output capacitors close to MSM

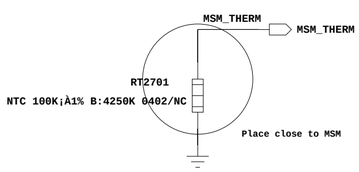
NOTE3: Route VSENSE_KRAIT_0P9 and REMOTE_GND_SNS as a differential.



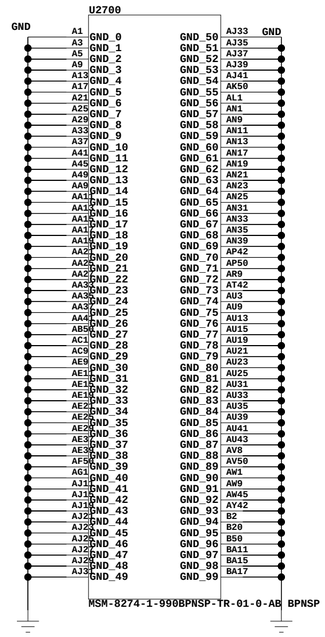
	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet 19 of 19	Ver:
Standard By			oppo	
Approved By				

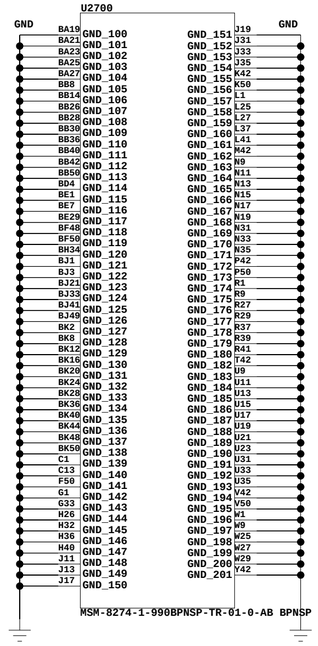
MSM8974 : CONTROL

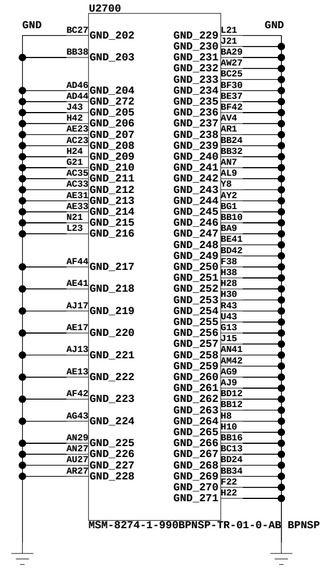


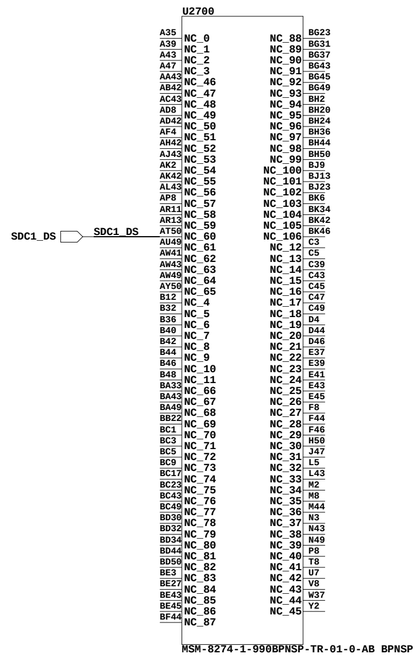


MSM8974 : GND & NC



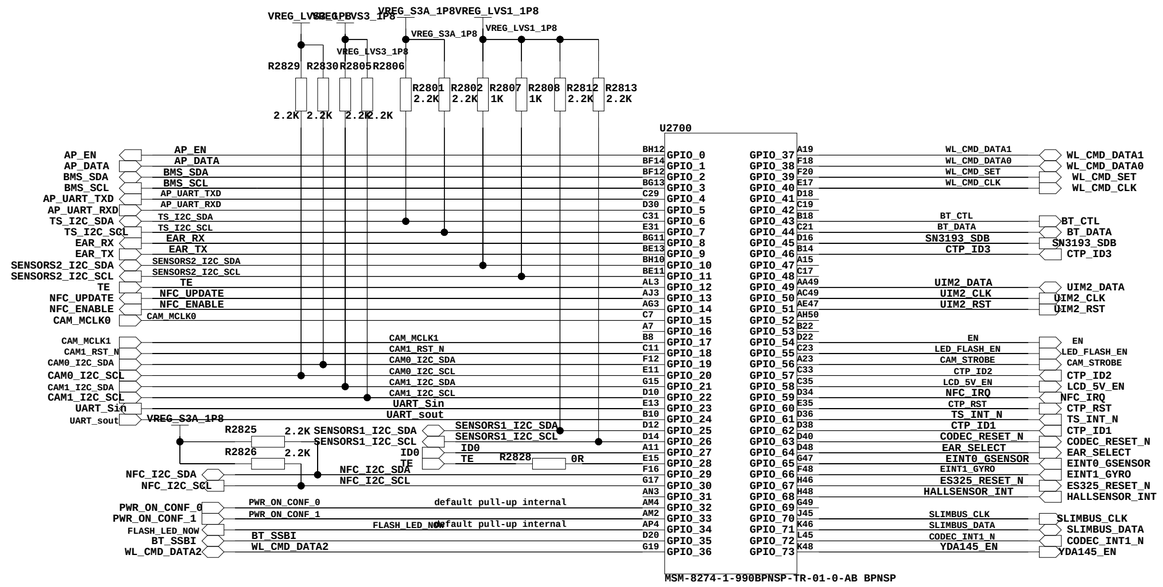


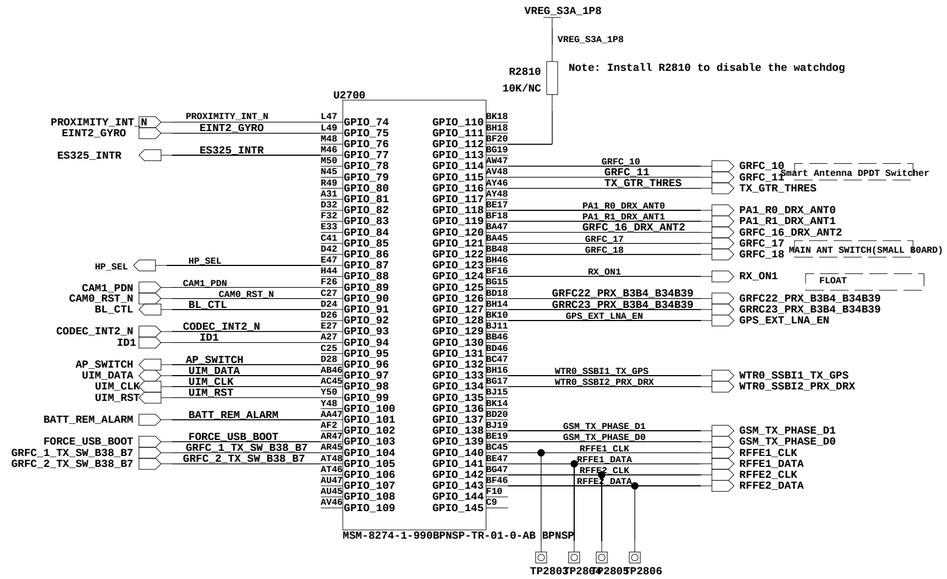




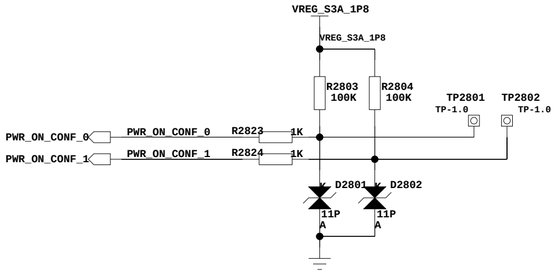
	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 16 of 16 Ver:
Standard By			oppo
Approved By			

MSM8974 : GPIOS





Test Confige



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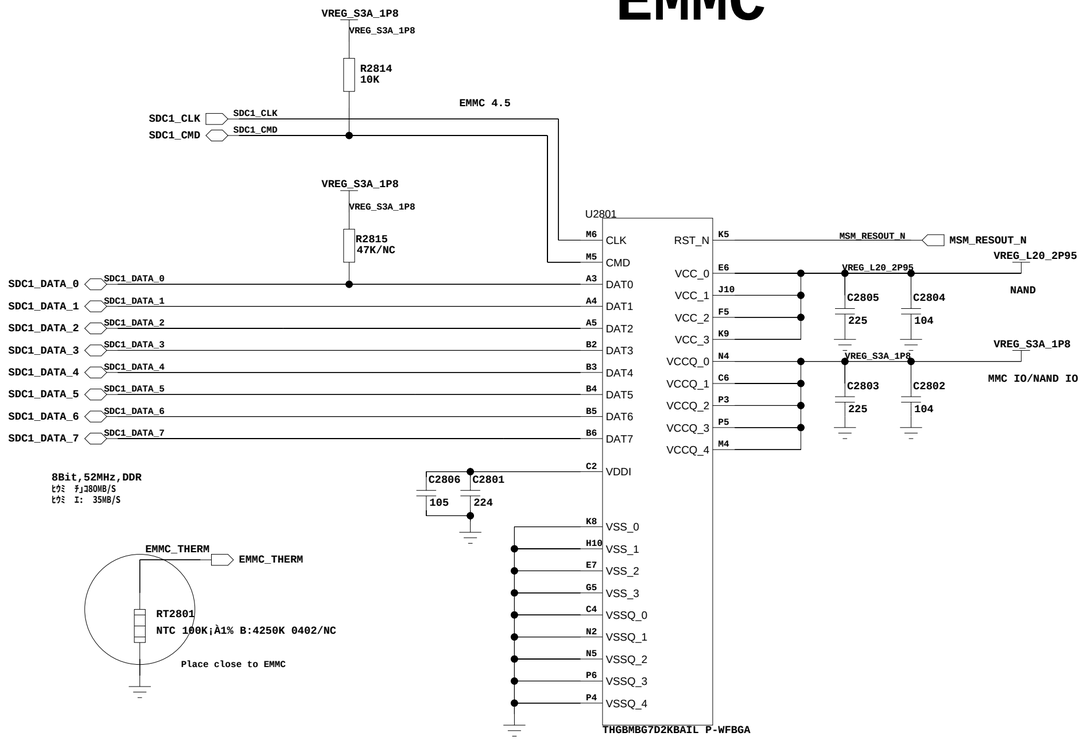
BOOT MODE

CONF_0	CONF_1	Mode
0	0	Factory Mode
0	1	WLAN Final Test
1	0	RF mode
1	1	Ordinary Power On

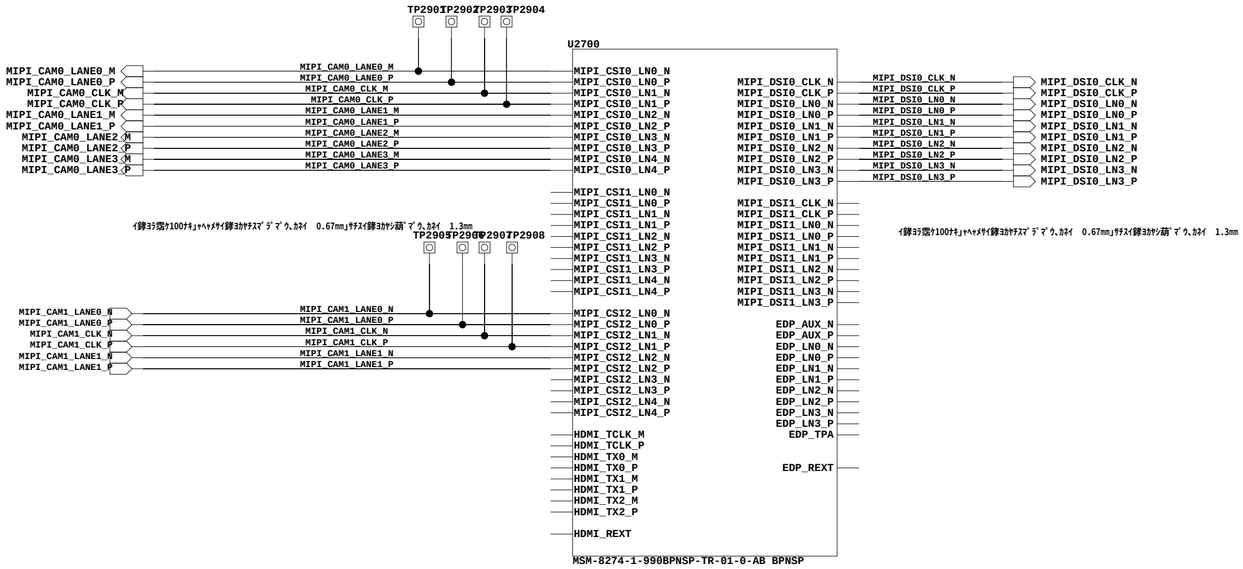
EMMC



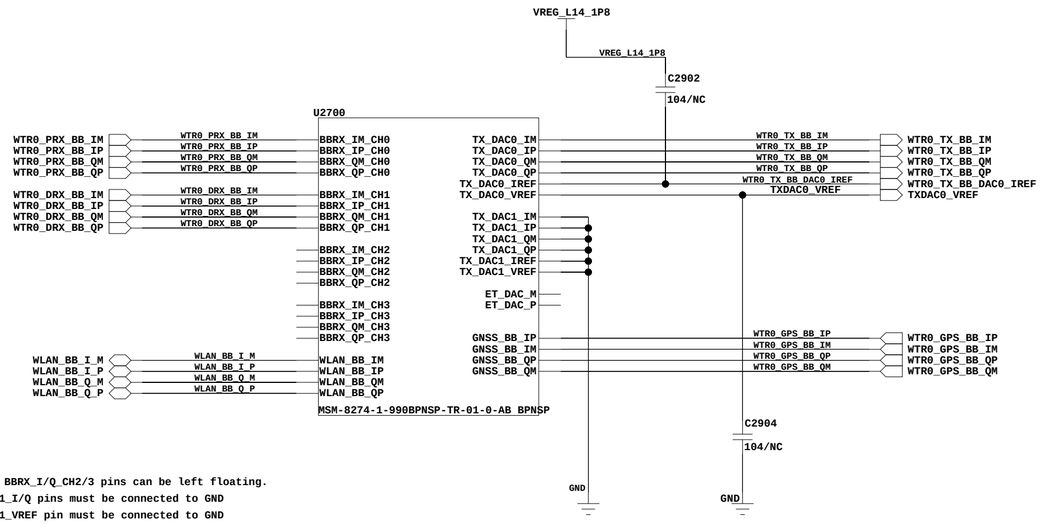
and the chip should has no special requirement on 1.8V/2.95V power on sequence (which is fixed by our pmic, some eMMC has special requirement on it, most has no requirement on it).

	Sign	Date	Type:	
Drawn By			Draw No: 213007-SA	
Checked By			Sheet 1 of 29	Ver:
Standard By			oppo	
Approved By				

MSM8974: MIPI



MSM8974 : RF, GPS AND WLAN

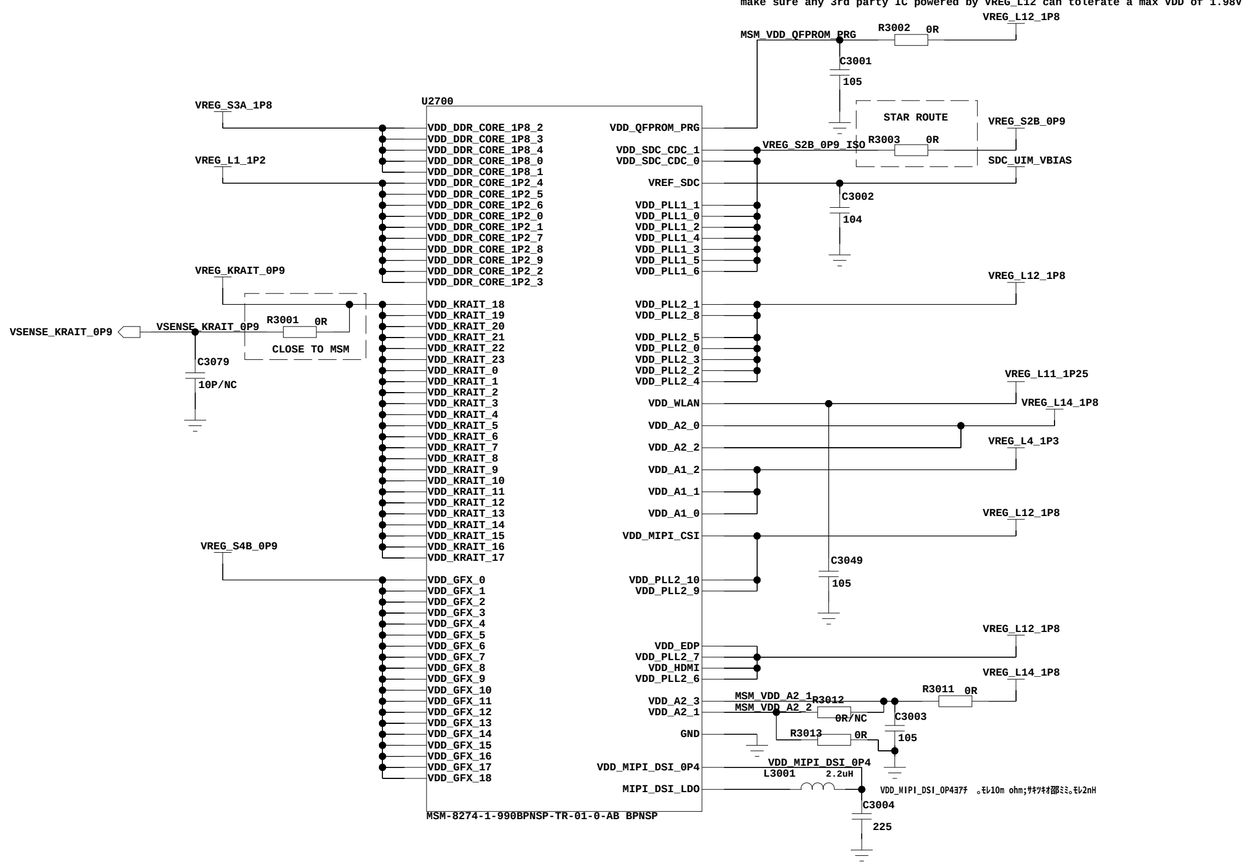


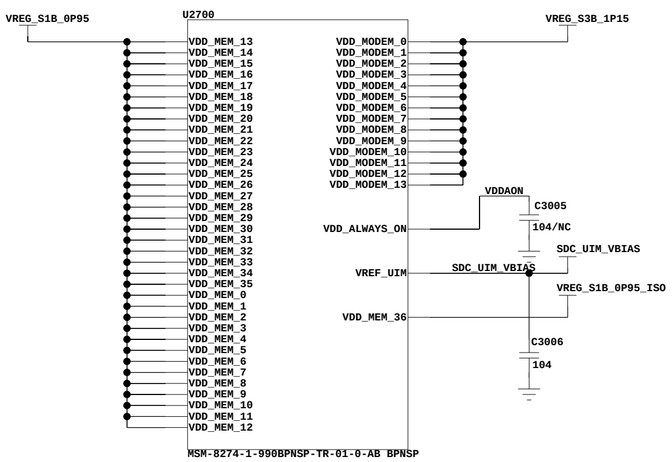
Note: For CSFB - unused BBRX_I/Q_CH2/3 pins can be left floating.
Unused TXDAC1_I/Q pins must be connected to GND
Unused TXDAC1_VREF pin must be connected to GND
TXDAC1_IREF pin must be connected to VREG_L14_1P8.

	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet 18 of 18	Ver:
Standard By			oppo	
Approved By				

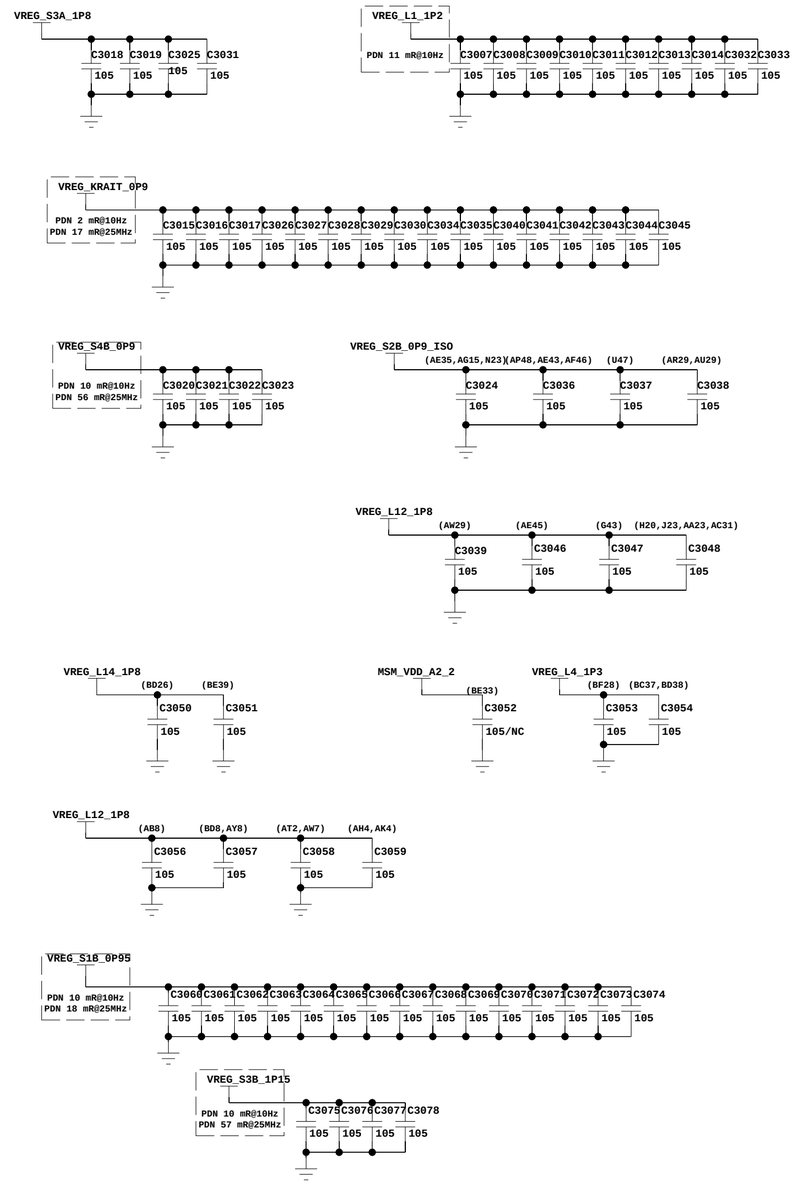
MSM8974 : POWER 1

When blowing fuses,VREG_L12 will be set to 1.9V
make sure any 3rd party IC powered by VREG_L12 can tolerate a max VDD of 1.98V





MSM8974 : DECOUPLING CAPS



	Sign	Date	Type:
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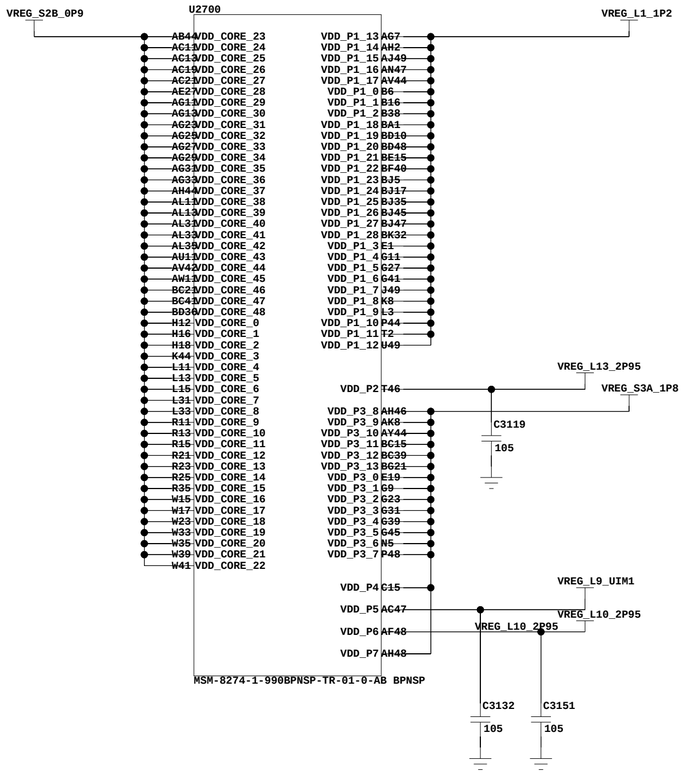
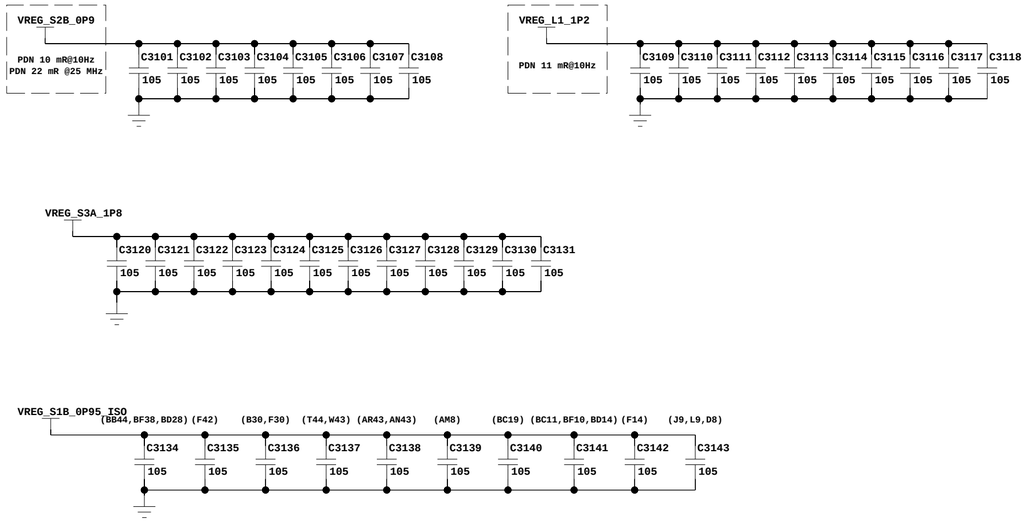
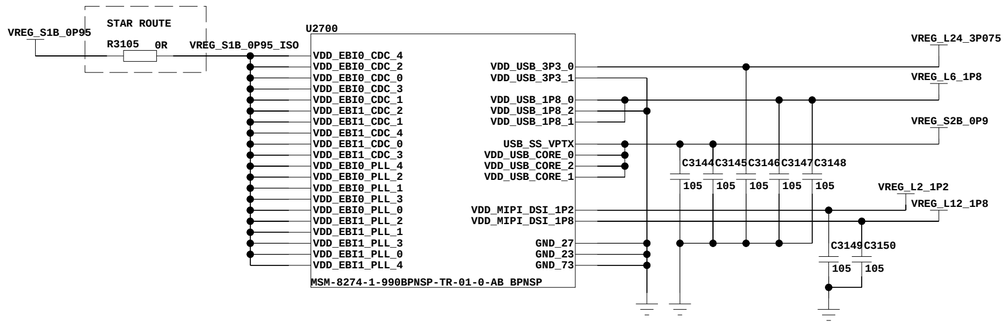
Checked By			Sheet 20_MSM8974_POWER1_DECAPS 19 of 21
Standard By			
Approved By			

MSM8974 : POWER 2



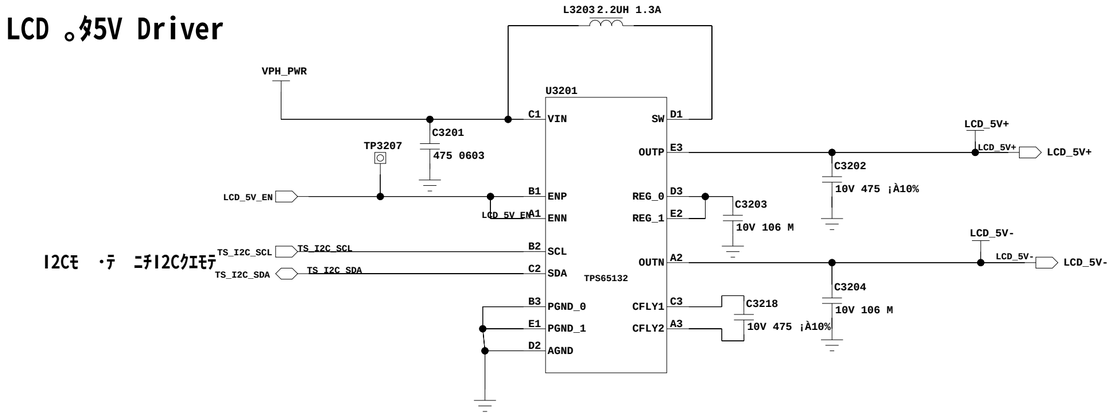
MSM8974 : DECOUPLING CAPS



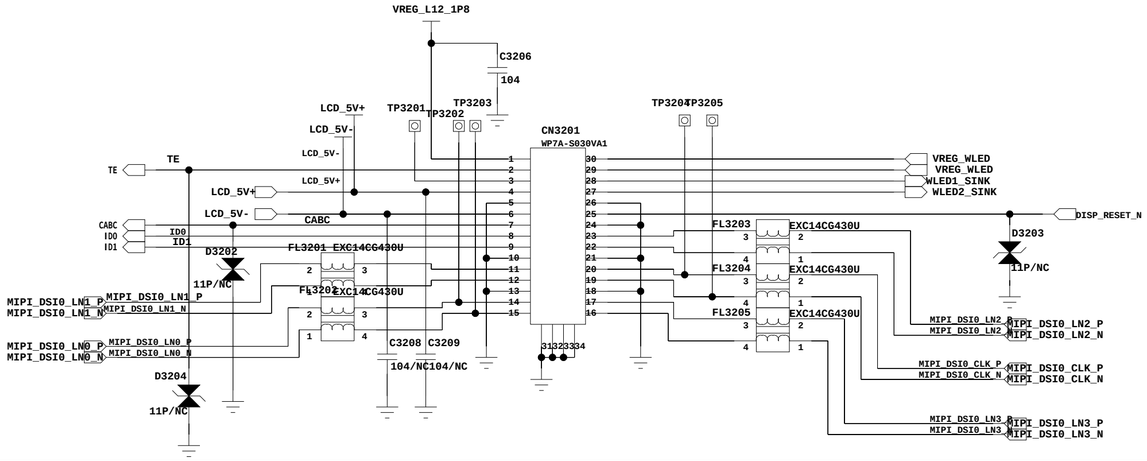


	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet 21 of 21	Ver:
Standard By			oppo	
Approved By				

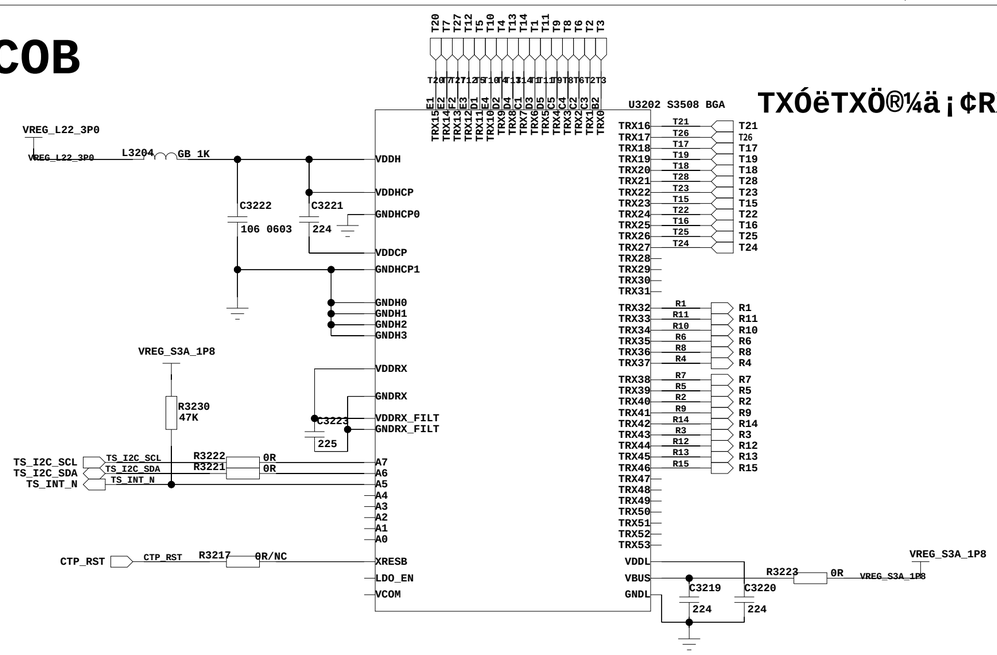
LCD ｡ｸ5V Driver



LCD connector



TP COB



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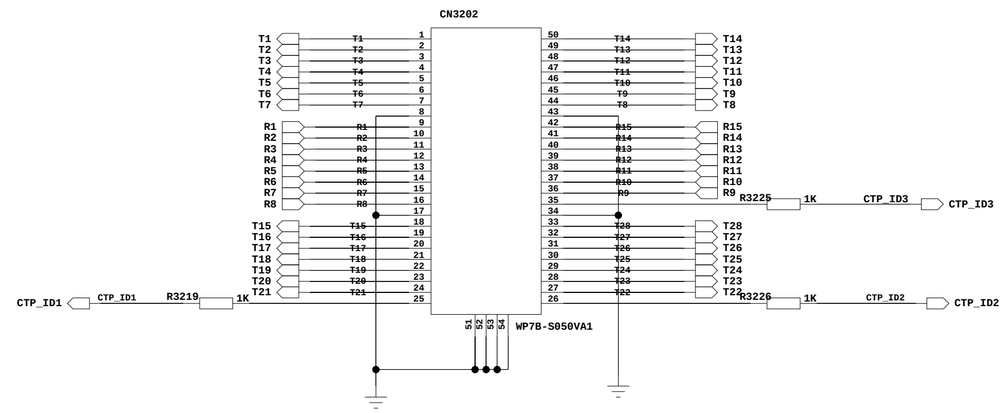
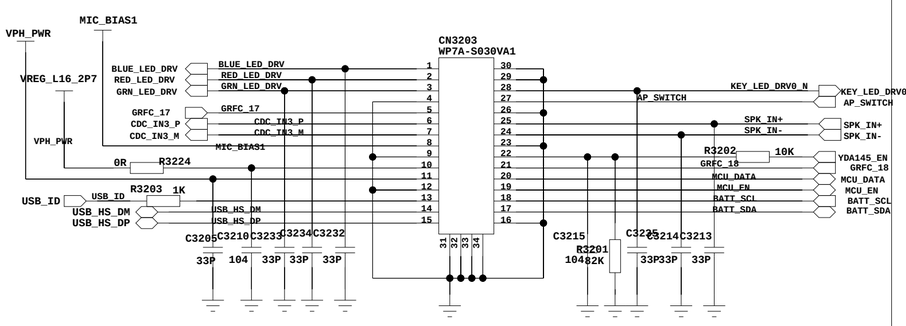


ub board connector



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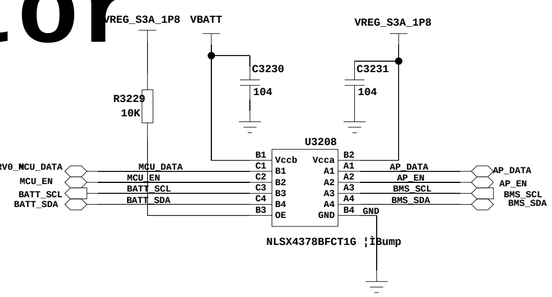
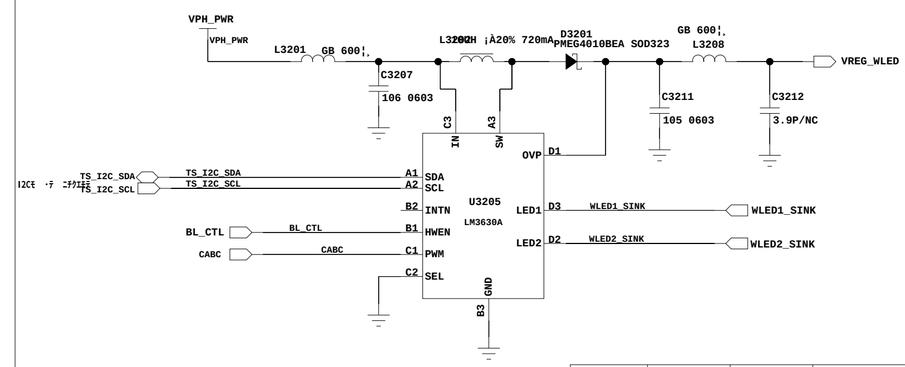


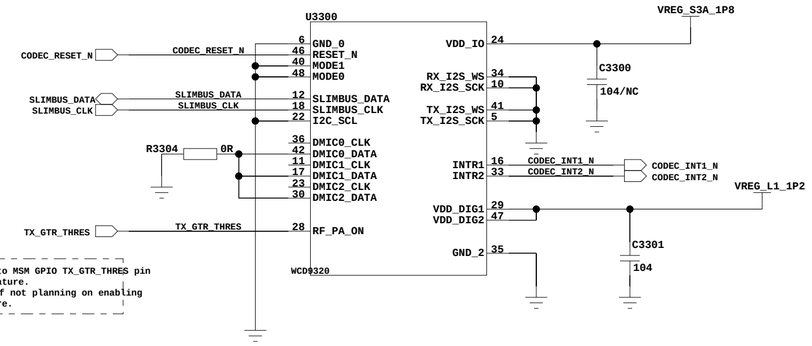
LED DRIVER



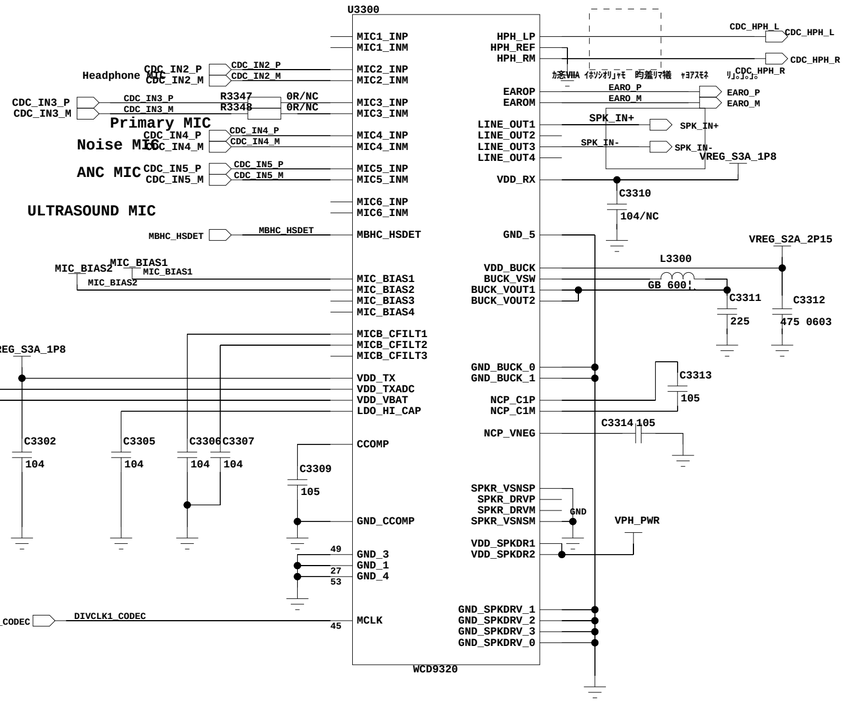
I2C address:36H

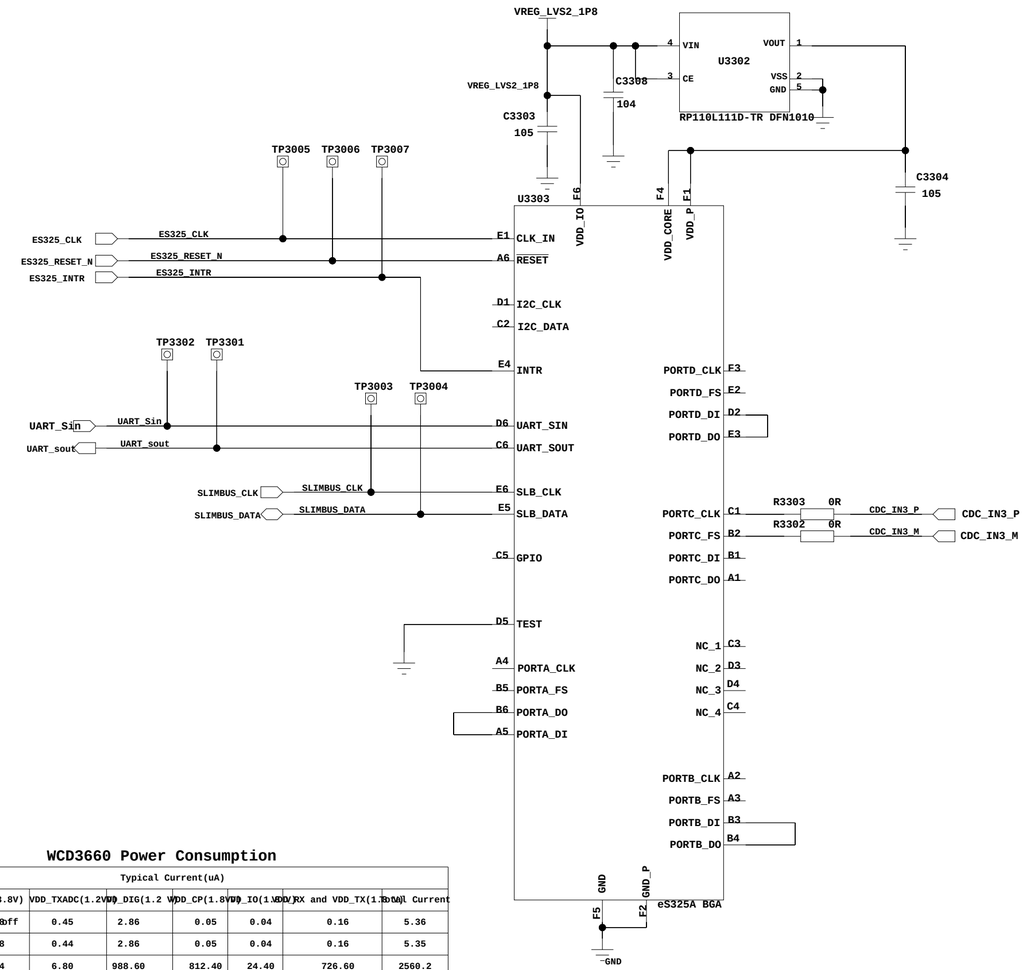
	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 29 of 29 Ver:
Standard By			
Approved By			

	I2S/I2CSLIMbus	
mode0	VDD	GND
mode1	GND	GND



Note: RF_PA_ON connection to MSM GPIO TX_GTR_THRES pin for VBAT Monitoring Feature. Connect RF_PA_ON to GND if not planning on enabling VBAT Monitoring Feature.





WCD3660 Frequency Table

Name	Clock Source Active Mode	Frequency(MHz)
System Clock	GPIO_39(APQ8064)	12.288
MBHC	MCLK	12.288
TxADC	MCLK/2	6.144
RxDAC	MCLK/2	6.144
SLIMBus Clock	MSM LPASS	24.576
	Standby Mode	
System Clock	RC oscillator	12.288
MBHC	RC oscillator	12.288
AUX_PGA	RC oscillator	12.288
Charge Pump	RC oscillator	12.288

WCD3660 Power Tree

VDD_BAT(Pin 63)	VPH_PWR
VDD_TXADC(Pin 41) VDD_DIG(Pin 26)	VREG_L25_1P225
VDD_CP(Pin3) VDD_IO(Pin33) VDDA_RX(Pin30) VDDA_TX(Pin64)	VREG_S4_1P8

WCD3660 Power Consumption

Scenario	Test Conditions	Typical Current(uA)						
		VBAT(3.8V)	VDD_TXADC(1.2V)	VDD_DIG(1.2 V)	VDD_CP(1.8V)	VDD_IO(1.8V)	VDD_RX and VDD_TX(1.8V)	Total Current
Reset	WCD in reset (reset pin held high), MCLK off	1.8	0.45	2.86	0.05	0.04	0.16	5.36
Standby (idle)	WCD taken out of reset, MCLK off	1.8	0.44	2.86	0.05	0.04	0.16	5.35
Stereo playback to HP	48 kHz,24 bits,16 R load quiescent	1.4	6.80	988.60	812.40	24.40	726.60	2560.2
mono-differential line output	48kHz, 24 bits, 10 k? load	4.00	3.00	640.00	4.00	40.00	1445.00	2136.00
Handset voice call	8 kHz sample rate, 16 bits	258.00	325.00	1210.00	644.00	110.00	920.00	3467
Headset voice call	stereo HPH 16R 8 kHz	568.00	159	10	783	10	981	2511
Speaker phone mode	Mono analog mic,8 kHz,16 bits	218	162	810	4	30	1695	2919
Stereo recording	Dual analog mics capless,16 bits,48 kHz	20	324	720	3	70	523	1660

	Sign	Date	Type:	
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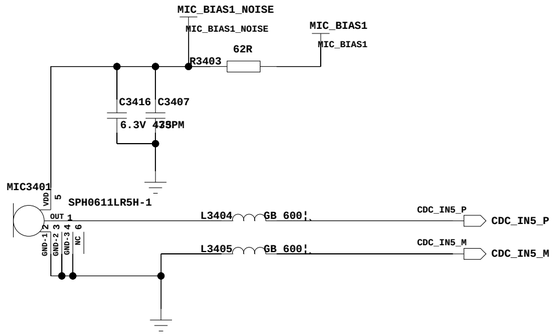
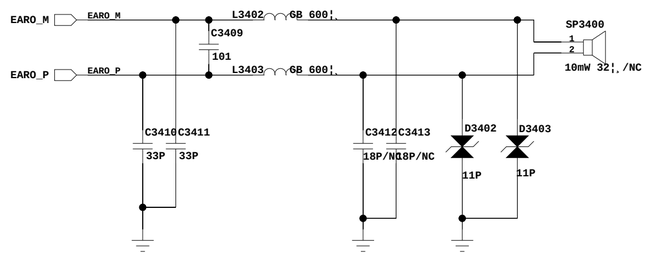
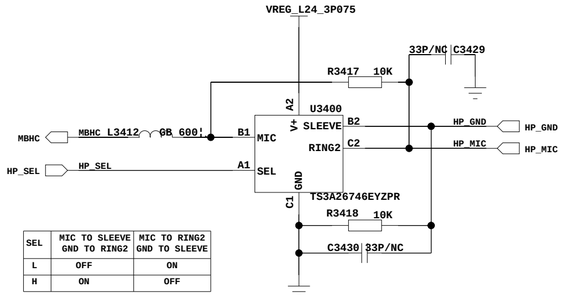
Checked By			Sheet 1 of 29	Ver:
Standard By			oppo	
Approved By				

RECEIVER

ANC MIC

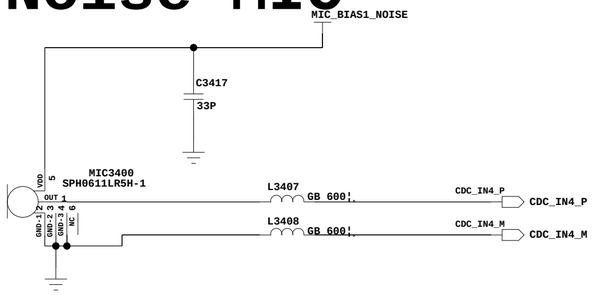


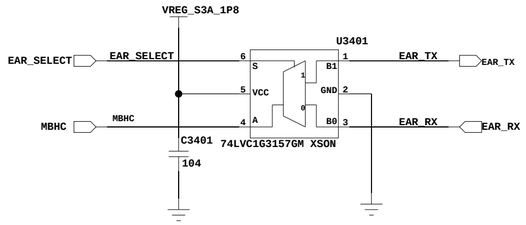




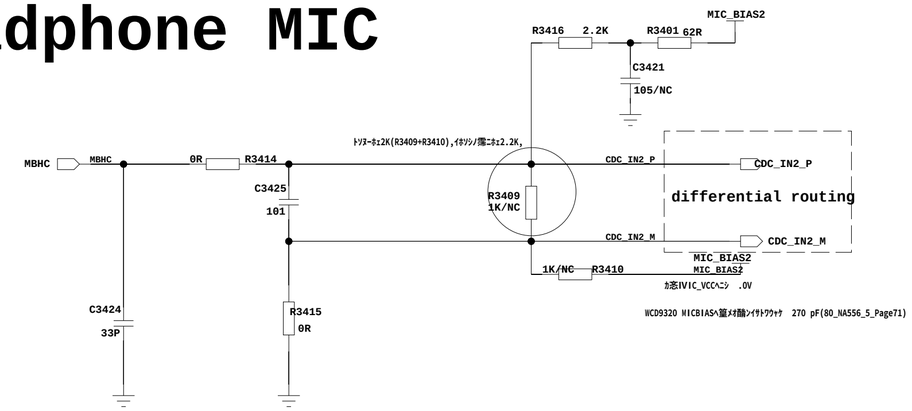
SEL	MIC TO SLEEVE GND TO RING2	MIC TO RING2 GND TO SLEEVE
L	OFF	ON
H	ON	OFF

Noise MIC

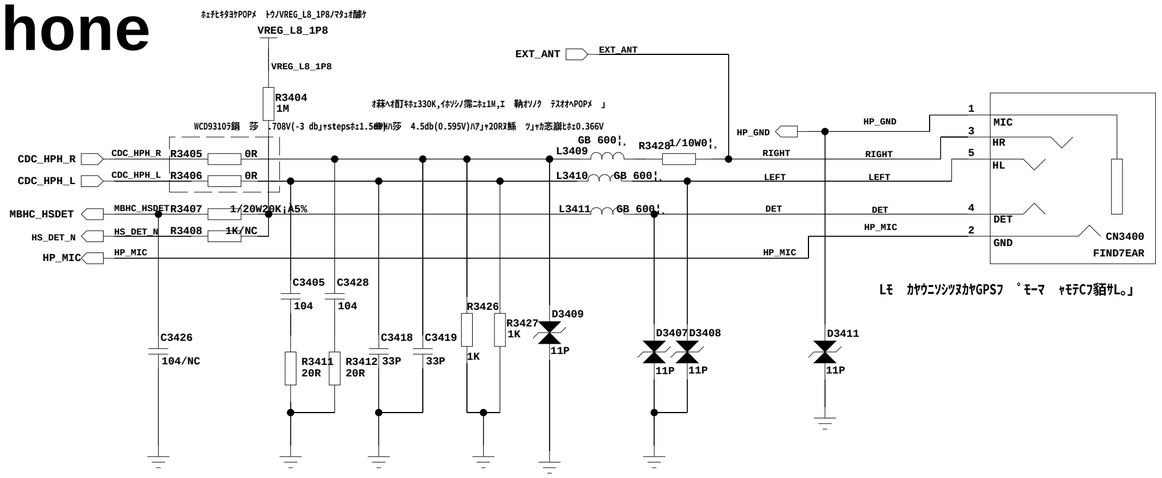




Headphone MIC

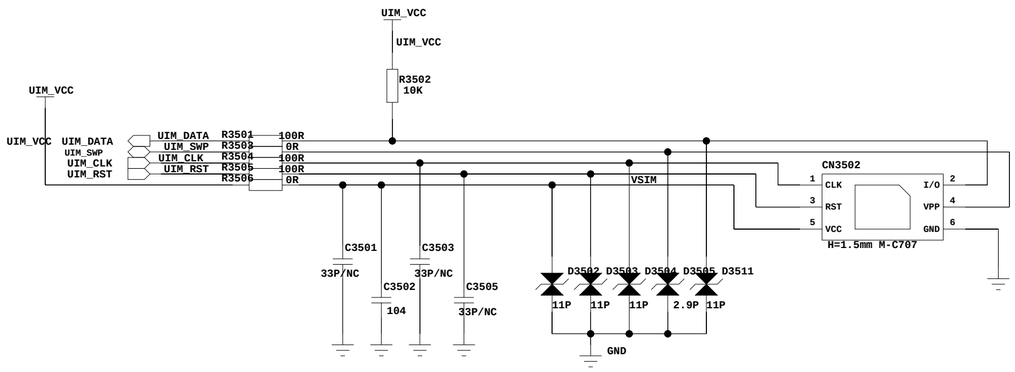


Headphone

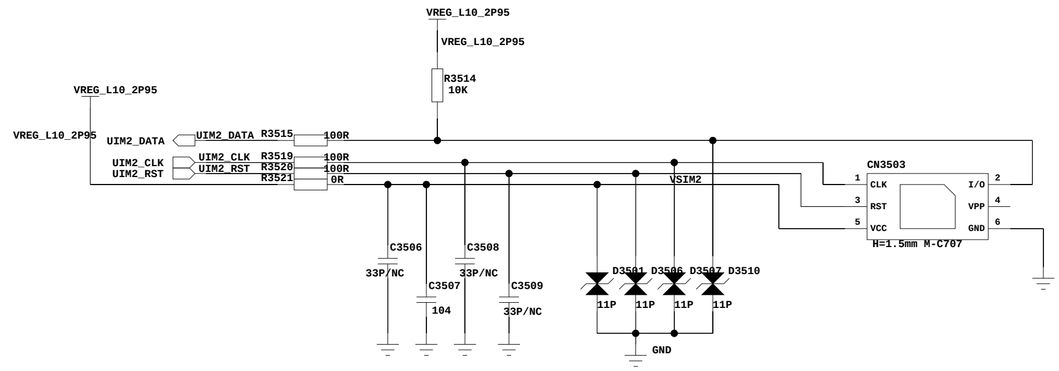


	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 23 of 23 Ver:
Standard By			oppo
Approved By			

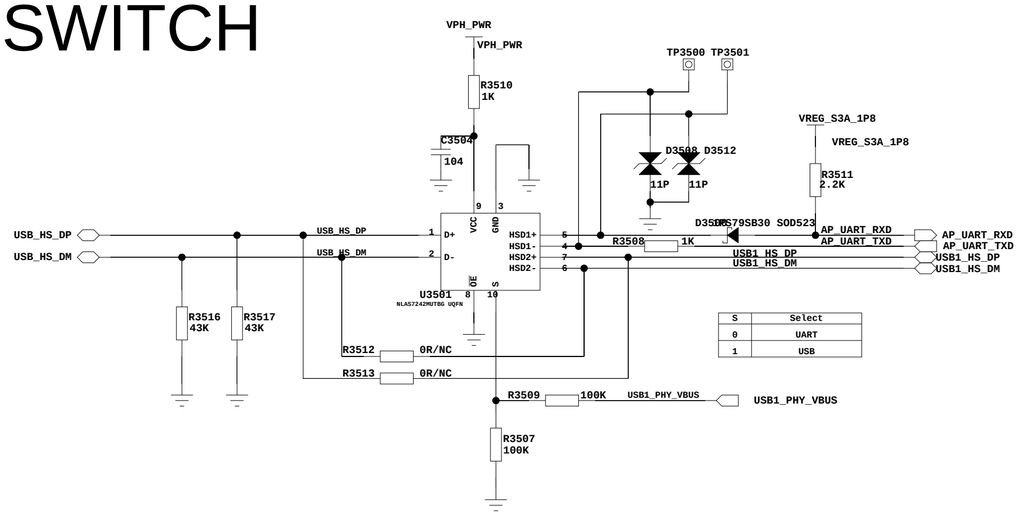
SIM CARD



SIM CARD 2

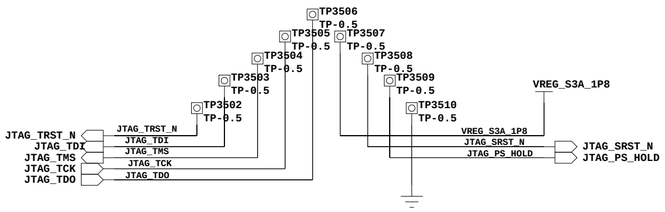


USB SWITCH



S	Select
0	UART
1	USB

MSM8974 JTAG DEBUG



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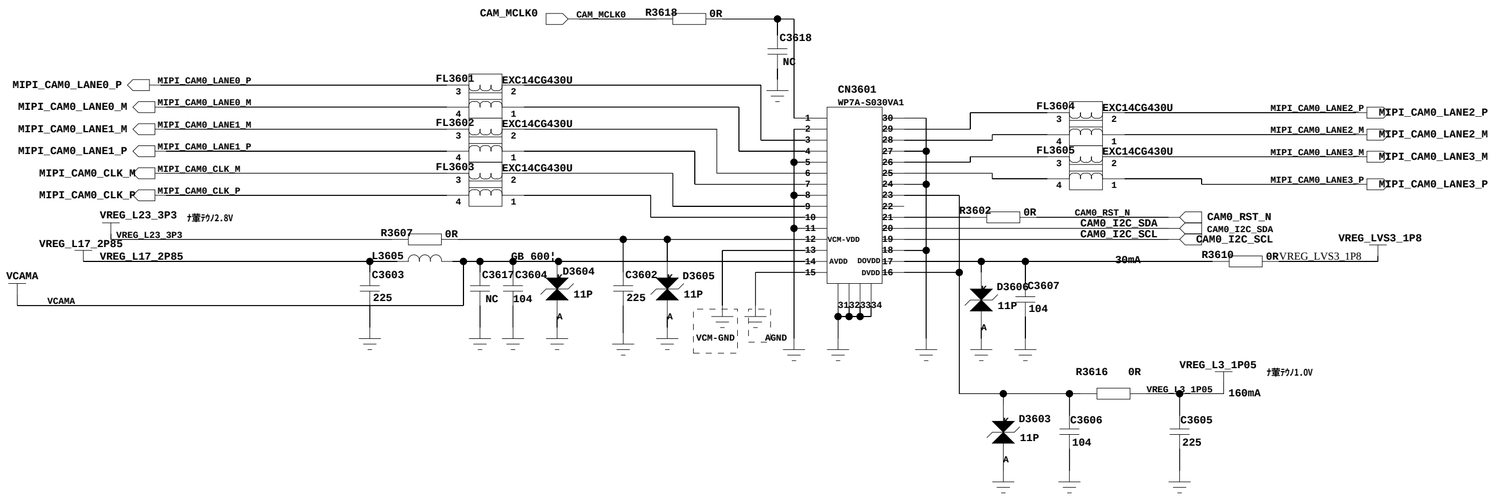
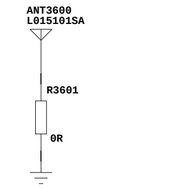
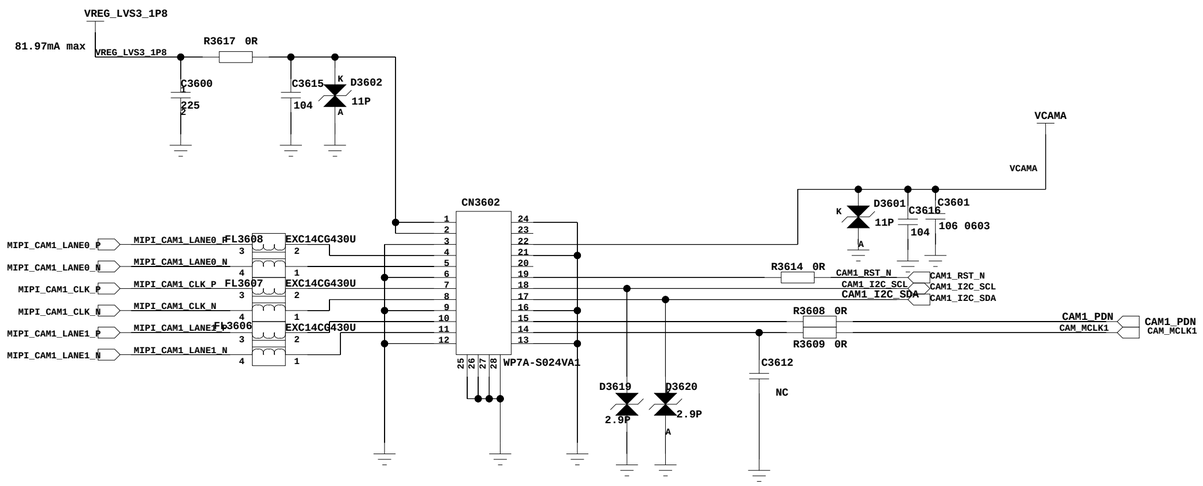
Checked By			Sheet 24 of 24	Ver:
Standard By			oppo	
Approved By				

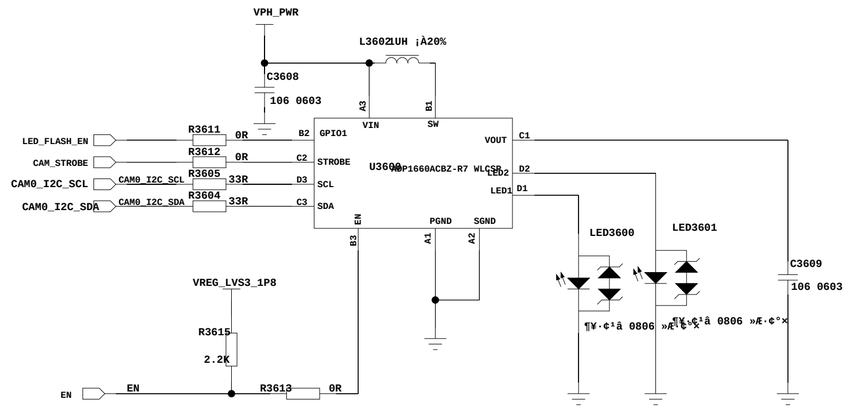




GPS スモオリオッニャ

Flash LED Driver





	Sign	Date	Type:	
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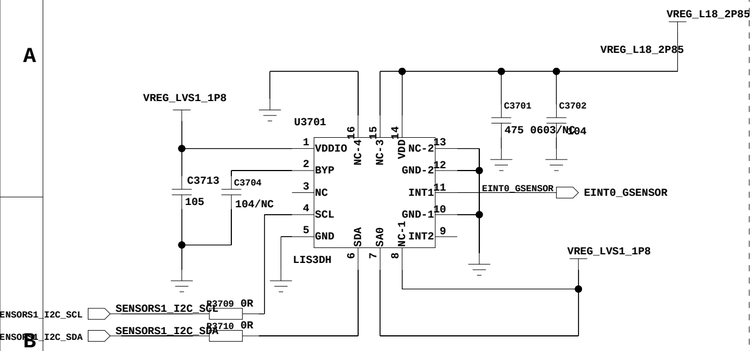
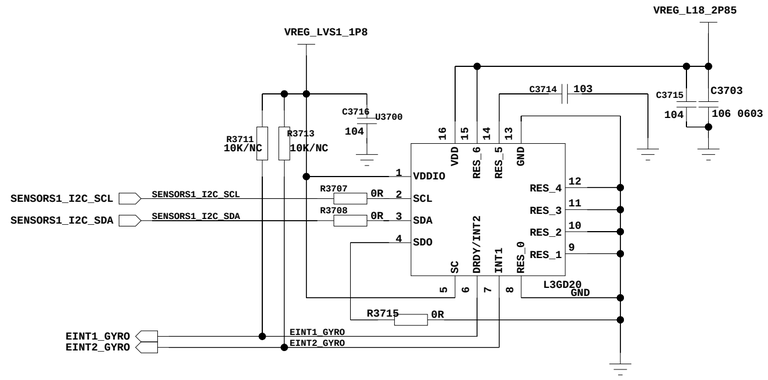
Checked By			Sheet 26_CAMERA 28 of	Ver:
Standard By			oppo	
Approved By				

G-sensor



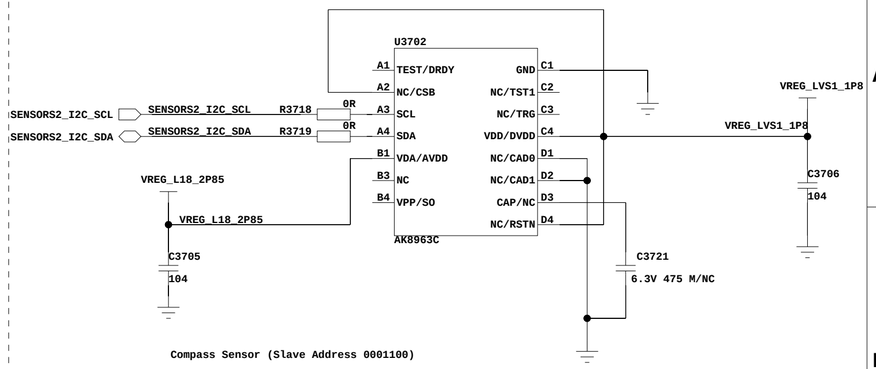
GSensor (Slave Address 0011001)

GYRO



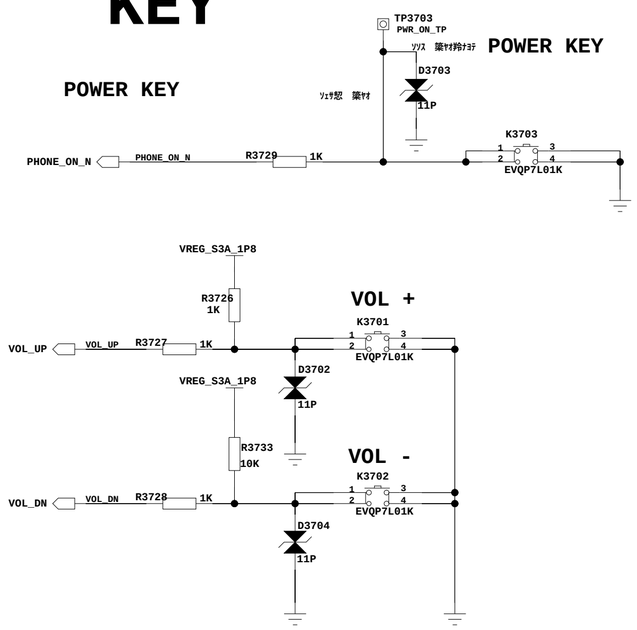
Gyro (Slave Address 1101010)

M-Sensor

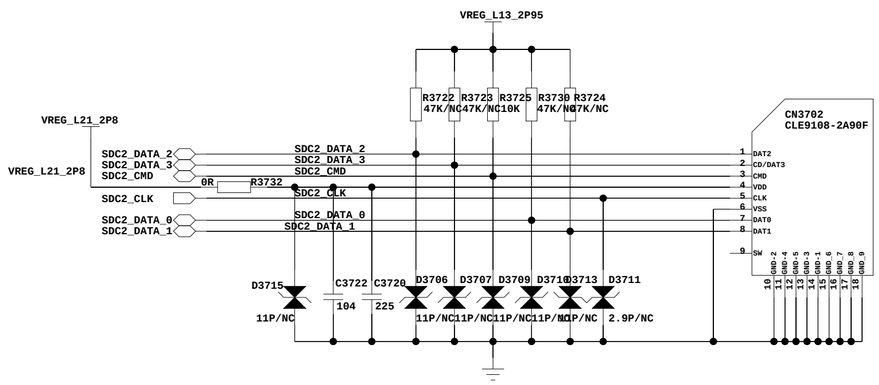


Compass Sensor (Slave Address 0001100)

KEY

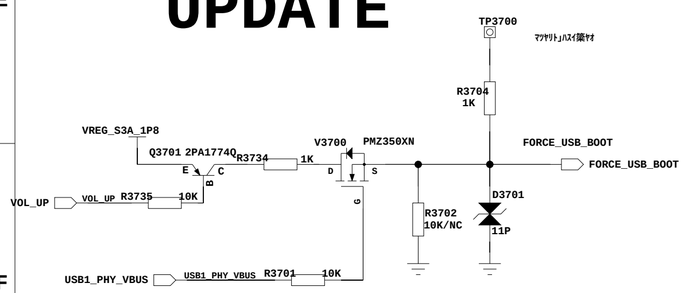


TF CARD

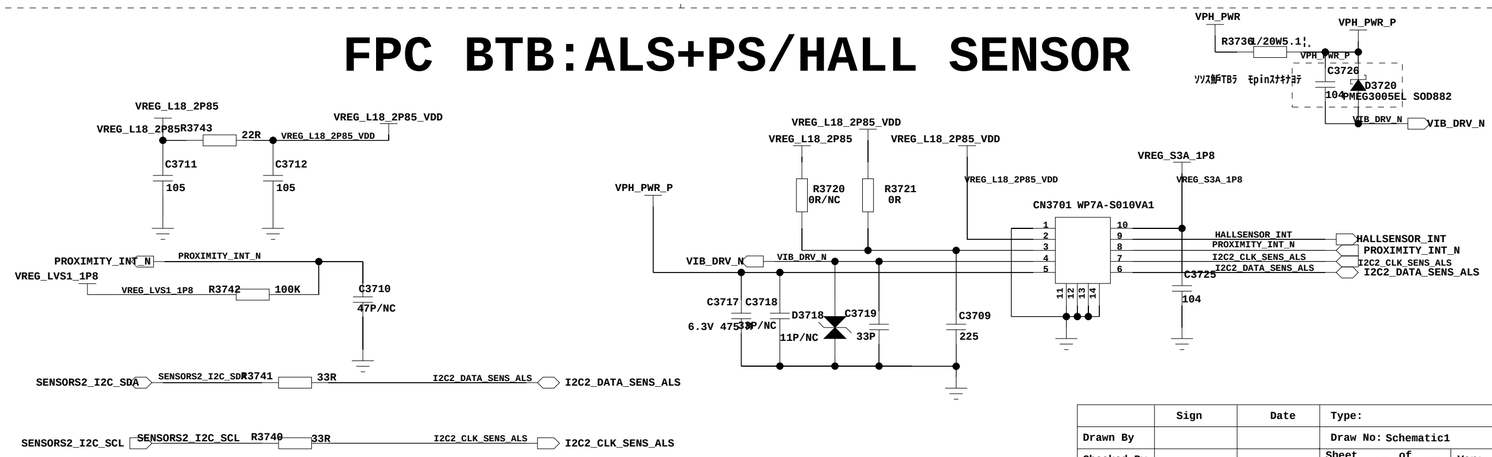


Pressure Sensor

UPDATE



FPC BTB:ALS+PS/HALL SENSOR



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Drawn By			Draw No: Schematic1	
Checked By			Sheet 27 of 27	Ver:
Standard By				
Approved By				