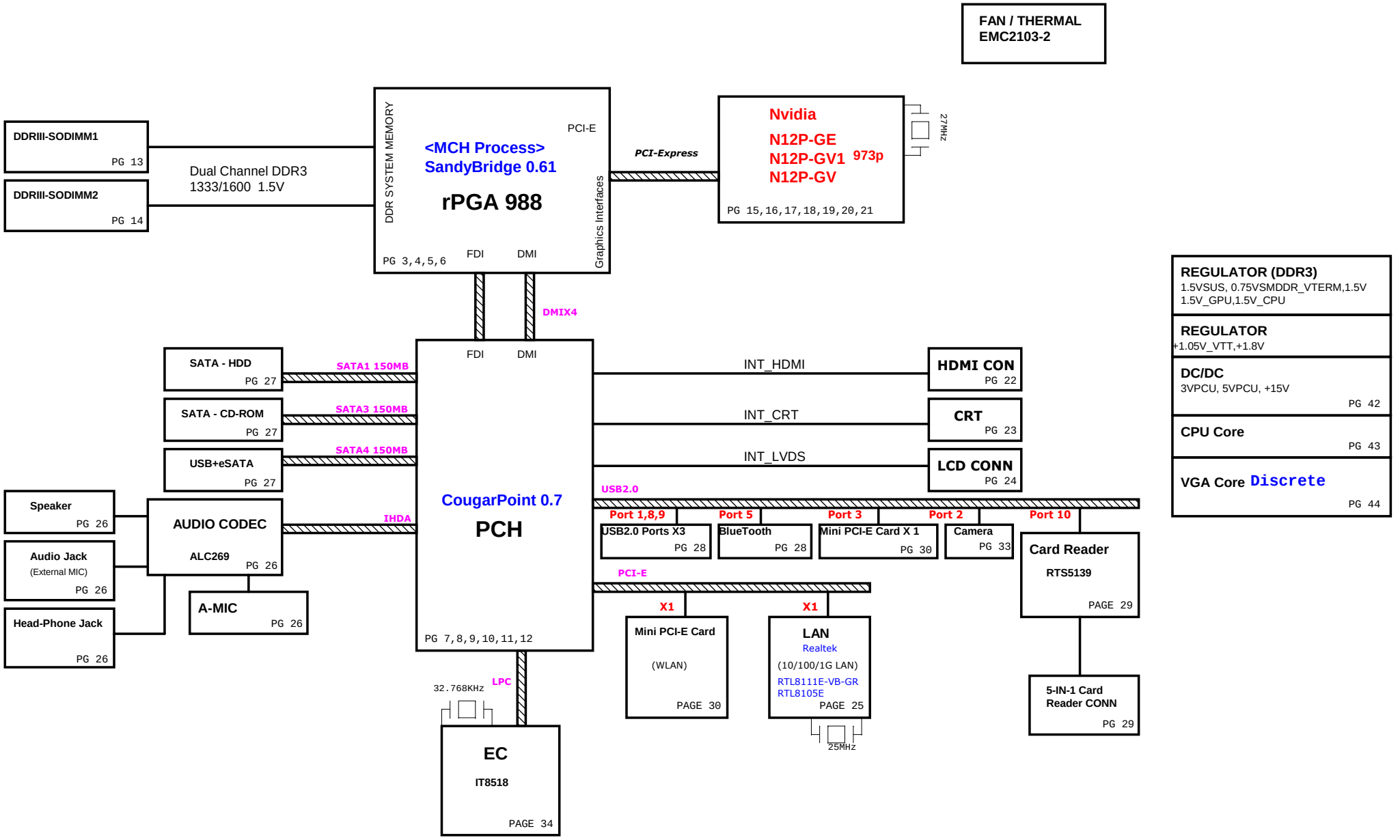
Schematics_ForFree



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Quanta Computer Inc.

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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	15,30,31,32,33,34,35	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	11,12,38	RTC		S0~S5
3VPCU	+3.3V	11,15,18,25,26,28,30,31,34,36	ITE8052 POWER	3V5V_EN	S0~S5
5VPCU	+5V	11,30,31,32,33,34,36	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	15,30,32,34	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	18,30	LAN POWER	LAN_ON	
5V_S5	+5V	12,20,30	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,11,12,21,22,30	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	15,30,35,36	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	26,30,35,36	SLP_S4# CTRLD POWER	SUSON	S0~S3
+VCC_GFX_CORE	+0.9V~+1.2V	6,36	VGA CORE POWER	MAIN_ON	S0
0.9VSMDDR_VTERM	+0.75V	5,14,32	DDR2 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,15,16,17,19,25,27,28,30	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,6,9,10,11,12,14,15,16,17,18,19,21,22,23,24,26,28,30,32,33,34,35	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,21,32	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	6,8,12,17,22,23,36	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V	+1.05V	3,4,6,9,12,30,33	PCH CORE POWER	MAIN_ON	S0
VCC_CORE		6,30,35	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	15	LCD Power	L_VDD_EN	S0
BAT-V	+10V~+17V	31	MAIN BATTERY	CHG_PBATT	S0~S5

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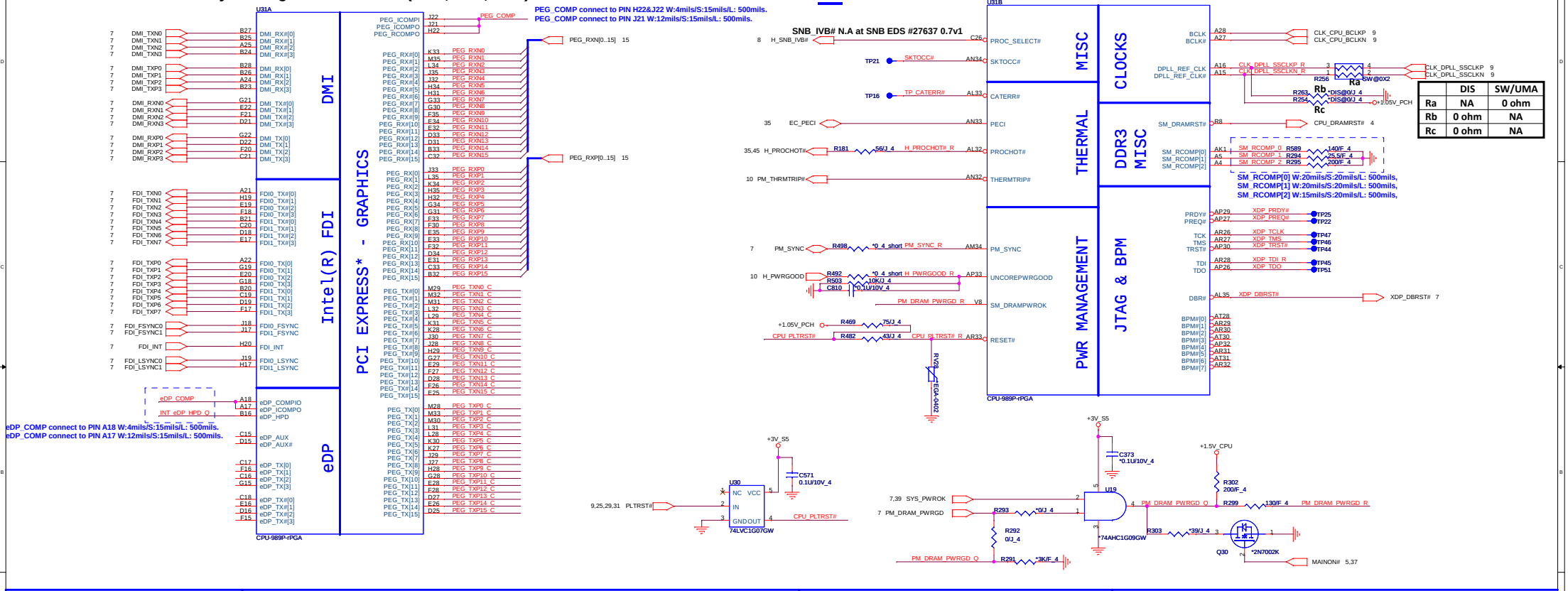
Sandy Bridge Processor (DMI,PEG,FDI)

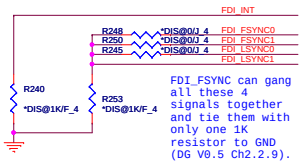
Sandy Bridge Processor (CLK,MISC,JTAG)

03



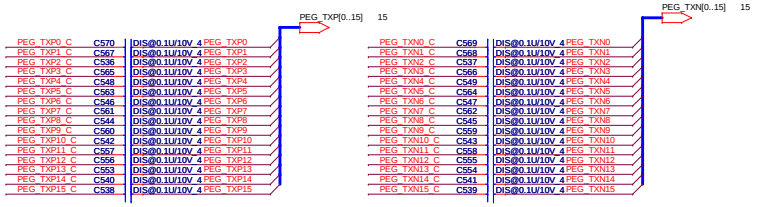
	DIS	SW/UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

FDI Disable

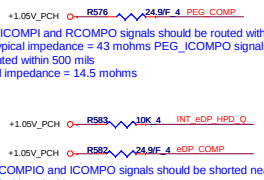


FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 (UMA Non-stuff)



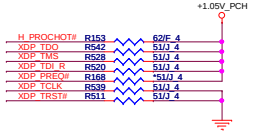
DP & PEG Compensation



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)



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Sandy Bridge Processor (DDR3)

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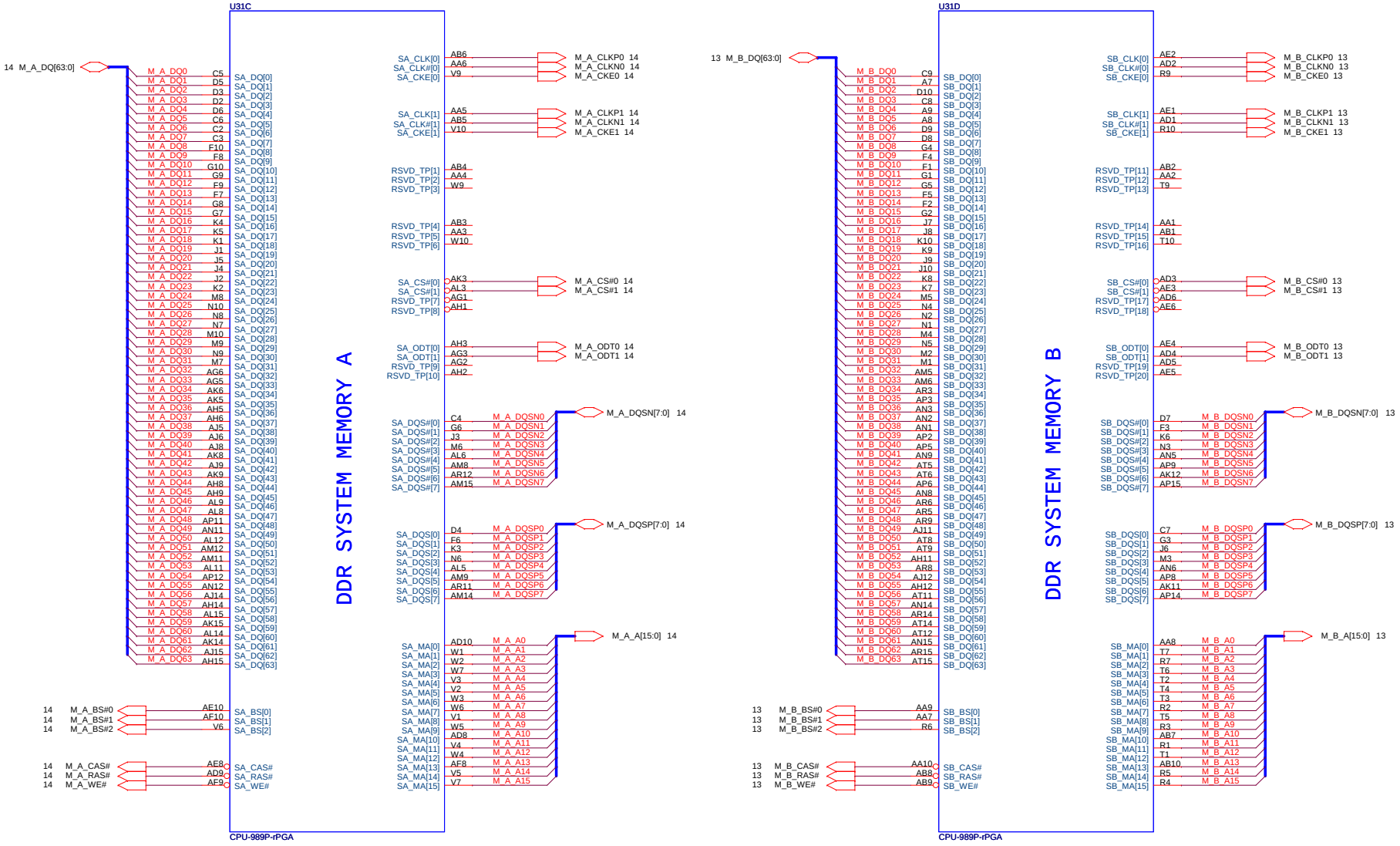

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Quanta Computer Inc.			
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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

CPU VGT
SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

POWER
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
GRAPHICS
DDR3 -1.5V RAILS
VREF
SA RAIL
1.8V RAIL
MISC

Reserved

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Close to VR
Place PU resistor close to CPU
SVID DATA
Close to VR
Place PU resistor close to CPU
SVID ALERT

4.5A

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

3/26 DB add for Intel. Placement close to CPU.

Ra	DIS	SW
Ra	0 ohm	NA

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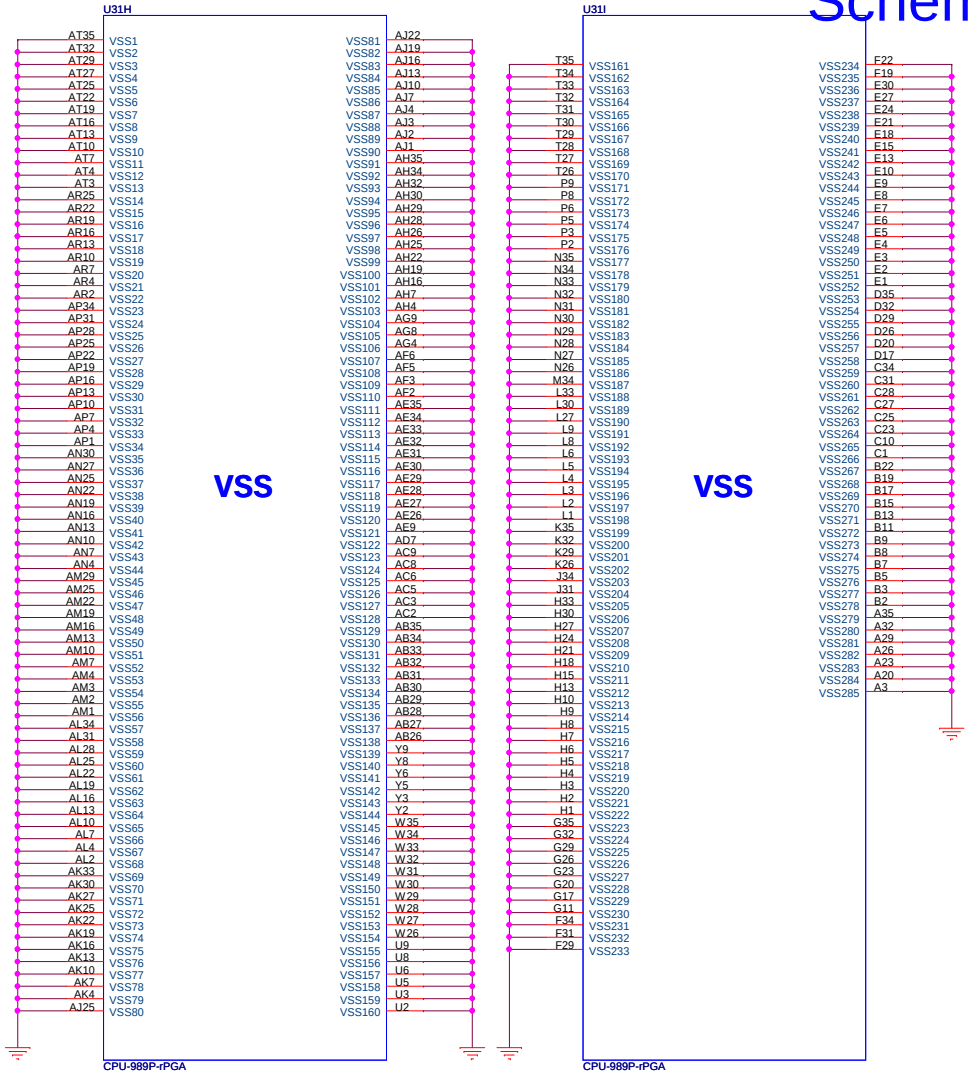
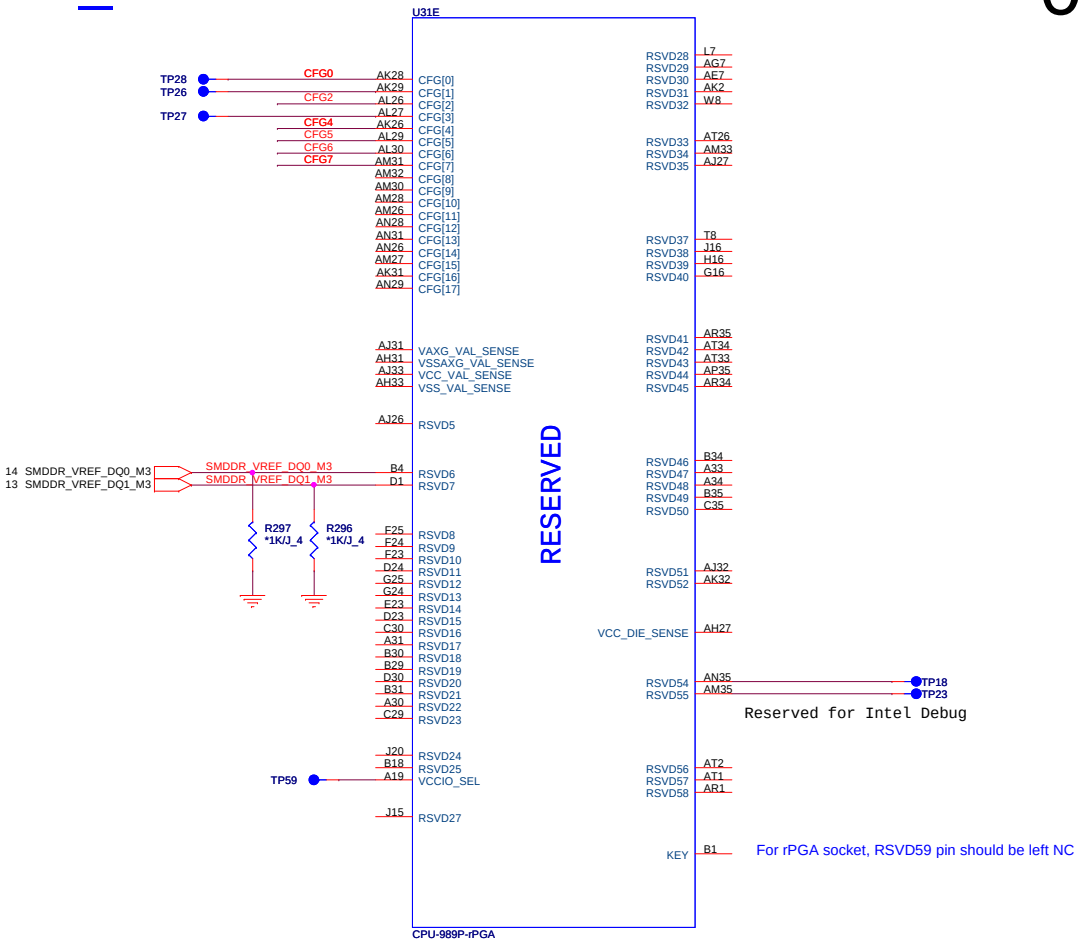
Sandy Bridge Processor (GND)



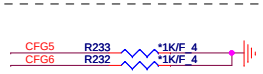
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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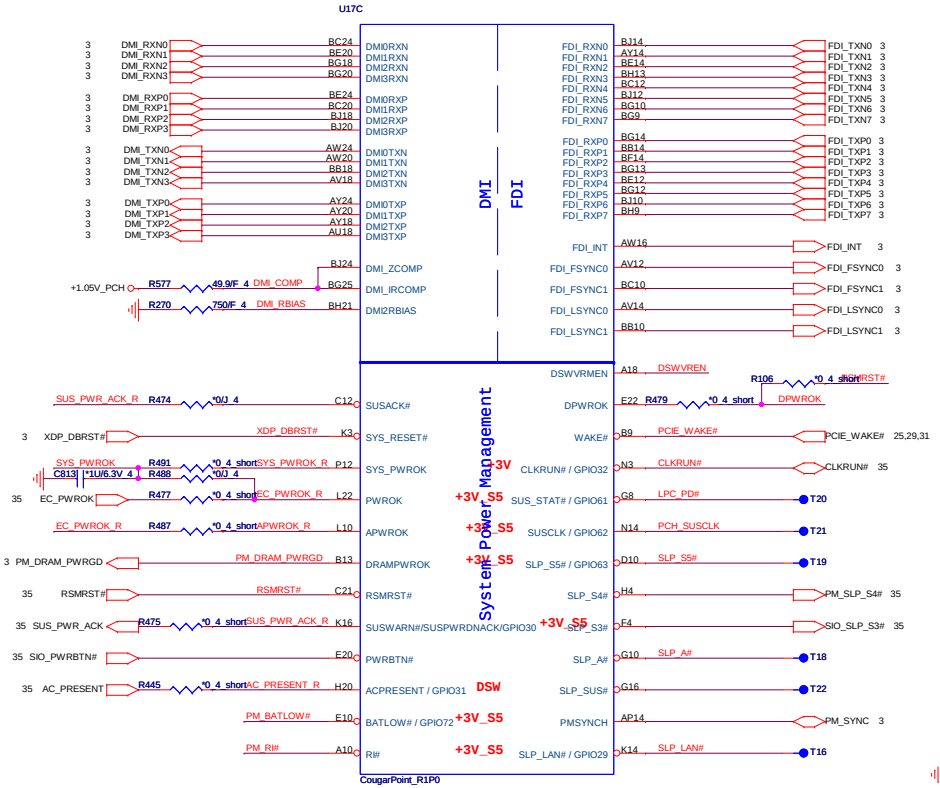
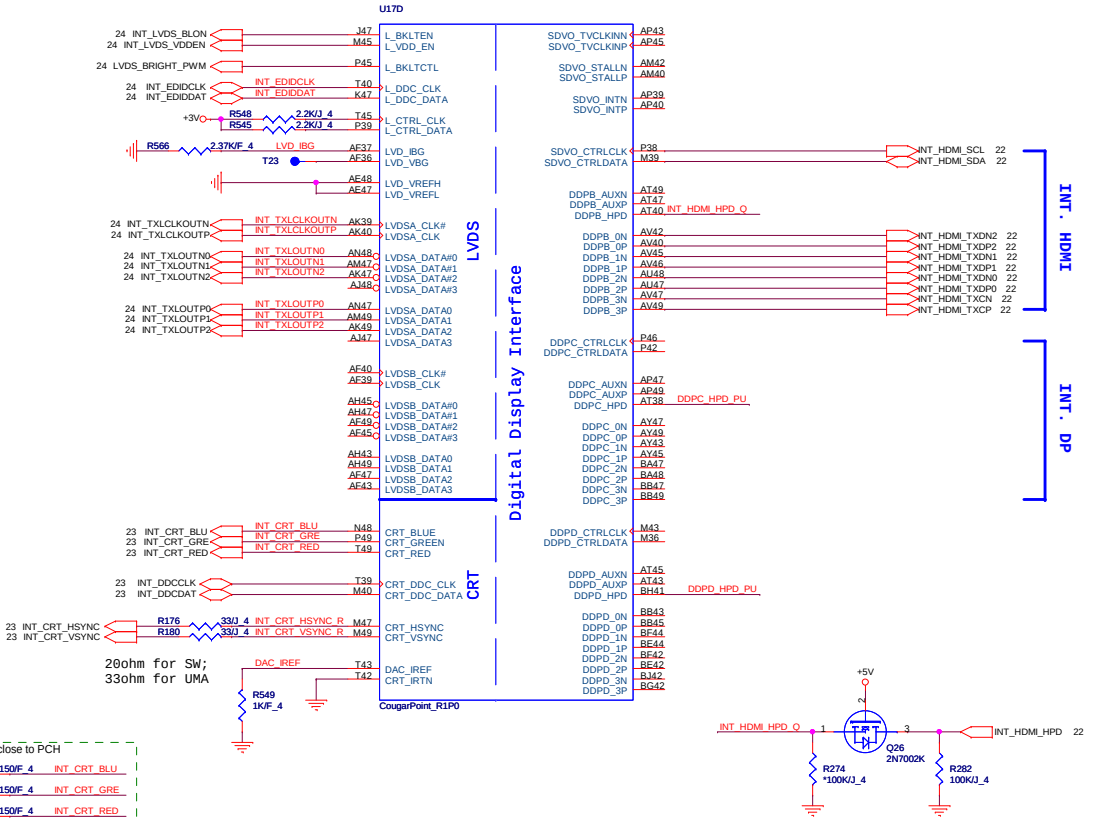
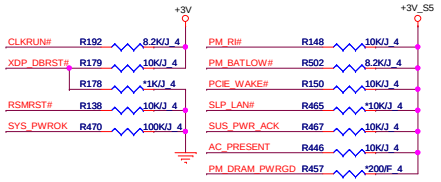
Cougar Point (DMI,FDI,PM)



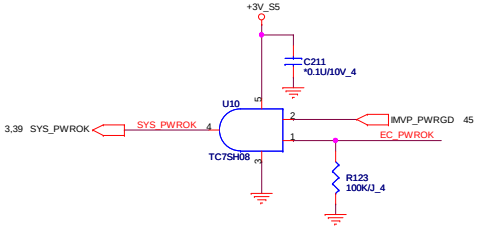
Cougar Point (LVDS,DDI)

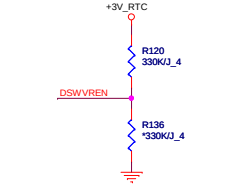


PCH Pull-high/low(CLG)

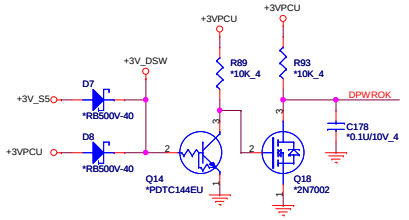


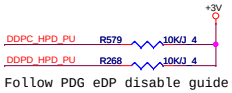
System PWR_OK(CLG)





DPWROK FOR DSW





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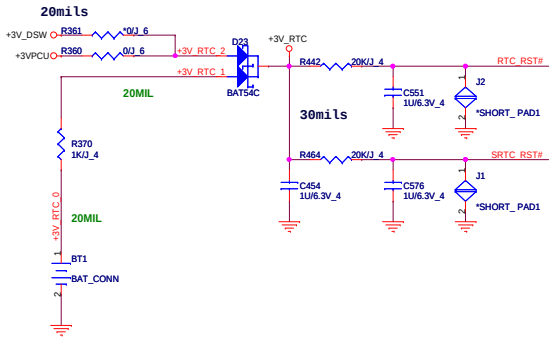
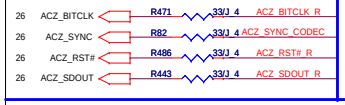
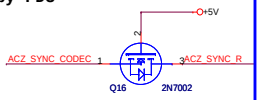
RTC Circuitry(RTC)



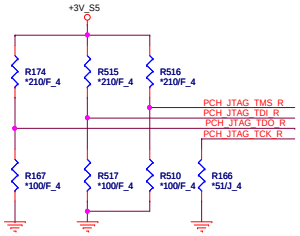
HDA Bus(CLG)



To Separate Codec Sync by PD3



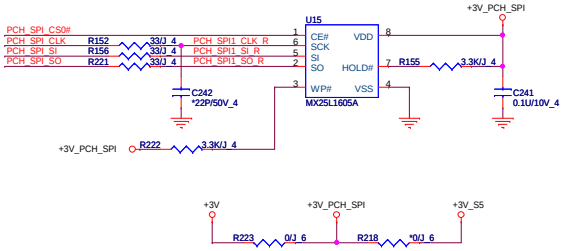
PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

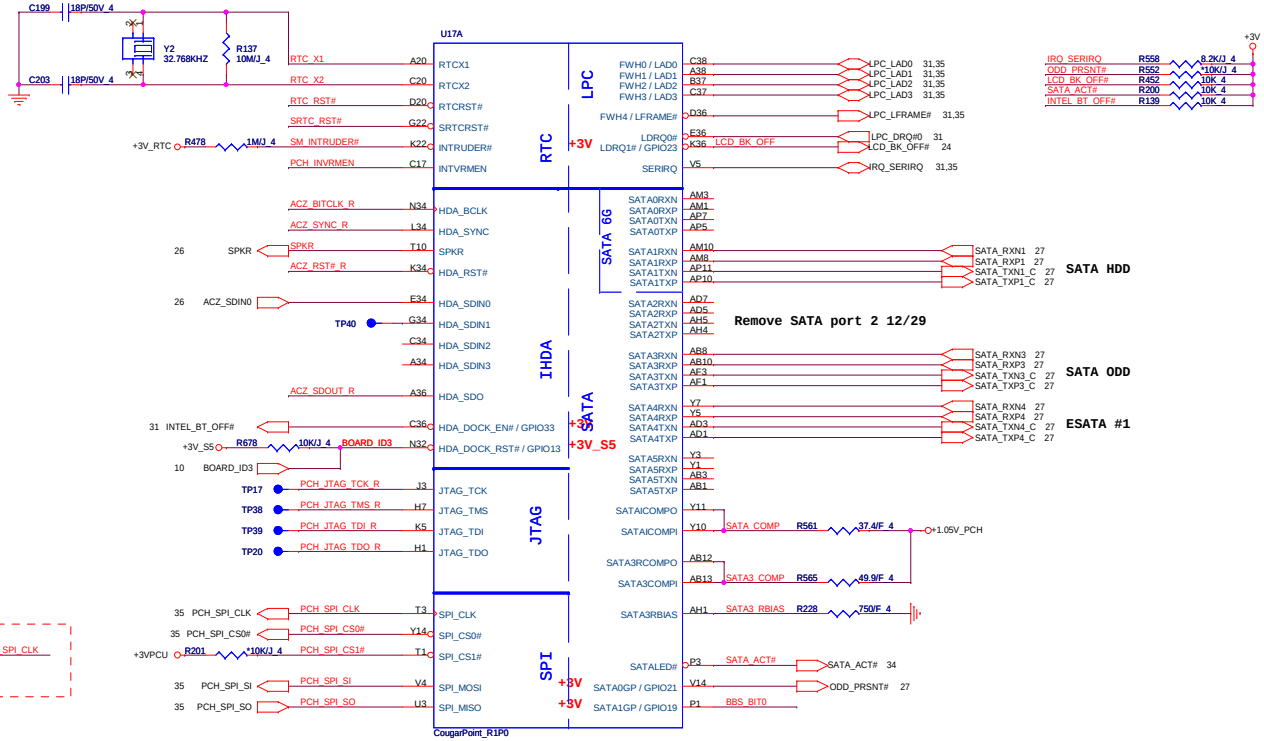
32Mbit (4M Byte), SPI

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031



PCH2(CLG)

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R557 *1K/J 4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R521 *1K/J 4 PCI_GNT3# 9
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R121 330K/J 4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] R504 *1K/J 4 BBS_BIT1 9 R193 *1K/J 4 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R463 *1K/J 4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R265 2.2K/J 4 R266 4.7K/J 4 +1.8V DF_TVS 10 H_SNB_IVB# 3
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R522 *1K/J 4 PLL_ODVR_EN 10
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R81 1K/J 4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R146 *1K/J 4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

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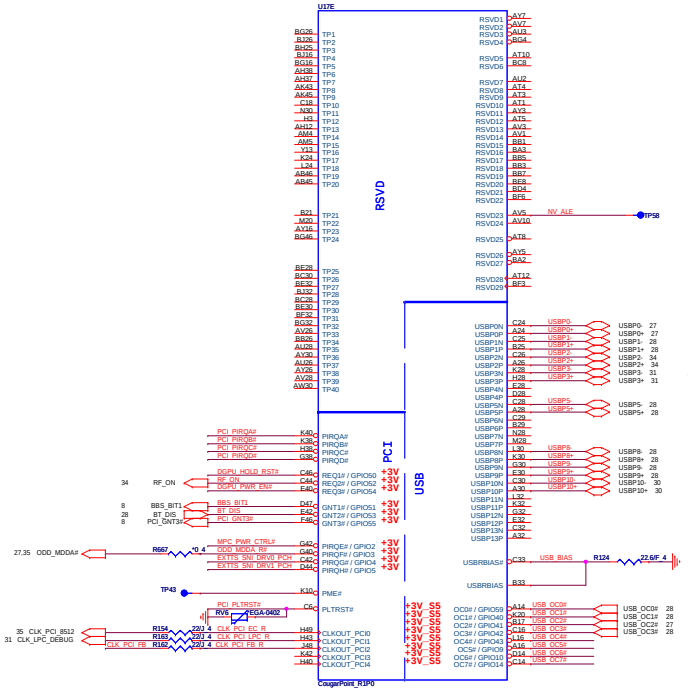
Cougar Point-M (PCI,USB,NVRAM)



USB/eSATA Combo #1(Phoenix debug)
USB#0-> L port((BIOS debug)
CCD
WLAN
WWAN(common design reserved)
BlueTooth

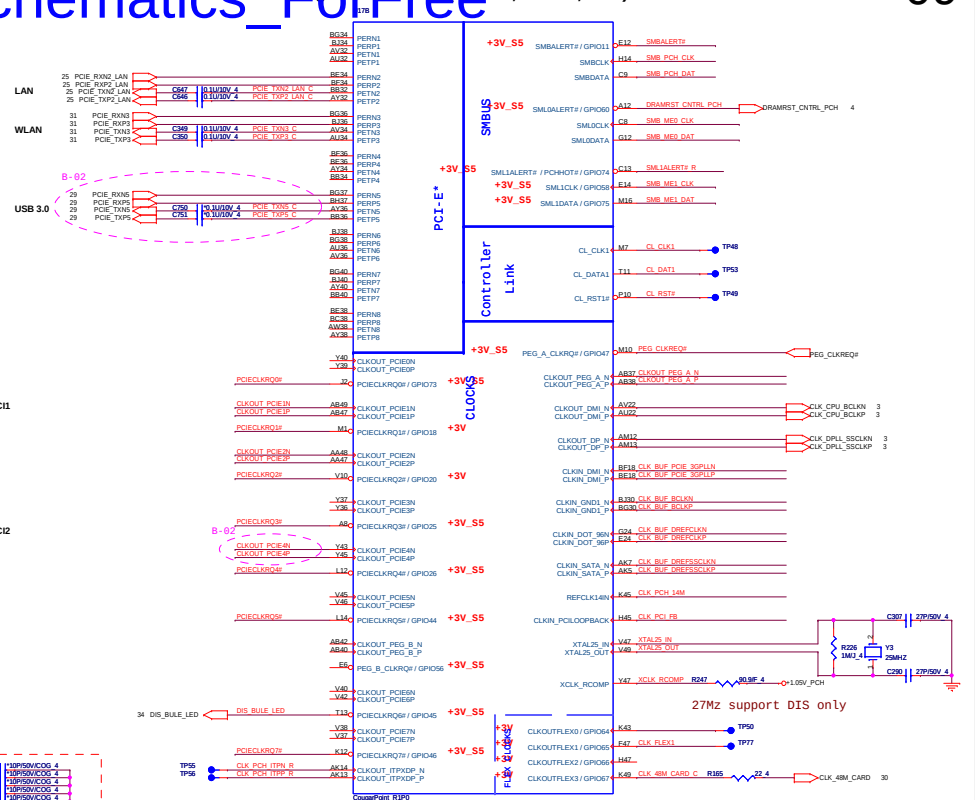
EHCI1

USB#2-->R port(Right side)
USB #1-->R port(DB&BIOS debug)
Card Reader

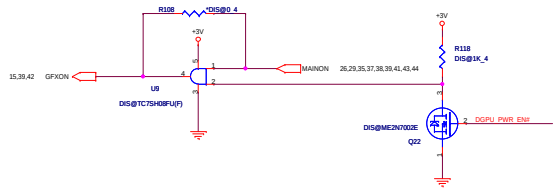
EHCI2

USB port 6,7disable for HM65.

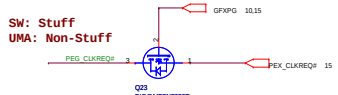
Cougar Point-M (PCI-E,SMBUS,CLK)



DGPU Power ON

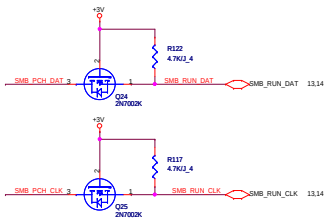


PEG CLK detect

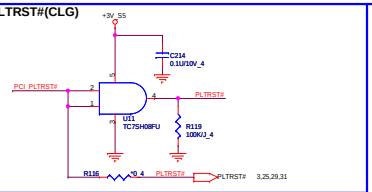


RF request

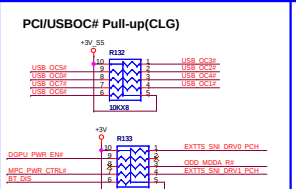
SMBus(CLK)



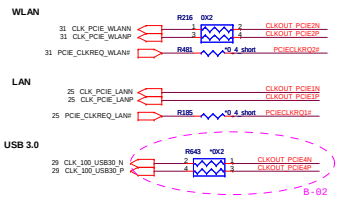
PLTRST#(CLG)



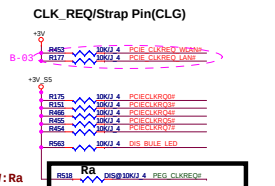
PCI/USBOC# Pull-up(CLG)



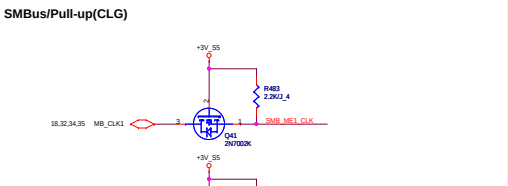
WLAN / LAN / USB 3.0



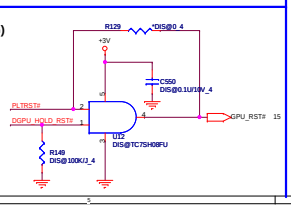
CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



GPU RST#(CLG)



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Cougar Point (GPIO,NCTF,RSVD)

U17F

S_GPIO R546 100_4 — T7 BMBUSY# / GPIO0 +3V
29,35 EC_EXT_SMI# — A42 TACH1 / GPIO1 +3V
BOARD_ID1 — H36 TACH2 / GPIO6 +3V
35 EC_EXT_SCI# — E38 TACH3 / GPIO7 +3V
TP76 ICC_EN# — C10 GPIO8 +3V_S5
31 LAN_DISABLE# — C4 LAN_PHY_PWR_CTRL / GPIO12 +3V_S5
HOST_ALERT#1_R — G2 GPIO15 +3V_S5
BOARD_ID0 — U2 SATA4GP / GPIO16 +3V
GFXPG_R — D40 TACH0 / GPIO17 +3V
BIOS_REC — T5 SCLOCK / GPIO22 +3V
USB30_ID — E8 GPIO24 / MEM_LED +3V_S5
GPIO27 — E16 GPIO27 DSW
8 PLL_ODVR_EN — R536 *0_4_short PLL_ODVR_EN_R — P8 GPIO28 +3V_S5
SYSTEM_ID — K1 STP_PCI# / GPIO34 +3V
28 BT_ON# — K4 GPIO35 +3V
TP54 DMI_OVRVLTG — V8 SATA2GP / GPIO36 +3V
FDI_OVRVLTG — M5 SATA3GP / GPIO37 +3V
MFG_MODE — N2 SLOAD / GPIO38 +3V
DGPU_PRSNT# — M3 SDATAOUT0 / GPIO39 +3V
TEST_SET_UP — V13 SDATAOUT1 / GPIO48 +3V
32,35 TEMP_ALERT# — V3 SATA5GP / GPIO49 +3V
SV_DET — D6 GPIO57 +3V_S5

GPIO

CPU_ID — C40 TACH4 / GPIO68
R126 1.5K/F_4 — B41 TACH5 / GPIO69
COLOR_ENGINE_DET — C41 TACH6 / GPIO70
BOARD_ID2 — A40 TACH7 / GPIO71

CPU/MISC

P4 A20GATE — EC_A20GATE 35
AU16 PECI — TP57
P5 RCIN# — EC_RCIN# 35
AY11 PROCPWRGD — H_PWRGOOD 3
AY10 THRMTRIP# — PCH_THRMTRIP# R578 390/J_4 — PM_THRMTRIP# 3
T14 INIT3_3V#
AY1 DF_TVS — DF_TVS 8

AH8 TS_VSS1
AK11 TS_VSS2
AH10 TS_VSS3
AK10 TS_VSS4
P37 NC_1

NCTF

A4 VSS_NCTF_1
A44 VSS_NCTF_2
A45 VSS_NCTF_3
A46 VSS_NCTF_4
A5 VSS_NCTF_5
A6 VSS_NCTF_6
B3 VSS_NCTF_7
B47 VSS_NCTF_8
BD1 VSS_NCTF_9
BD49 VSS_NCTF_10
BE1 VSS_NCTF_11
BE49 VSS_NCTF_12
BF1 VSS_NCTF_13
BF49 VSS_NCTF_14

BG2 VSS_NCTF_15
BG48 VSS_NCTF_16
BH3 VSS_NCTF_17
BH47 VSS_NCTF_18
BJ4 VSS_NCTF_19
BJ44 VSS_NCTF_20
BJ45 VSS_NCTF_21
BJ46 VSS_NCTF_22
BJ5 VSS_NCTF_23
BJ6 VSS_NCTF_24
C2 VSS_NCTF_25
C48 VSS_NCTF_26
D1 VSS_NCTF_27
D49 VSS_NCTF_28
E1 VSS_NCTF_29
E49 VSS_NCTF_30
F1 VSS_NCTF_31
F49 VSS_NCTF_32

CougarPoint_R1P0

R114 *DIS@0_4 — +3V
GFXPG_R — GFXPG_R — U8 — HWPG 35,39,40,41,43,44,45 — GFXPG 9,15
DIS@TC7SH08FU(F)

SGPIO

S_GPIO — R551 10K/J_4 — R550 *0/J_4 — +3V

GPIO Pull-up/Pull-down(CLG)

+3V_S5
LAN_DISABLE# — R164 10K/J_4
+3V
COLOR_ENGINE_DET R644 10K_4
EC_EXT_SMI# R127 10K/J_4
EC_EXT_SCI# R461 10K/J_4
EC_A20GATE R543 10K/J_4
EC_RCIN# R556 10K/J_4
TEMP_ALERT# R211 10K/J_4
BT_ON# R507 10K/J_4
GPIO27 R490 10K/J_4
GFXPG_R R113 DIS@10K/J_4

Board ID

B-04

Board ID For Function	SYSTEM_ID GPIO34	ID2 GPIO71	ID3 GPIO13	ID1 GPIO6	ID0 GPIO16	CPU_ID GPIO68
SDV	1	1	0	0	0	1
SIV	1	1	0	0	1	1
SIT	1	1	0	1	0	1
SVT	1	1	0	1	1	1
SOVP	1	1	1	0	0	1

Board ID use below GPIO:
BOARD_ID0
BOARD_ID1
BOARD_ID3

ID2: 0-->6 layer
1-->8 layer

System ID: 0-->KL5
1-->KL6

CPU_ID: 0-->35W
1-->45W

+3V
R675 *10K/J_4 CPU_ID R676 10K/J_4
R207 10K/J_4 BOARD_ID0 R199 *10K/J_4
R462 *10K/J_4 BOARD_ID1 R444 10K/J_4
R140 10K/J_4 BOARD_ID2 R125 *10K/J_4
R147 *10K/J_4 SYSTEM_ID R142 10K/J_4
+3V_S5
R682 10K/J_4 BOARD_ID3 R683 *10K/J_4 — BOARD_ID3 8

SV_SET_UP
High = Strong (Default)

TEST_SET_UP — R559 10K/J_4 — R555 *0/J_4 — +3V

USB30_ID	GPIO24
USB3.0	0
Non-USB3.0	1

+3V_S5
R679 *10K/J_4 USB30_ID R680 10K/J_4

+3V
R509 *10K/J_4 SV_DET R501 100K/J_4

HOST_ALERT#1_R R508 1K/J_4 — +3V_S5

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

	SWITCHABLE	UMA
Stuff	R532	R533
No Stuff	R533	R532

+3V
R533 *10K/J_4 DGPU_PRSNT# R532 DIS@100K/J_4

R526 100K/J_4 FDI_OVRVLTG R527 *1K/F_4 — +3V

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI_OVRVLTG R668 *200K/F_4 — +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS_REC — R547 10K/J_4 — R554 *0/J_4 — +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

MFG_MODE — R184 10K/J_4 — R194 *0/J_4 — +3V

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Quanta Computer Inc.

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	Cougar Point 4/6	1A
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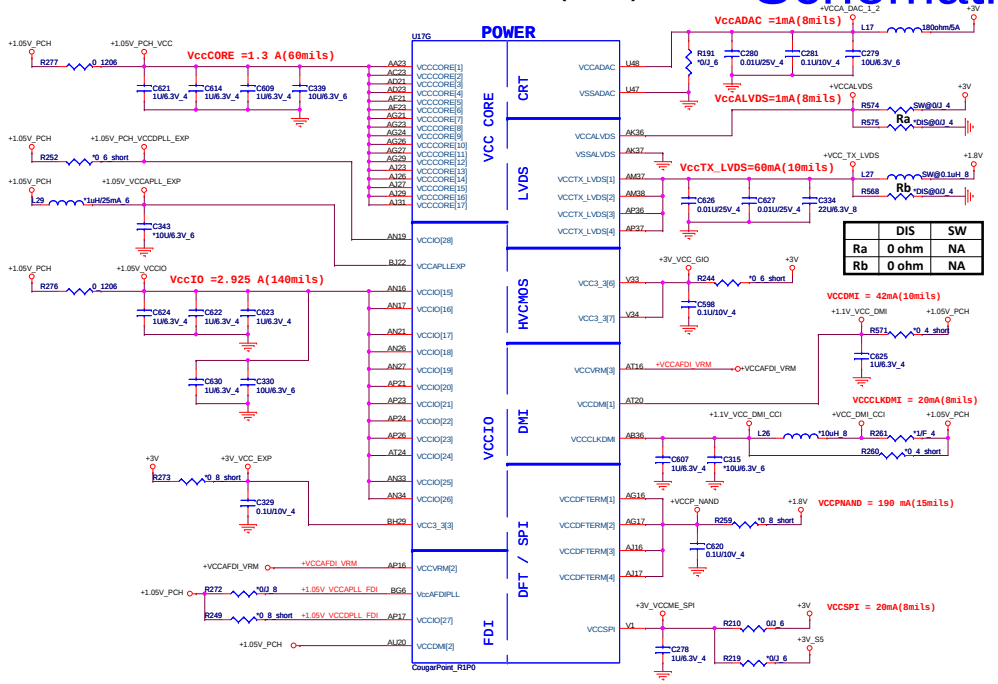
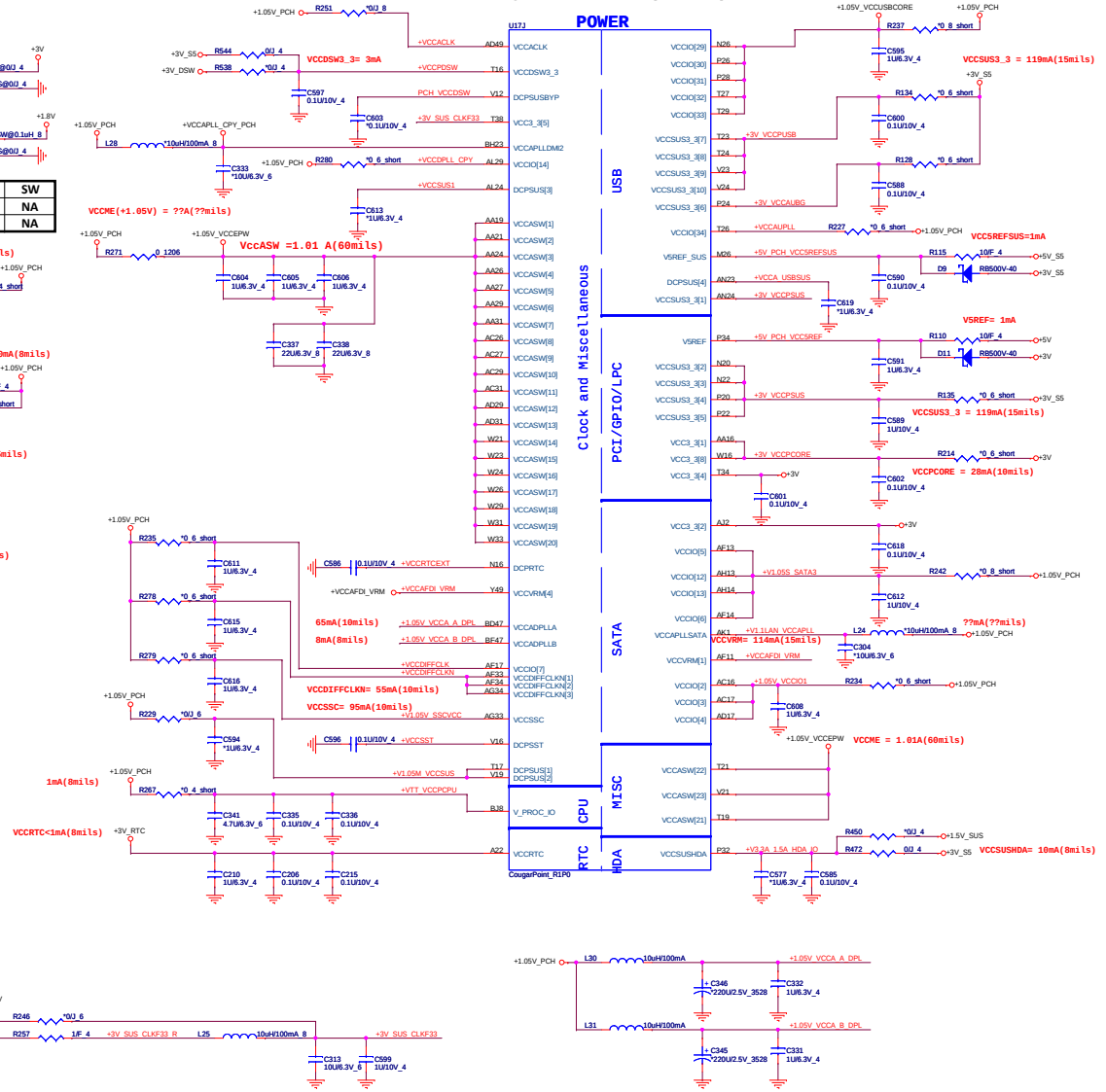
COUGAR POINT (POWER)

Schematics_ForFree



Cougar Point-M (POWER)



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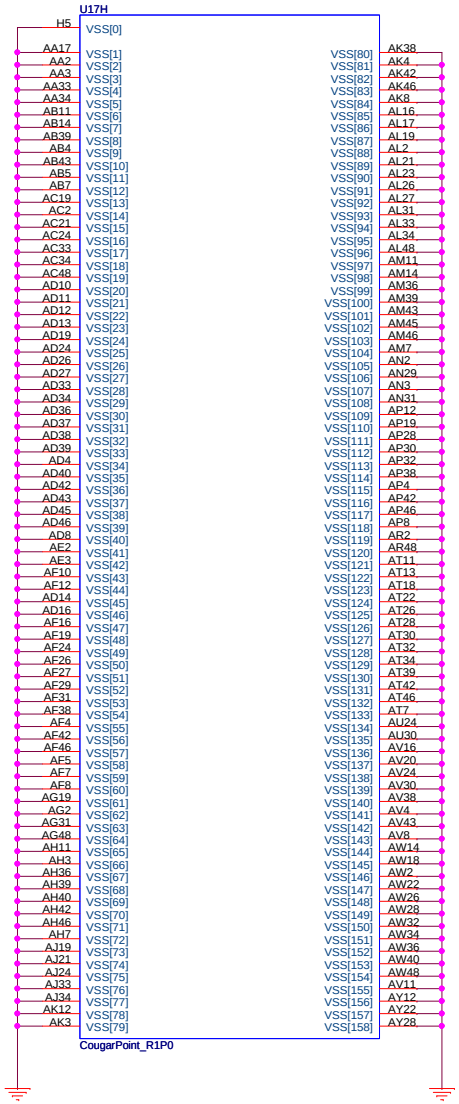
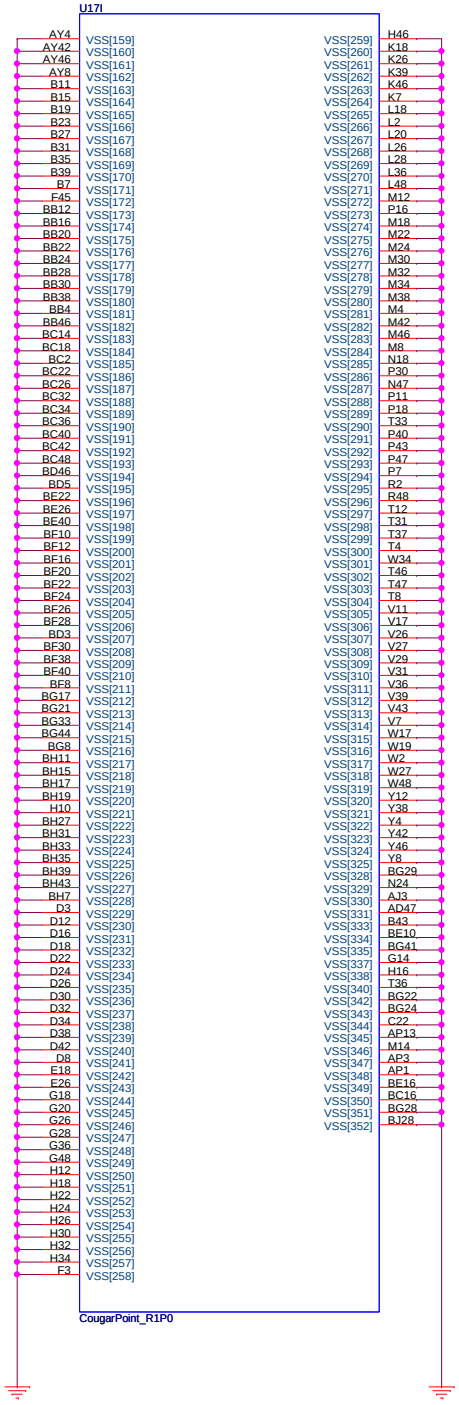
Schematics_ForFree

IBEX PEAK-M (GND)





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Quanta Computer Inc.		
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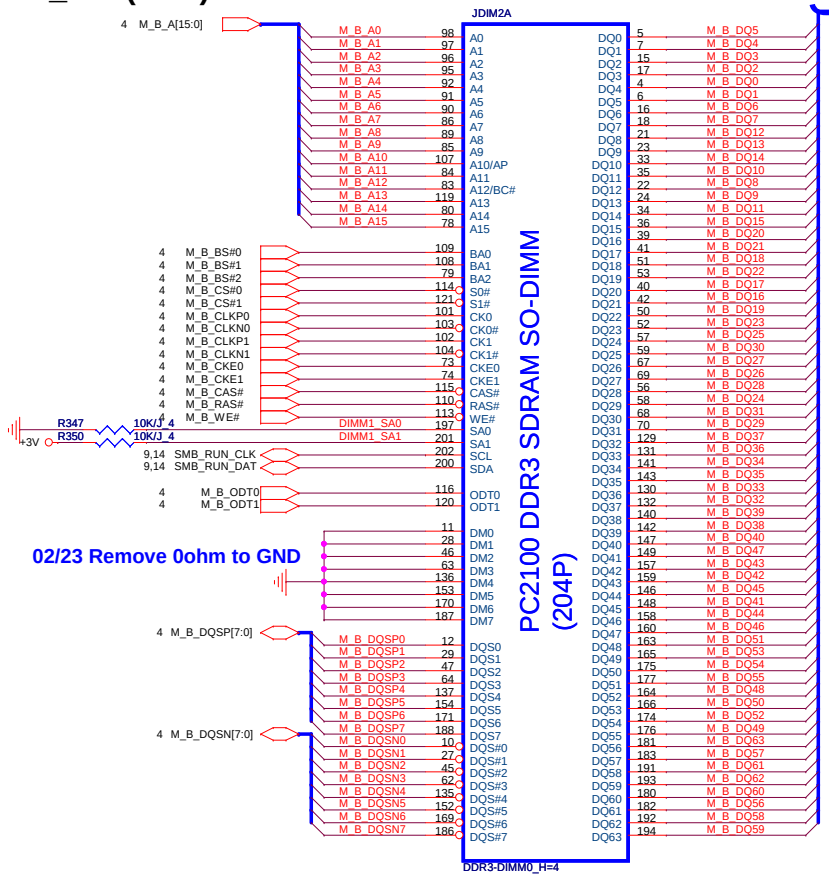
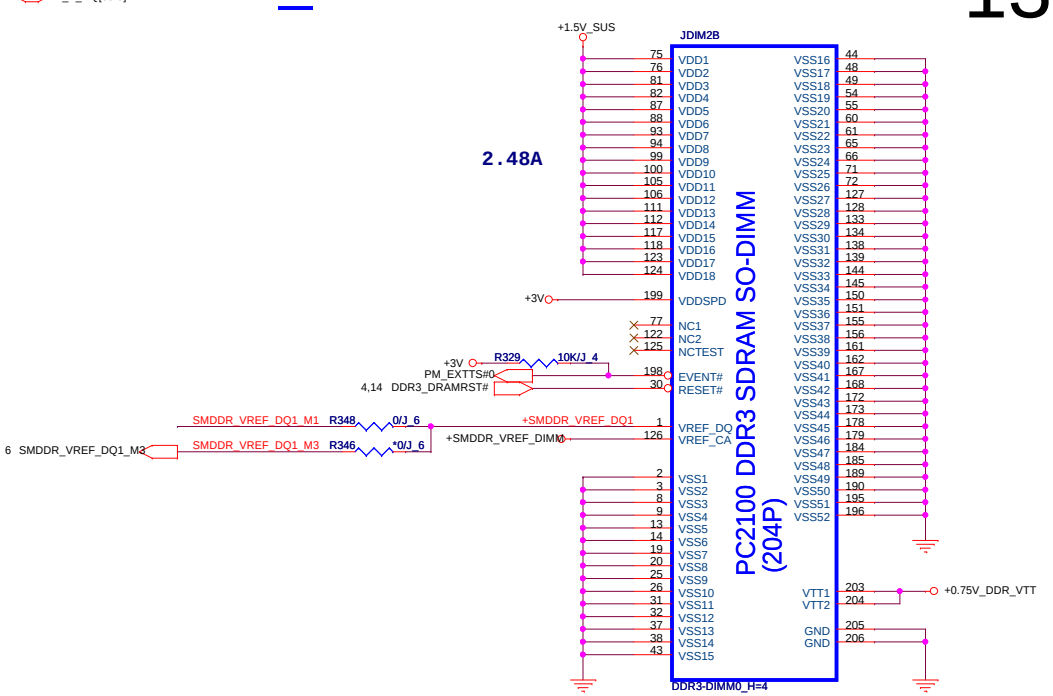
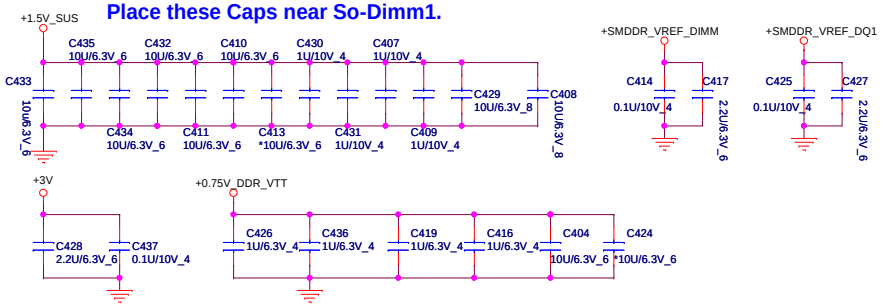
Schematics_ForFree



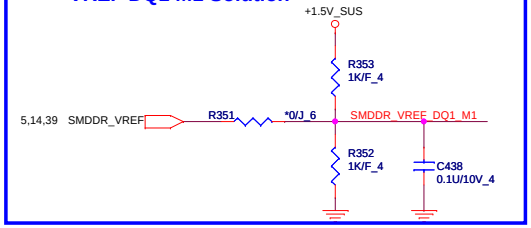


Place these Caps near So-Dimm1.



VREF DQ1 M2 Solution

VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

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	DDRIII SO-DIMM-0	1A

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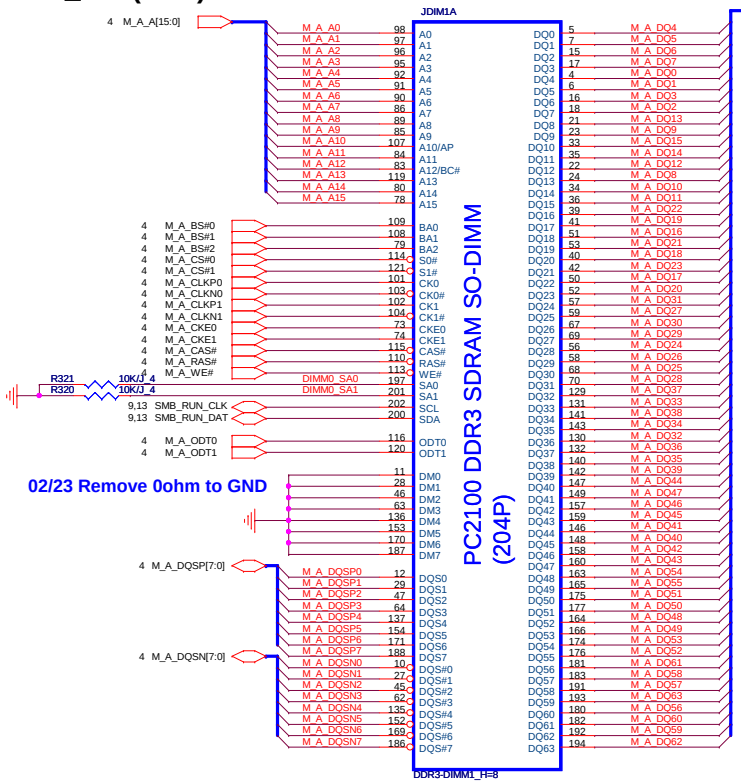
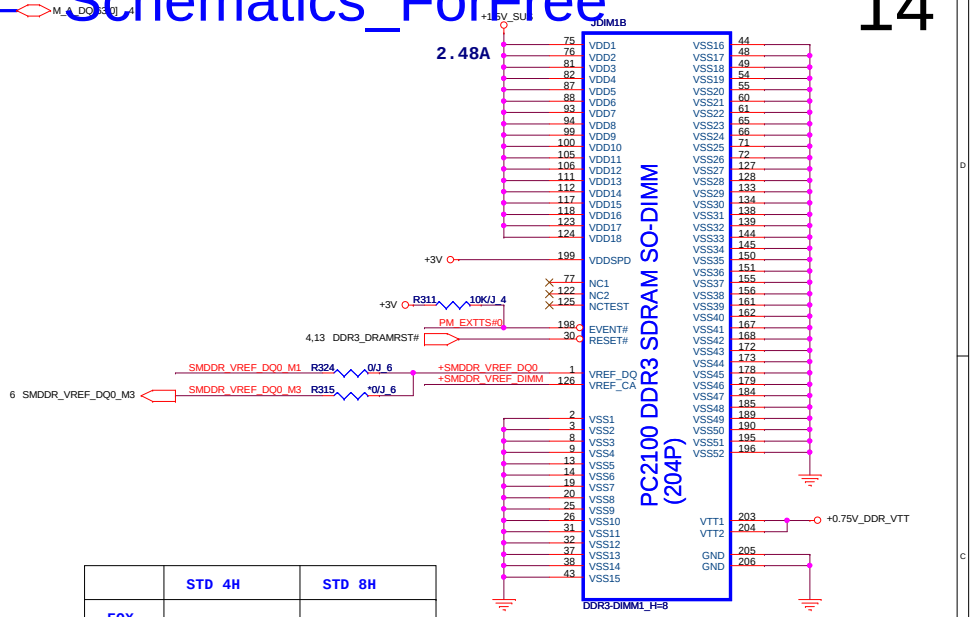
Schematics_ForFree

DDR_STD(DDR)



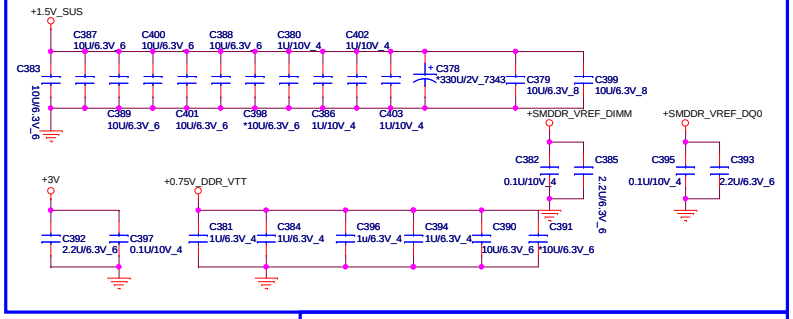
02/23 Remove 0ohm to GND

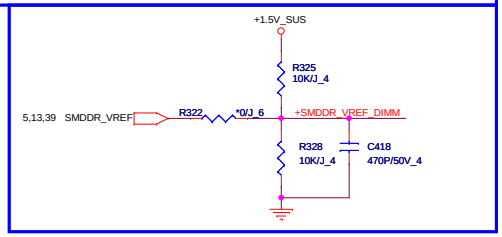


	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

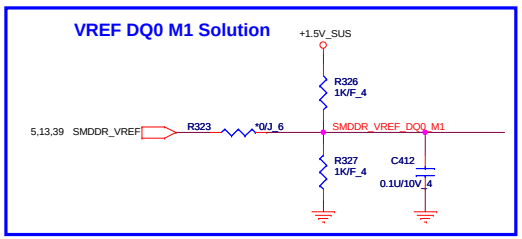
VREF DQ0 M2 Solution

Place these Caps near So-Dimm0.





VREF DQ0 M1 Solution



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Quanta Computer Inc.

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	DDRIII SO-DIMM-1	1A
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Schematics_ForFree

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

0.5A

+1.05V_GFX_PCIE

C171 0.1U/10V_4
C167 0.1U/10V_4
C172 1U/6.3V_4
C173 1U/6.3V_4
C216 4.7U/6.3V_6
C201 10U/6.3V_8
C213 22U/6.3V_8

1.6A

+1.05V_GFX_PCIE

C169 0.1U/10V_4
C154 0.1U/10V_4
C155 1U/6.3V_4
C156 1U/6.3V_4
C166 4.7U/6.3V_6
C195 10U/6.3V_8
C212 22U/6.3V_8

CAP CLOSE TO BGA

U28A
fcbga973-nvidia-n12p-ge
COMMON

AK16 PEX_IOVDD_1
AK17 PEX_IOVDD_2
AK21 PEX_IOVDD_3
AK24 PEX_IOVDD_4
AK27 PEX_IOVDD_5

AG11 PEX_IOVDDQ_1
AG12 PEX_IOVDDQ_2
AG13 PEX_IOVDDQ_3
AG15 PEX_IOVDDQ_4
AG16 PEX_IOVDDQ_5
AG17 PEX_IOVDDQ_6
AG18 PEX_IOVDDQ_7
AG22 PEX_IOVDDQ_8
AG23 PEX_IOVDDQ_9
AG24 PEX_IOVDDQ_10
AG25 PEX_IOVDDQ_11
AG26 PEX_IOVDDQ_12
AJ14 PEX_IOVDDQ_13
AJ15 PEX_IOVDDQ_14
AJ19 PEX_IOVDDQ_15
AJ21 PEX_IOVDDQ_16
AJ22 PEX_IOVDDQ_17
AJ24 PEX_IOVDDQ_18
AJ25 PEX_IOVDDQ_19
AJ27 PEX_IOVDDQ_20
AK18 PEX_IOVDDQ_21
AK20 PEX_IOVDDQ_22
AK23 PEX_IOVDDQ_23
AK26 PEX_IOVDDQ_24
AL16 PEX_IOVDDQ_25

+3V_GPU

C107 4.7U/6.3V_6
C93 1U/6.3V_4
C82 0.1U/10V_4
C86 0.1U/10V_4
C97 0.1U/10V_4

J10 VDD33_1
J11 VDD33_2
J12 VDD33_3
J13 VDD33_4
J9 VDD33_5

GFX_CORE

AD20 VDD_SENSE
D35 NC_9/ VDD_SENSE
P7 NC_16/ VDD_SENSE

12~16 mils width for 110mA

AD19 GND_SENSE
E35 NC_10/ GND_SENSE
R7 NC_17/ GND_SENSE

+1.05V_GFX_PCIE

L15 BLM18PG121SN
C196 0.1U/10V_4
C187 1U/6.3V_4
C200 4.7U/6.3V_6

+PEX_PLLVDD

AG14 PEX_PLLVDD

12~16 mils width

+3V_GPU

L1 0/J_6 +PEX_SVDD_3V3

AG19 PEX_CAL_PD_VDDQ/ PEX_SVDD_3V3
F7 NC_12/ PEX_SVDD_3V3

C64 1U/6.3V_4
C153 0.1U/10V_4
C76 4.7U/6.3V_6

AG20 PEX_CAL_PU_GND/ NC
A2 NC_1
AB7 NC_2
AD6 NC_3
AF6 NC_4
AG6 NC_5
AJ5 NC_6
AK15 NC_7
AL7 NC_8
E7 NC_11
H32 NC_13
M7 NC_14
P6 NC_15
U7 NC_18
V6 NC_19

R60 *10K/J_4 PGOOD

R420 *40.2K/F_4 MULTI_STRAP_REF2_GND

PCI EXPRESS

PEX_RX0 AP17
PEX_RX0* AN17
PEX_RX1 AN19
PEX_RX1* AP19
PEX_RX2 AR19
PEX_RX2* AR20
PEX_RX3 AP20
PEX_RX3* AN20
PEX_RX4 AN22
PEX_RX4* AP22
PEX_RX5 AR22
PEX_RX5* AR23
PEX_RX6 AP23
PEX_RX6* AN23
PEX_RX7 AN25
PEX_RX7* AP25
PEX_RX8 AR25
PEX_RX8* AR26
PEX_RX9 AP26
PEX_RX9* AN26
PEX_RX10 AN28
PEX_RX10* AP28
PEX_RX11 AR28
PEX_RX11* AR29
PEX_RX12 AP29
PEX_RX12* AN29
PEX_RX13 AN31
PEX_RX13* AP31
PEX_RX14 AR31
PEX_RX14* AR32
PEX_RX15 AP32
PEX_RX15* AP34

PEG_TXP15 3
PEG_TXN15 3
PEG_TXP14 3
PEG_TXN14 3
PEG_TXP13 3
PEG_TXN13 3
PEG_TXP12 3
PEG_TXN12 3
PEG_TXP11 3
PEG_TXN11 3
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PEG_TXN10 3
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PEG_TXP5 3
PEG_TXN5 3
PEG_TXP4 3
PEG_TXN4 3
PEG_TXP3 3
PEG_TXN3 3
PEG_TXP2 3
PEG_TXN2 3
PEG_TXP1 3
PEG_TXN1 3
PEG_TXP0 3
PEG_TXN0 3

PEX_TX0 AL17 PEG_RXP15_C C260 0.1U/10V_4
PEX_TX0* AM17 PEG_RXN15_C C259 0.1U/10V_4
PEX_TX1 AM18 PEG_RXP14_C C231 0.1U/10V_4
PEX_TX1* AM19 PEG_RXN14_C C232 0.1U/10V_4
PEX_TX2 AL19 PEG_RXP13_C C258 0.1U/10V_4
PEX_TX2* AK19 PEG_RXN13_C C257 0.1U/10V_4
PEX_TX3 AL20 PEG_RXP12_C C230 0.1U/10V_4
PEX_TX3* AM20 PEG_RXN12_C C229 0.1U/10V_4
PEX_TX4 AM21 PEG_RXP11_C C255 0.1U/10V_4
PEX_TX4* AM22 PEG_RXN11_C C256 0.1U/10V_4
PEX_TX5 AL22 PEG_RXP10_C C228 0.1U/10V_4
PEX_TX5* AK22 PEG_RXN10_C C227 0.1U/10V_4
PEX_TX6 AL23 PEG_RXP9_C C254 0.1U/10V_4
PEX_TX6* AM23 PEG_RXN9_C C253 0.1U/10V_4
PEX_TX7 AM24 PEG_RXP8_C C226 0.1U/10V_4
PEX_TX7* AM25 PEG_RXN8_C C225 0.1U/10V_4
PEX_TX8 AL25 PEG_RXP7_C C252 0.1U/10V_4
PEX_TX8* AK25 PEG_RXN7_C C251 0.1U/10V_4
PEX_TX9 AL26 PEG_RXP6_C C224 0.1U/10V_4
PEX_TX9* AM26 PEG_RXN6_C C223 0.1U/10V_4
PEX_TX10 AM27 PEG_RXP5_C C250 0.1U/10V_4
PEX_TX10* AM28 PEG_RXN5_C C249 0.1U/10V_4
PEX_TX11 AL28 PEG_RXP4_C C222 0.1U/10V_4
PEX_TX11* AK28 PEG_RXN4_C C221 0.1U/10V_4
PEX_TX12 AK29 PEG_RXP3_C C219 0.1U/10V_4
PEX_TX12* AL29 PEG_RXN3_C C220 0.1U/10V_4
PEX_TX13 AM29 PEG_RXP2_C C248 0.1U/10V_4
PEX_TX13* AM30 PEG_RXN2_C C247 0.1U/10V_4
PEX_TX14 AM31 PEG_RXP1_C C218 0.1U/10V_4
PEX_TX14* AM32 PEG_RXN1_C C217 0.1U/10V_4
PEX_TX15 AN32 PEG_RXP0_C C245 0.1U/10V_4
PEX_TX15* AP32 PEG_RXN0_C C246 0.1U/10V_4

PEG_RXP15 3
PEG_RXN15 3
PEG_RXP14 3
PEG_RXN14 3
PEG_RXP13 3
PEG_RXN13 3
PEG_RXP12 3
PEG_RXN12 3
PEG_RXP11 3
PEG_RXN11 3
PEG_RXP10 3
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PEG_RXP9 3
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PEG_RXP8 3
PEG_RXN8 3
PEG_RXP7 3
PEG_RXN7 3
PEG_RXP6 3
PEG_RXN6 3
PEG_RXP5 3
PEG_RXN5 3
PEG_RXP4 3
PEG_RXN4 3
PEG_RXP3 3
PEG_RXN3 3
PEG_RXP2 3
PEG_RXN2 3
PEG_RXP1 3
PEG_RXN1 3
PEG_RXP0 3
PEG_RXN0 3

PEX_REFCLK AR16 CLK_PCIE_VGAP 9
PEX_REFCLK* AR17 CLK_PCIE_VGAN 9

PEX_TSTCLK_OUT AJ17 PEX_TSTCLK R90 *200/J_4
PEX_TSTCLK_OUT* AJ18 PEX_TSTCLK#

PEX_RST* AM16 VGA_RST# R435 *0_4_short GPU_RST# GPU_RST# 9

R441 1 2 100K/J_4

PEX_CLKREQ* AR13 R468 10K/J_4 +3V_GPU PEX_CLKREQ# 9

PEX_TERMP AG21 PEX_TERMP R79 2.49K/F_4

TESTMODE AP35 TESTMODE R141 10K/J_4

+3V_GPU
+3V
R104 EV@10K/F_4
R85 EV@10K/F_4
GFXPG 9,10
Q19 MMBT3904

+1.8V_GPU R101 EV@10K/F_4
*EV@1000P/50V/X7R_4@NC C197
R80 *EV@0_4
Q17 PDTC143TT

+1.5V_GPU R72 EV@10K/F_4
*EV@1000P/50V/X7R_4@NC C147
Q12 PDTC143TT

For power-down sequency

+3V_GPU +1.5V_GPU +3V_GPU GFX_CORE
D6 RB500V-40
D5 RB500V-40

The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

- NVVDD <= VDD33+0.5 V
- FBVDDQ <= VDD33+0.5 V

9,39,42 GFXON

R107 0/J_4
C179 *1U/6.3V_4

+1.05V_GFX_PCIE +3V
R102 *100K/F_4
R109 *390/F_4
R112 *8.2K_4
Q21 *MMBT3904
Q20 *ME2N7002E
+3V_GPU_EN
+3V_GPU_EN 44

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(PCIe)	1A
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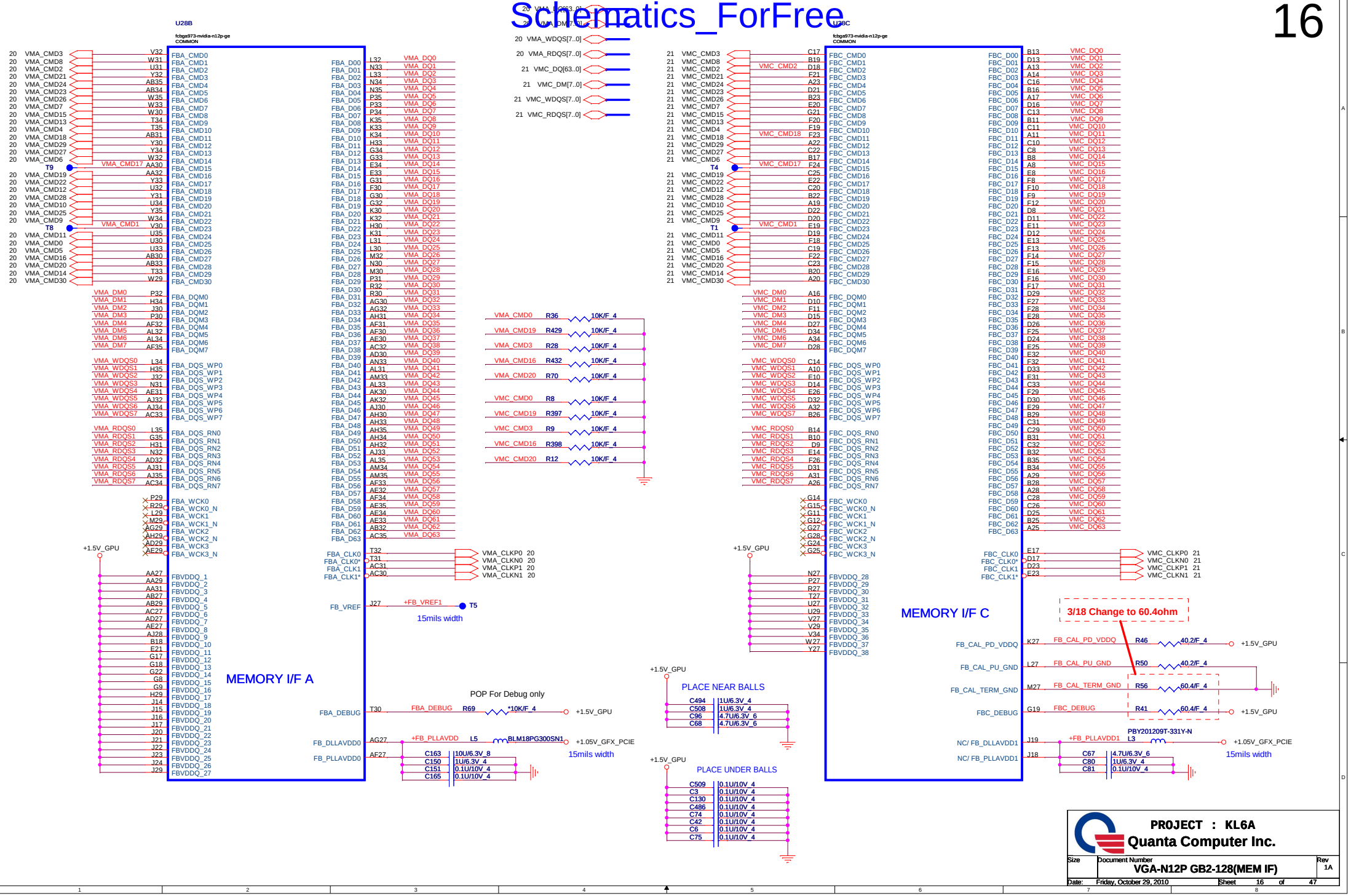
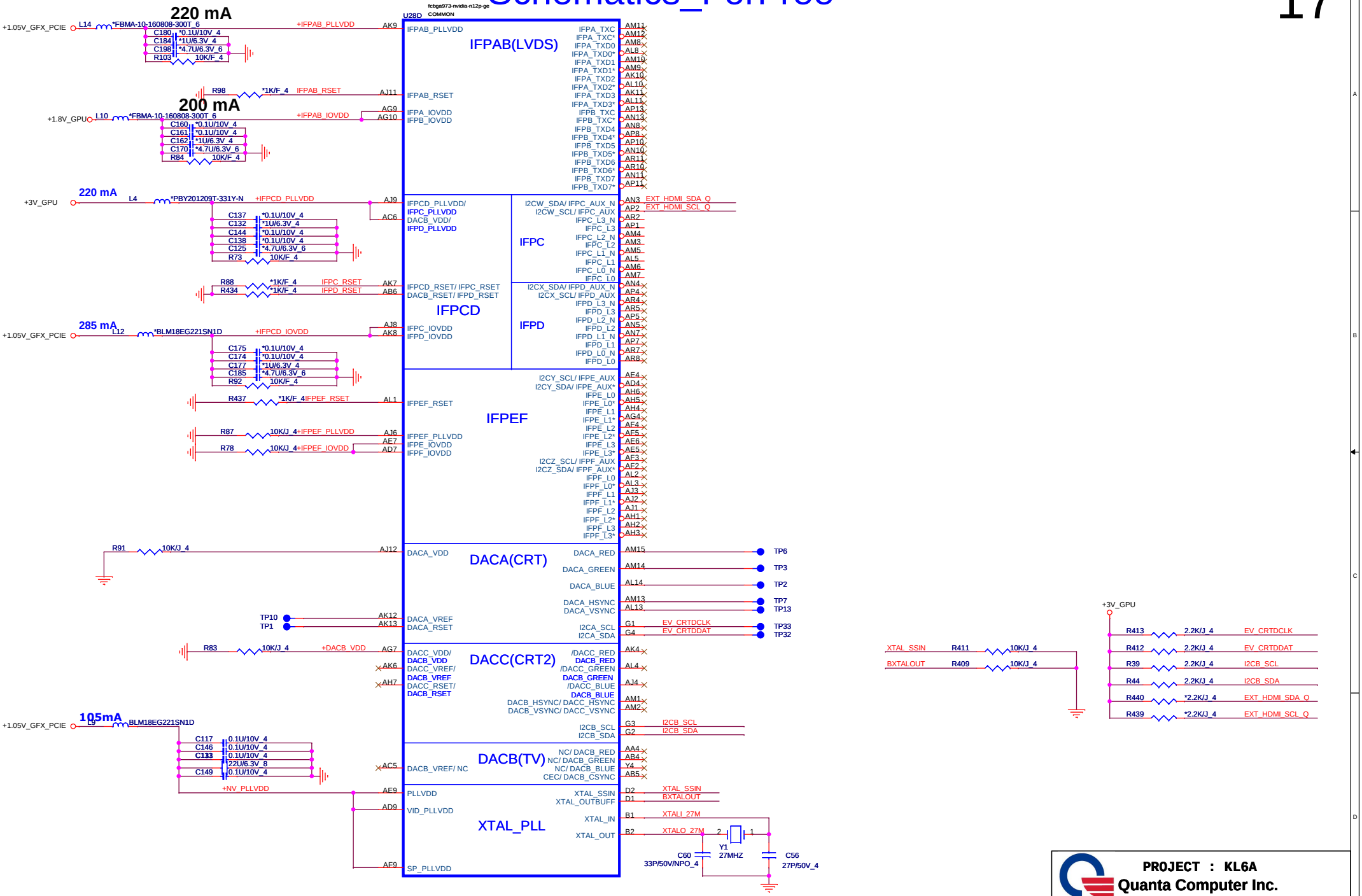
Schematics_ForFree



4/28 Enable LVDS For 3DV



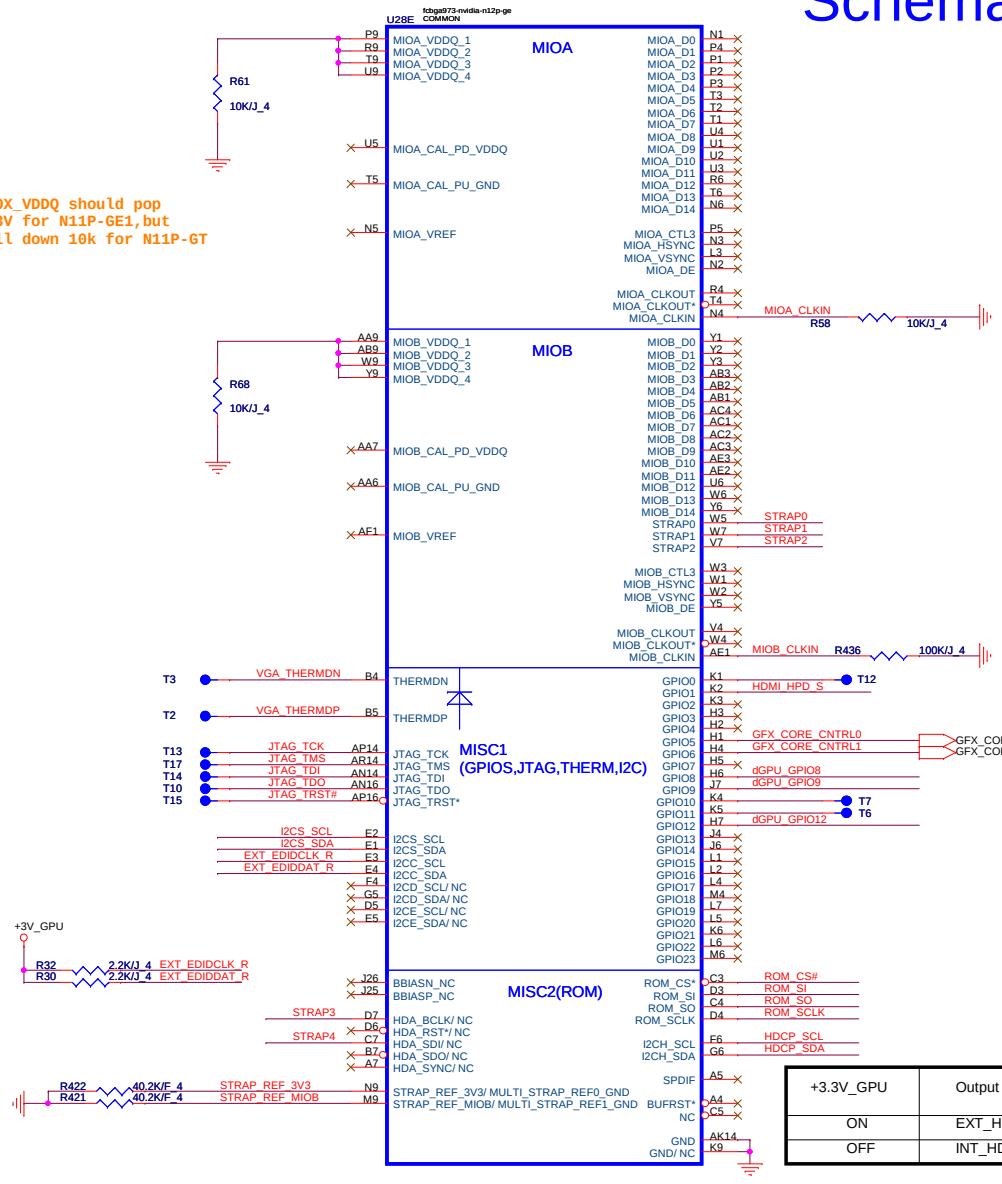
PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(Display)	1A
Date: Friday, October 29, 2010	Sheet 17 of 47	

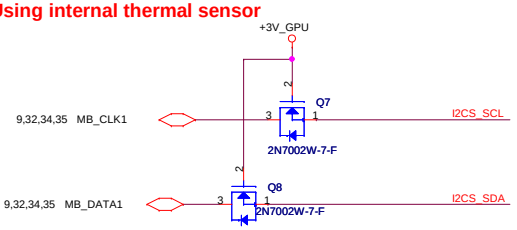
Schematics_ForFree

MIOX_VDDQ should pop
3.3V for N11P-GE1,but
pull down 10k for N11P-GT



+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP

Using internal thermal sensor



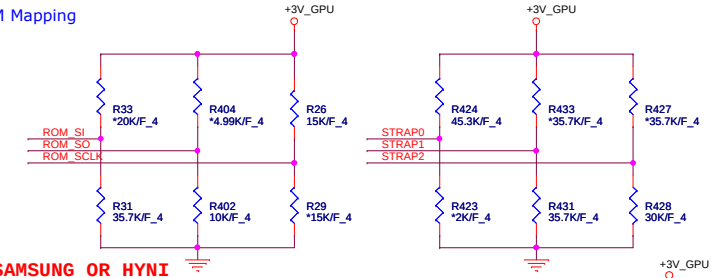
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0101
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW01	AKD5LZWTW00	H5TQ1G63BFR-11C
0x6(0110)	800MHz 2GB(128M*16) Hynix	AKD5MGGTW00	AKD5MGGTW06	H5TQ2G63BFR-12C
0x7(0111)	800MHz 2GB(128M*16) Samsung	AKD5MGGT501	AKD5MGGT507	K4W2G1646B-HC12
0x6(0110)	900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

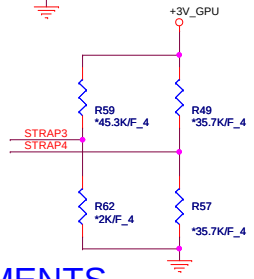
ROM_SI Strap Bit for RAM Mapping

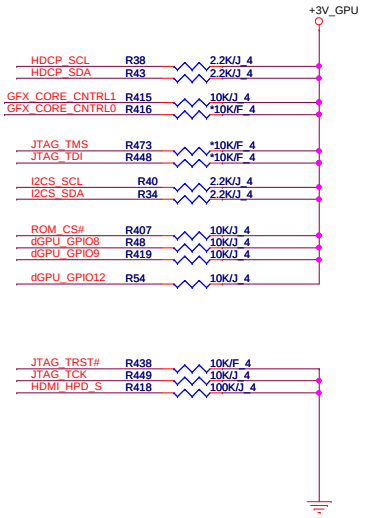
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

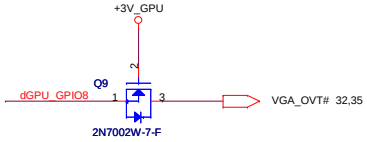


SAMSUNG OR HYNI

N12P-GE ROM_SO 10K pull low
Strap2 30K pull low
N12P-GV1 ROM_SO 10K pull low
Strap2 45K pull low
N12P-GV ROM_SO 10K pull high
Strap2 45K pull high
Strap3 5K pull low
Strap4 20K pull low







GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	N/A	
3	OUT	N/A	
4	OUT	N/A	
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(GPIO/STRAP)	1A

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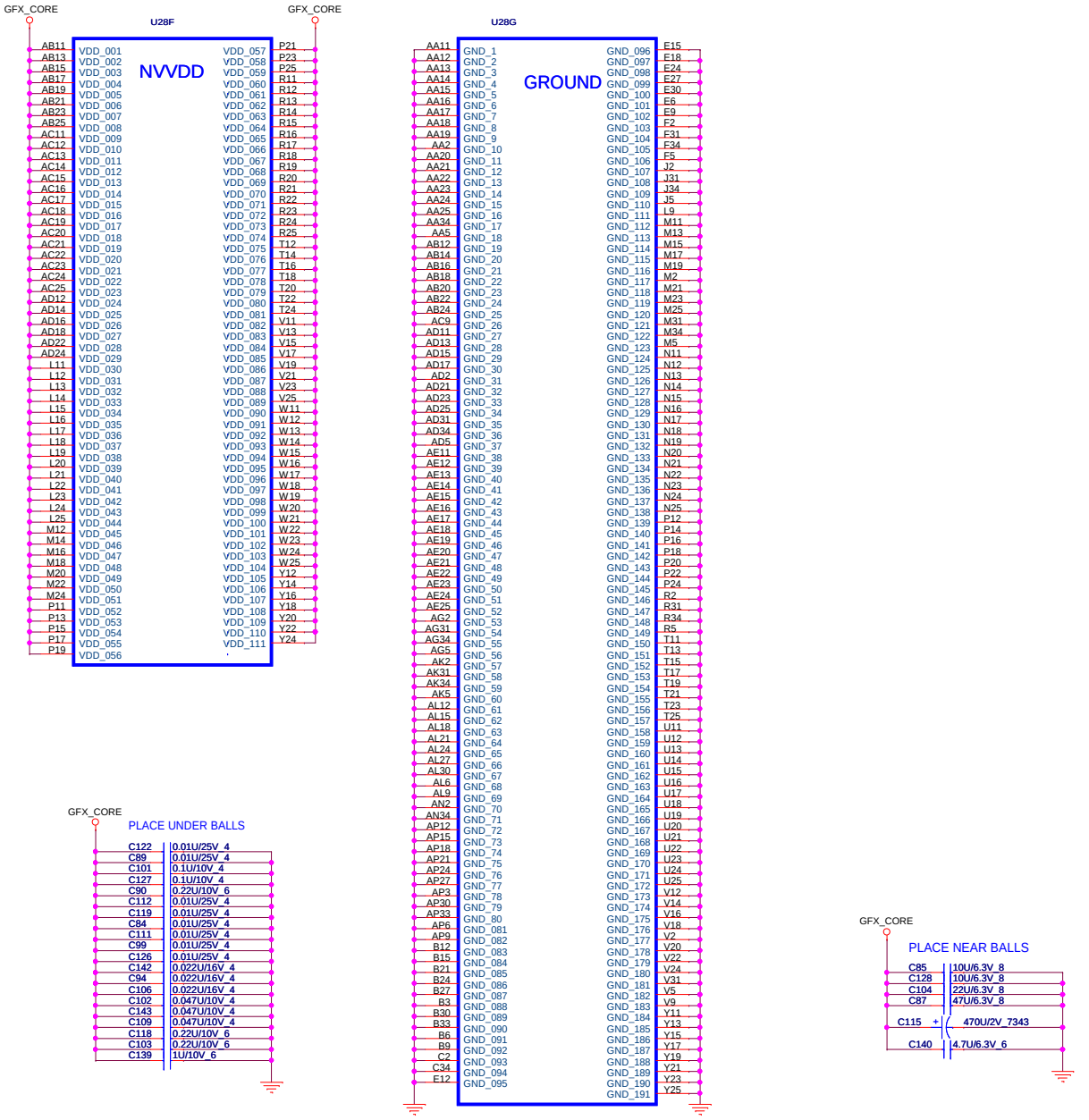

PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(POWER)	1A

Date: Friday, October 29, 2010 Sheet 19 of 47

Schematics ForFree

CHANNEL A: 512MB/1024MB DDR3

16 VMA_DQ[63..0]
16 VMA_DM[7..0]
16 VMA_WDQS[7..0]
16 VMA_RDQS[7..0]

U4 / U27 / U7 / U29 — 96-BALL SDRAM DDR3 K4W1G1646E-HC11

Should be 240 Ohms +-1%

R67 240/F_4 · R410 240/F_4 · R97 240/F_4 · R430 240/F_4

+1.5V_GPU

R417 1.33K/F_4 · R414 1.33K/F_4 · C518 0.01U/25V_4
R52 1.33K/F_4 · R45 1.33K/F_4 · C70 0.01U/25V_4
C123 *10U/6.3V_6
R77 1.33K/F_4 · R86 1.33K/F_4 · C159 0.01U/25V_4
R425 1.33K/F_4 · R426 1.33K/F_4 · C529 0.01U/25V_4

Placement has to be close to VRAM

R405 162/F_4 · R95 162/F_4

C528 C65 C168 C145 C531 C186 C7 C15 C234 C235 C133 C535 — 1U/6.3V_4 / 0.1U/10V_4
C572 C526 C527 C533 C532 C71 C523 C524 C574 C573 C236 C194 — 1U/6.3V_4 / 0.1U/10V_4
C32 C48 C52 C55 C507 C100 C525 C59 C88 C58 C114 C176 — 1U/6.3V_4 / 0.1U/10V_4
C510 C520 C513 C514 C72 C4 C5 C515 C519 C522 C183 C516 — 1U/6.3V_4 / 0.1U/10V_4

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(VRAM-1)	1A

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Schematics For Free

CHANNEL B: 512MB 128MB DDR3

16 VMC_DQ[63..0]
16 VMC_DM[7..0]
16 VMC_WDQS[7..0]
16 VMC_RDQS[7..0]

U2 — K4W1G1646E-HC11 (96-BALL SDRAM DDR3)

VREFC_VMC1 M8 — VREFCA
VREFD_VMC1 H1 — VREFDQ

DQ0 E3 VMC_DQ21
DQ1 F7 VMC_DQ20
DQ2 F2 VMC_DQ17
DQ3 F8 VMC_DQ22
DQ4 H8 VMC_DQ16
DQ5 G2 VMC_DQ18
DQ6 H7 VMC_DQ19
DQ7 VMC_DQ23

16 VMC_CMD7 N3 — A0
16 VMC_CMD10 P7 — A1
16 VMC_CMD24 P3 — A2
16 VMC_CMD6 N2 — A3
16 VMC_CMD22 P8 — A4
16 VMC_CMD26 P2 — A5
16 VMC_CMD5 R8 — A6
16 VMC_CMD21 R2 — A7
16 VMC_CMD8 T8 — A8
16 VMC_CMD4 R3 — A9
16 VMC_CMD25 L7 — A10/AP
16 VMC_CMD23 R7 — A11
16 VMC_CMD9 N7 — A12/BC
16 VMC_CMD12 T3 — A13
16 VMC_CMD14 T7 — A14
16 VMC_CMD30 M7 — A15

D7 VMC_DQ7
C3 VMC_DQ0
C8 VMC_DQ4
C2 VMC_DQ2
A7 VMC_DQ5
A2 VMC_DQ1
B8 VMC_DQ6
A3 VMC_DQ3
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7

16 VMC_CMD29 M2 — BA0
16 VMC_CMD13 N8 — BA1
16 VMC_CMD27 M3 — BA2

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GPU

16 VMC_CLKP0 J7 — CK
16 VMC_CLKN0 K7 — CK
16 VMC_CMD3 K9 — CKE

16 VMC_CMD0 K1 — ODT
16 VMC_CMD2 L2 — CS
16 VMC_CMD11 J3 — RAS
16 VMC_CMD15 K3 — CAS
16 VMC_CMD28 L3 — WE

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VMC_WDQS2 F3 — DQSL
VMC_RDQS2 G3 — DQSL

VMC_DM2 E7 — DML
VMC_DM0 D3 — DMU

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VMC_WDQS0 C7 — DQSU
VMC_RDQS0 B7 — DQSU

16 VMC_CMD20 — VMC_CMD20 T2 — RESET
VMC_ZQ1 L8 — ZQ

Should be 240 Ohms +-1%
R23 240/F_4

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

U25 — K4W1G1646E-HC11 (96-BALL SDRAM DDR3)

VREFC_VMC1 M8 — VREFCA
VREFD_VMC1 H1 — VREFDQ

DQ0 E3 VMC_DQ24
DQ1 F7 VMC_DQ25
DQ2 F2 VMC_DQ28
DQ3 F8 VMC_DQ26
DQ4 H3 VMC_DQ31
DQ5 G2 VMC_DQ29
DQ6 H7 VMC_DQ27
DQ7

VMC_CMD7 N3 — A0
VMC_CMD10 P7 — A1
VMC_CMD24 P3 — A2
VMC_CMD6 N2 — A3
VMC_CMD22 P8 — A4
VMC_CMD26 P2 — A5
VMC_CMD5 R8 — A6
VMC_CMD21 R2 — A7
VMC_CMD8 T8 — A8
VMC_CMD4 R3 — A9
VMC_CMD25 L7 — A10/AP
VMC_CMD23 R7 — A11
VMC_CMD9 N7 — A12/BC
VMC_CMD12 T3 — A13
VMC_CMD14 T7 — A14
VMC_CMD30 M7 — A15

D7 VMC_DQ13
C3 VMC_DQ10
C8 VMC_DQ15
C2 VMC_DQ8
A7 VMC_DQ12
A2 VMC_DQ9
B8 VMC_DQ14
A3 VMC_DQ11
DQU0
DQU1
DQU2
DQU3
DQU4
DQU5
DQU6
DQU7

VMC_CMD29 M2 — BA0
VMC_CMD13 N8 — BA1
VMC_CMD27 M3 — BA2

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GPU

VMC_CLKP0 J7 — CK
VMC_CLKN0 K7 — CK
VMC_CMD3 K9 — CKE

VMC_CMD0 K1 — ODT
VMC_CMD2 L2 — CS
VMC_CMD11 J3 — RAS
VMC_CMD15 K3 — CAS
VMC_CMD28 L3 — WE

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VMC_WDQS3 F3 — DQSL
VMC_RDQS3 G3 — DQSL

VMC_DM3 E7 — DML
VMC_DM1 D3 — DMU

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VMC_WDQS1 C7 — DQSU
VMC_RDQS1 B7 — DQSU

VMC_CMD20 T2 — RESET
VMC_ZQ2 L8 — ZQ

Should be 240 Ohms +-1%
R393 240/F_4

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

U3 — K4W1G1646E-HC11 (96-BALL SDRAM DDR3)

VREFC_VMC3 M8 — VREFCA
VREFD_VMC3 H1 — VREFDQ

DQ0 E3 VMC_DQ37
DQ1 F7 VMC_DQ36
DQ2 F2 VMC_DQ33
DQ3 F8 VMC_DQ32
DQ4 H3 VMC_DQ38
DQ5 G2 VMC_DQ39
DQ6 H7 VMC_DQ34
DQ7

VMC_CMD9 N3 — A0
VMC_CMD24 P7 — A1
VMC_CMD10 P3 — A2
VMC_CMD13 N2 — A3
VMC_CMD26 P8 — A4
VMC_CMD22 P2 — A5
VMC_CMD21 R8 — A6
VMC_CMD5 R2 — A7
VMC_CMD8 T8 — A8
VMC_CMD23 R3 — A9
VMC_CMD28 L7 — A10/AP
VMC_CMD4 R7 — A11
VMC_CMD7 N7 — A12/BC
VMC_CMD14 T3 — A13
VMC_CMD12 T7 — A14
VMC_CMD27 M7 — A15

D7 VMC_DQ44
C3 VMC_DQ46
C8 VMC_DQ40
C2 VMC_DQ45
A7 VMC_DQ42
A2 VMC_DQ47
B8 VMC_DQ41
A3 VMC_DQ43
DQU0
DQU1
DQU2
DQU3
DQU4
DQU5
DQU6
DQU7

VMC_CMD29 M2 — BA0
VMC_CMD6 N8 — BA1
VMC_CMD30 M3 — BA2

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GPU

16 VMC_CLKP1 J7 — CK
16 VMC_CLKN1 K7 — CK
16 VMC_CMD16 K9 — CKE

16 VMC_CMD19 K1 — ODT
16 VMC_CMD18 L2 — CS
VMC_CMD11 J3 — RAS
VMC_CMD15 K3 — CAS
VMC_CMD25 L3 — WE

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VMC_WDQS4 F3 — DQSL
VMC_RDQS4 G3 — DQSL

VMC_DM4 E7 — DML
VMC_DM5 D3 — DMU

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VMC_WDQS5 C7 — DQSU
VMC_RDQS5 B7 — DQSU

VMC_CMD20 T2 — RESET
VMC_ZQ3 L8 — ZQ

Should be 240 Ohms +-1%
R10 240/F_4

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

U26 — K4W1G1646E-HC11 (96-BALL SDRAM DDR3)

VREFC_VMC3 M8 — VREFCA
VREFD_VMC3 H1 — VREFDQ

DQ0 E3 VMC_DQ56
DQ1 F7 VMC_DQ60
DQ2 F2 VMC_DQ59
DQ3 F8 VMC_DQ61
DQ4 H8 VMC_DQ58
DQ5 G2 VMC_DQ62
DQ6 H7 VMC_DQ57
DQ7 VMC_DQ63

VMC_CMD9 N3 — A0
VMC_CMD24 P7 — A1
VMC_CMD10 P3 — A2
VMC_CMD13 N2 — A3
VMC_CMD26 P8 — A4
VMC_CMD22 P2 — A5
VMC_CMD21 R8 — A6
VMC_CMD5 R2 — A7
VMC_CMD8 T8 — A8
VMC_CMD23 R3 — A9
VMC_CMD28 L7 — A10/AP
VMC_CMD4 R7 — A11
VMC_CMD7 N7 — A12/BC
VMC_CMD14 T3 — A13
VMC_CMD12 T7 — A14
VMC_CMD27 M7 — A15

D7 VMC_DQ48
C3 VMC_DQ53
C8 VMC_DQ50
C2 VMC_DQ54
A7 VMC_DQ51
A2 VMC_DQ52
B8 VMC_DQ49
A3 VMC_DQ55
DQU0
DQU1
DQU2
DQU3
DQU4
DQU5
DQU6
DQU7

VMC_CMD29 M2 — BA0
VMC_CMD6 N8 — BA1
VMC_CMD30 M3 — BA2

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GPU

VMC_CLKP1 J7 — CK
VMC_CLKN1 K7 — CK
VMC_CMD16 K9 — CKE

VMC_CMD19 K1 — ODT
VMC_CMD18 L2 — CS
VMC_CMD11 J3 — RAS
VMC_CMD15 K3 — CAS
VMC_CMD25 L3 — WE

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VMC_WDQS7 F3 — DQSL
VMC_RDQS7 G3 — DQSL

VMC_DM7 E7 — DML
VMC_DM6 D3 — DMU

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VMC_WDQS6 C7 — DQSU
VMC_RDQS6 B7 — DQSU

VMC_CMD20 T2 — RESET
VMC_ZQ4 L8 — ZQ

Should be 240 Ohms +-1%
R20 240/F_4

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

+1.5V_GPU
R395 1.33K/F_4
15 mil width and <500 mil
VREFC_VMC1
R394 1.33K/F_4
C491 0.01U/25V_4

+1.5V_GPU
R6 1.33K/F_4
VREFD_VMC1
R7 1.33K/F_4
C9 0.01U/25V_4

+1.5V_GPU
C21 *10U/6.3V_6

+1.5V_GPU
R13 1.33K/F_4
VREFC_VMC3
R11 1.33K/F_4
C14 0.01U/25V_4

+1.5V_GPU
R399 1.33K/F_4
VREFD_VMC3
R396 1.33K/F_4
C497 0.01U/25V_4

Placement has to be close to VRAM

VMC_CLKP0
R400 162/F_4
VMC_CLKN0
VMC_CLKP1
R14 162/F_4
VMC_CLKN1
N12P-GE/GV1/GV ONLY

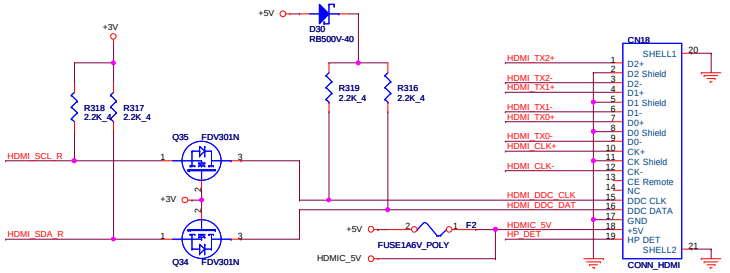
+1.5V_GPU
C24 1U/6.3V_4
C28 1U/6.3V_4
C25 1U/6.3V_4
C157 1U/6.3V_4
C30 1U/6.3V_4
C41 1U/6.3V_4
C110 1U/6.3V_4
C493 1U/6.3V_4
C51 0.1U/10V_4
C47 0.1U/10V_4
C44 0.1U/10V_4
C16 0.1U/10V_4

+1.5V_GPU
C498 1U/6.3V_4
C502 1U/6.3V_4
C506 1U/6.3V_4
C503 1U/6.3V_4
C35 1U/6.3V_4
C98 1U/6.3V_4
C105 1U/6.3V_4
C530 1U/6.3V_4
C45 0.1U/10V_4
C11 0.1U/10V_4
C489 0.1U/10V_4
C499 0.1U/10V_4

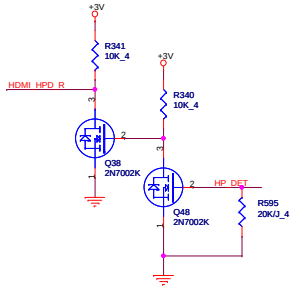
+1.5V_GPU
C13 1U/6.3V_4
C12 1U/6.3V_4
C39 1U/6.3V_4
C29 1U/6.3V_4
C78 1U/6.3V_4
C61 1U/6.3V_4
C108 1U/6.3V_4
C36 1U/6.3V_4
C495 0.1U/10V_4
C43 0.1U/10V_4
C40 0.1U/10V_4
C46 0.1U/10V_4

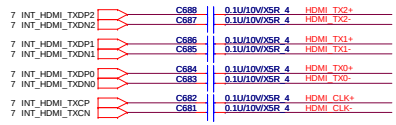
+1.5V_GPU
C490 1U/6.3V_4
C488 1U/6.3V_4
C487 1U/6.3V_4
C492 1U/6.3V_4
C121 1U/6.3V_4
C73 1U/6.3V_4
C33 1U/6.3V_4
C501 1U/6.3V_4
C505 0.1U/10V_4
C511 0.1U/10V_4
C38 0.1U/10V_4
C10 0.1U/10V_4

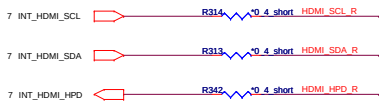
PROJECT : KL6A
Quanta Computer Inc.
Size
Document Number: VGA-N12P GB2-128(VRAM-2)
Rev: 1A
Date: Friday, October 29, 2010
Sheet 21 of 47

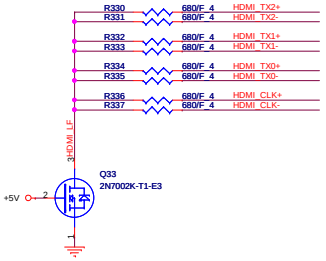


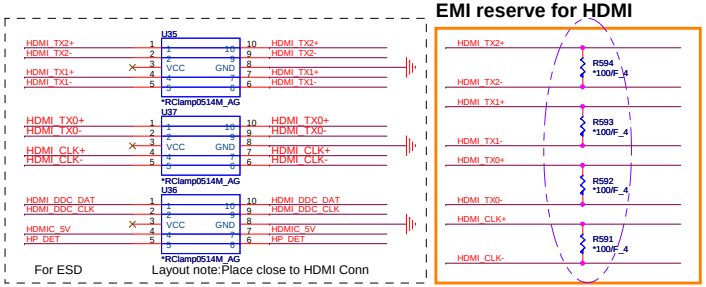
HDMI Hot-PLUG to EC and GPU











7,8,11,23,26,27,32,33,34,35,36,37,38,45 +5V
7,8,9,10,11,13,14,15,23,24,25,26,27,28,29,30,31,32,34,35,36,37,38,42,43,44,45 +3V

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

Date: Friday, October 29, 2010 Sheet 22 of 47

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

7 INT_CRT_RED
7 INT_CRT_GRE
7 INT_CRT_BLU

L23 BLM18BA470SN1
L22 BLM18BA470SN1
L21 BLM18BA470SN1

CRT_R1
CRT_G1
CRT_B1

R230 150/F_4
R225 150/F_4
R215 150/F_4

C305 5.6P/50V/COG_4
C291 5.6P/50V/COG_4
C285 5.6P/50V/COG_4
C284 5.6P/50V/COG_4
C292 5.6P/50V/COG_4
C306 5.6P/50V/COG_4

TP19

CRT_VCC
D26 RB500V-40
C617 0.1U/10V/X5R_4
+5V
F1 FUSE1A6V_POLY
C274 *VARISTOR_4
CRT_VCC_R

CN14 CRT_CONN

7 INT_CRT_VSYNC
7 INT_CRT_HSYNC

+5V
U14 AHCT1G125DCH
U16 AHCT1G125DCH
C286 0.1U/10V/X5R_4

VGAVSYNC_R
VGAHSYNC_R

R188 10_4
R203 10_4

Place near U37,U38 < 200 mil

CRTVSYNC1
CRTHSYNC1

C275 *10P/50V/COG_4
C265 *10P/50V/COG_4

L16 HB-1T1608-121JT
L20 HB-1T1608-121JT

CRTVSYNC
CRTHSYNC

C277 10P/50V/COG_4
C264 10P/50V/COG_4

Place near CN5002 connector < 200 mil

ESD PROTECTION

D21 *TVSS5VESPT — CRT_R1
D20 *TVSS5VESPT — CRT_G1
D18 *TVSS5VESPT — CRT_B1
D15 *TVSS5VESPT — CRTVSYNC
D16 *TVSS5VESPT — CRTHSYNC
D25 *TVSS5VESPT — DDCCLK
D27 *TVSS5VESPT — DDCDAT

+3V
R567 2.2K_4
R553 2.2K_4

CRT_VCC
R564 4.7K_4
R540 4.7K_4

7 INT_DDCCLK
7 INT_DDCDAT

Q43 2N7002K-T1-E3
Q44 2N7002K-T1-E3

DDCCLK
DDCDAT

C610 *10P/50V/COG_4
C587 *10P/50V/COG_4

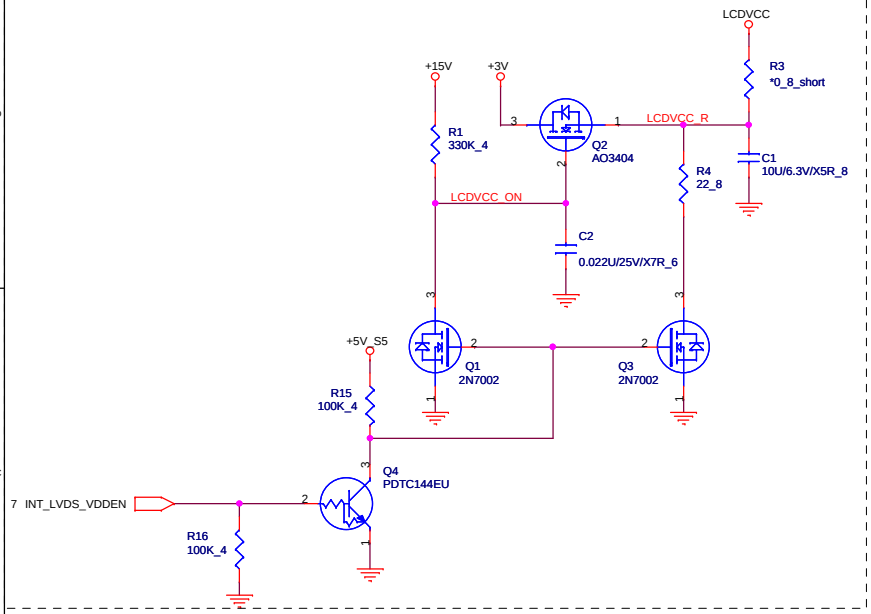
PROJECT : KL6A
Quanta Computer Inc.

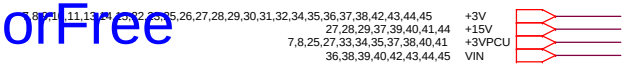
Size	Document Number	Rev
Custom	CRT CONN	1A

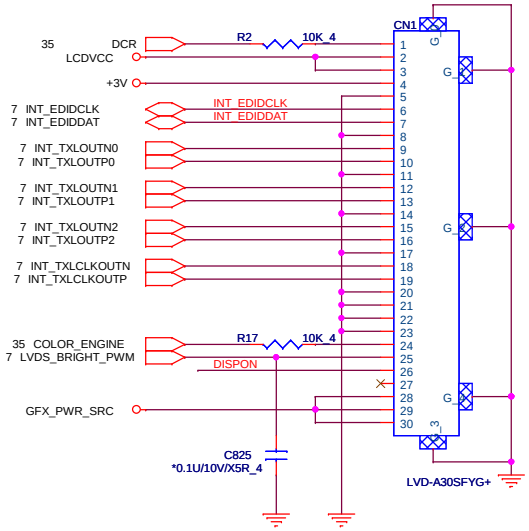
Date: Friday, October 29, 2010 Sheet 23 of 47

Schematics_ForFree

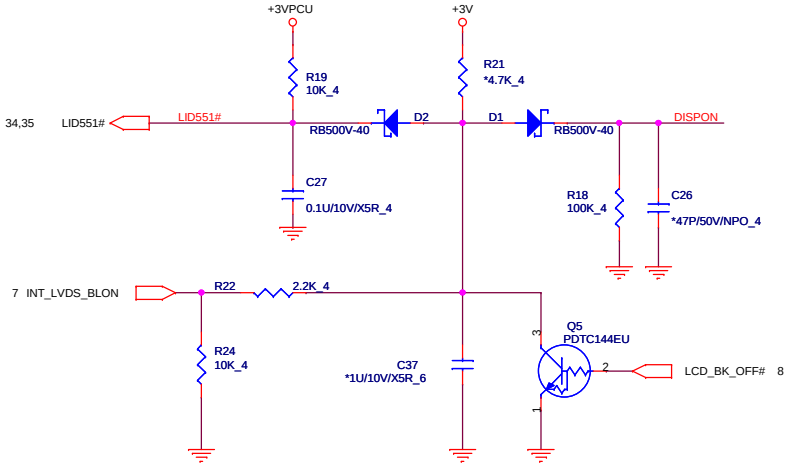
LCDVCC

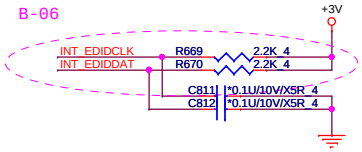


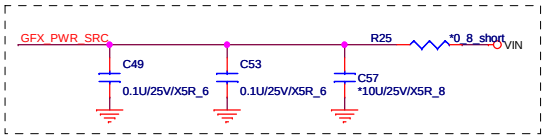




back light





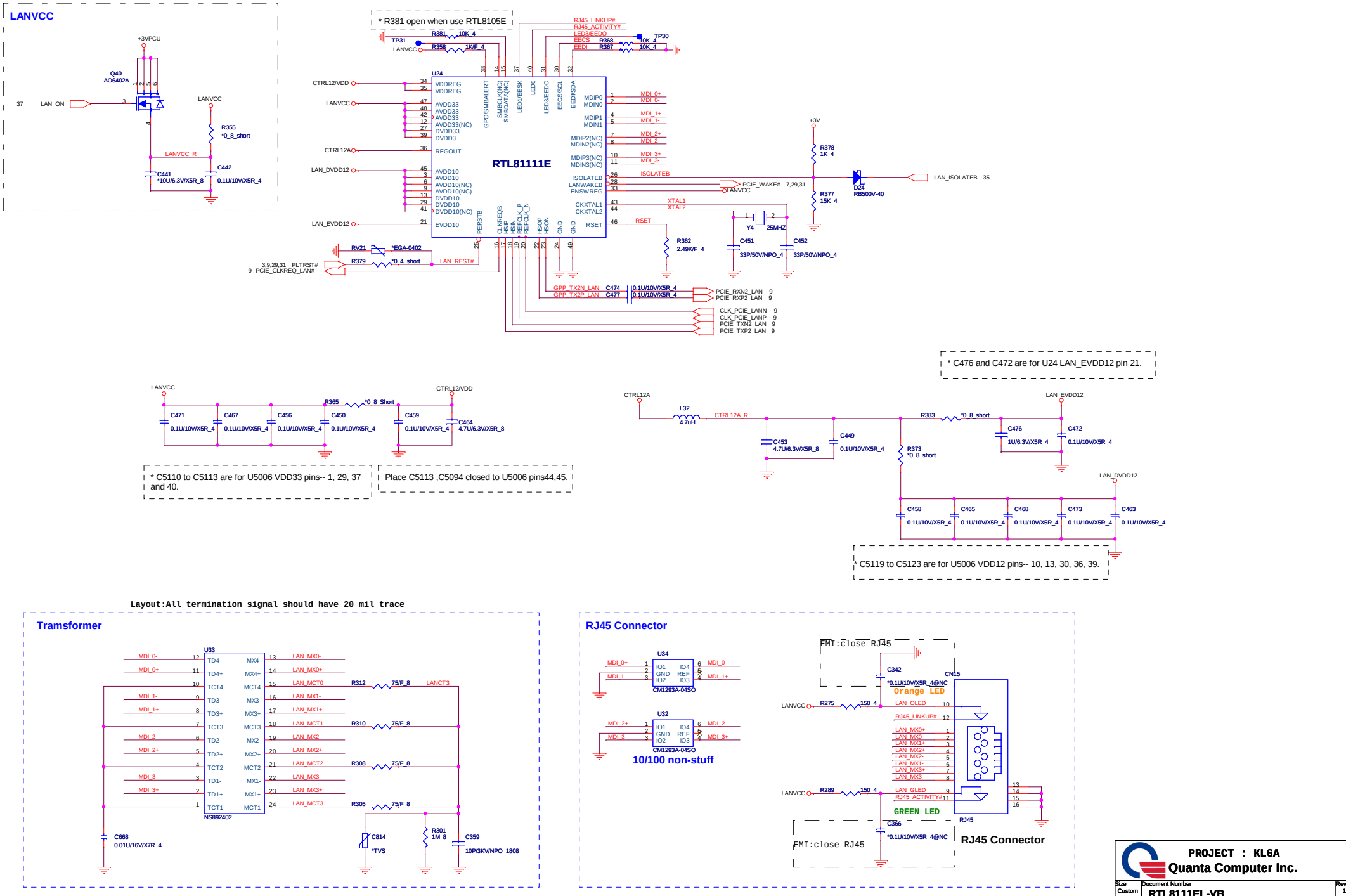


PROJECT : KL6A

Quanta Computer Inc.

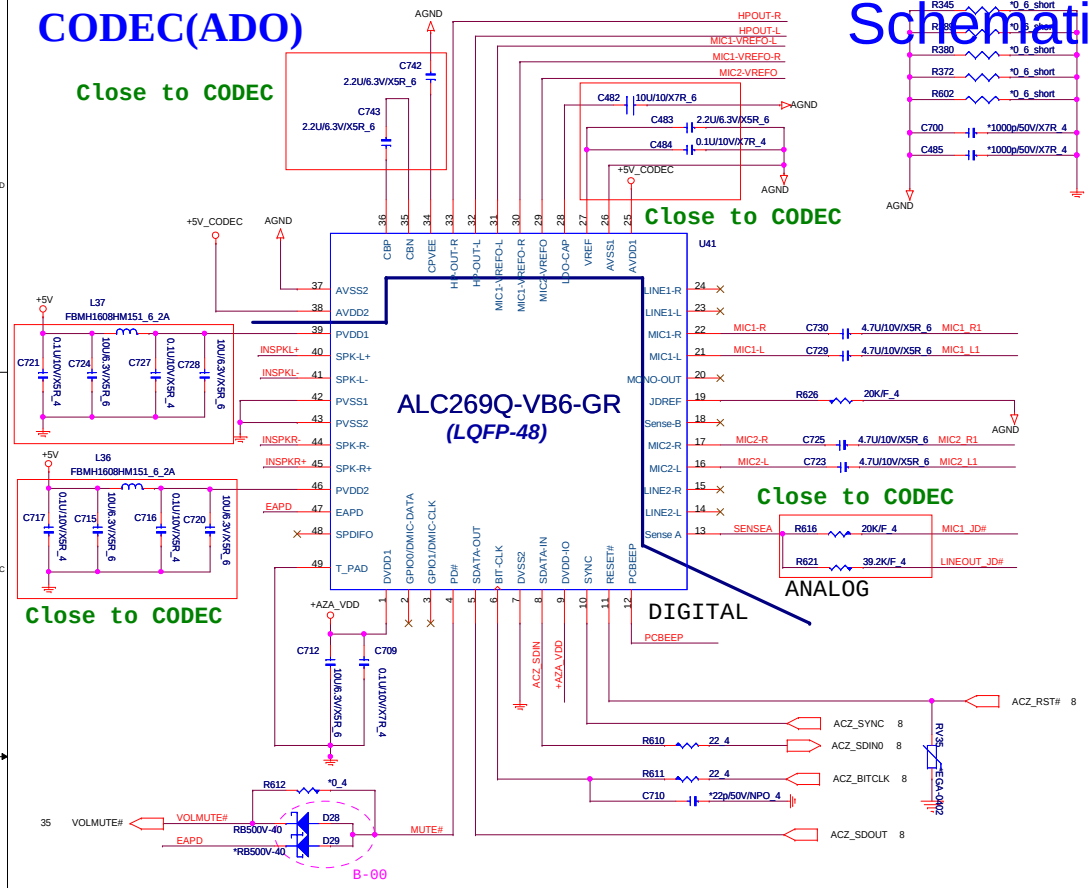
Size	Document Number	Rev
Custom	LCD CONN	1A

Date: Friday, October 29, 2010 Sheet 24 of 47

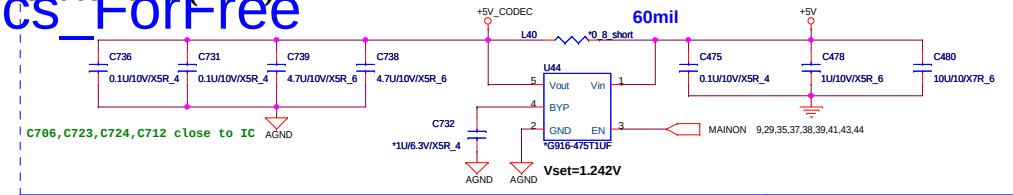

LANVCC
+3VPCU
Q40
AO6402A
LAN_ON
LANVCC
R355
*0_8_short
LANVCC_R
C441
*10U/6.3V/X5R_8
C442
0.1U/10V/X5R_4
* R381 open when use RTL8105E
R381 10K_4
TP31
LANVCC
R358 1K/F_4
RJ45_LINKUP#
RJ45_ACTIVITY#
LED3/EEDO
EECS
EEDI
R368 10K_4
R367 10K_4
TP30
U24
RTL81111E
CTRL12/VDD
LANVCC
CTRL12A
LAN_DVDD12
LAN_EVDD12
RV21 *EGA-0402
R379 *0_4_short
LAN_REST#
3,9,29,31 PLTRST#
9 PCIE_CLKREQ_LAN#
MDI_0+
MDI_0-
MDI_1+
MDI_1-
MDI_2+
MDI_2-
MDI_3+
MDI_3-
ISOLATEB
PCIE_WAKE# 7,29,31
LANVCC
+3V
R378 1K_4
R377 15K_4
D24 RB500V-40
LAN_ISOLATEB 35
XTAL1
XTAL2
Y4 25MHZ
C451 33P/50V/NPO_4
C452 33P/50V/NPO_4
R362 2.49K/F_4
RSET
GPP_TX2N_LAN C474 0.1U/10V/X5R_4
GPP_TX2P_LAN C477 0.1U/10V/X5R_4
PCIE_RXN2_LAN 9
PCIE_RXP2_LAN 9
CLK_PCIE_LANN 9
CLK_PCIE_LANP 9
PCIE_TXN2_LAN 9
PCIE_TXP2_LAN 9
* C476 and C472 are for U24 LAN_EVDD12 pin 21.
LANVCC
CTRL12/VDD
R365 *0_8_Short
C471 0.1U/10V/X5R_4
C467 0.1U/10V/X5R_4
C456 0.1U/10V/X5R_4
C450 0.1U/10V/X5R_4
C459 0.1U/10V/X5R_4
C464 4.7U/6.3V/X5R_8
* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.
Place C5113 ,C5094 closed to U5006 pins44,45.
CTRL12A
L32 4.7uH
CTRL12A_R
C453 4.7U/6.3V/X5R_8
C449 0.1U/10V/X5R_4
R383 *0_8_short
R373 *0_8_short
LAN_EVDD12
C476 1U/6.3V/X5R_4
C472 0.1U/10V/X5R_4
LAN_DVDD12
C458 0.1U/10V/X5R_4
C465 0.1U/10V/X5R_4
C468 0.1U/10V/X5R_4
C473 0.1U/10V/X5R_4
C463 0.1U/10V/X5R_4
* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.
Layout:All termination signal should have 20 mil trace
Tramsformer
U33
NS892402
MDI_0-
MDI_0+
MDI_1-
MDI_1+
MDI_2-
MDI_2+
MDI_3-
MDI_3+
LAN_MX0-
LAN_MX0+
LAN_MCT0
LAN_MX1-
LAN_MX1+
LAN_MCT1
LAN_MX2-
LAN_MX2+
LAN_MCT2
LAN_MX3-
LAN_MX3+
LAN_MCT3
R312 75/F_8
R310 75/F_8
R308 75/F_8
R305 75/F_8
LANCT3
C668 0.01U/16V/X7R_4
C814 *TVS
R301 1M_8
C359 10P/3KV/NPO_1808
RJ45 Connector
U34
U32
CM1293A-04SO
10/100 non-stuff
EMI:Close RJ45
C342 *0.1U/10V/X5R_4@NC
CN15
Orange LED
LANVCC
R275 150_4
LAN_OLED
RJ45_LINKUP#
LAN_MX0+
LAN_MX0-
LAN_MX1+
LAN_MX2+
LAN_MX2-
LAN_MX1-
LAN_MX3+
LAN_MX3-
R289 150_4
LAN_GLED
RJ45_ACTIVITY#
GREEN LED
C366 *0.1U/10V/X5R_4@NC
RJ45
EMI:close RJ45
RJ45 Connector
PROJECT : KL6A
Quanta Computer Inc.
Size Custom
Document Number RTL8111EL-VB
Rev 1A
Date: Friday, October 29, 2010
Sheet 25 of 47

Schematics_ForFree

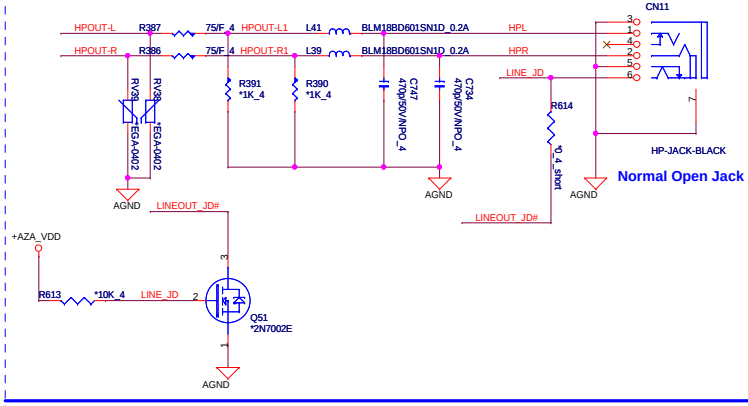
CODEC(ADO)



Codec Power(ADO)



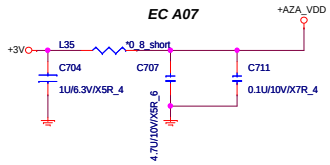
Earphone(AMP)



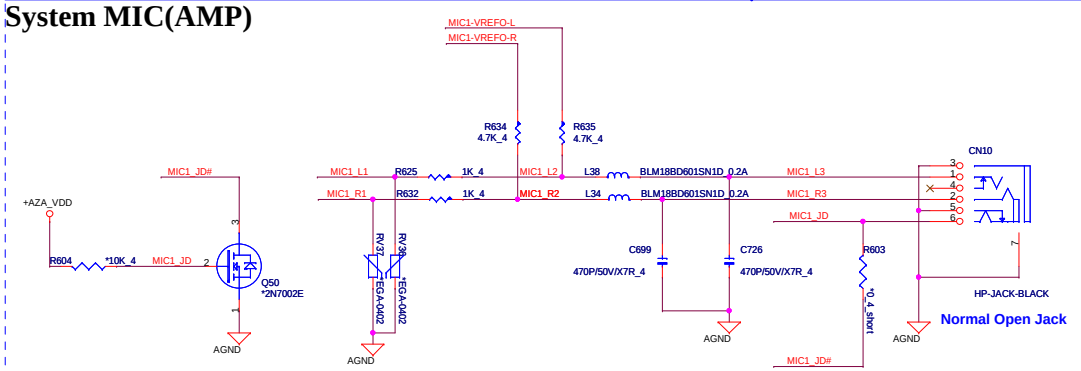
HDA Power(ADO)

*Intel HDA Either +1.5V_S5 or +3V_S5

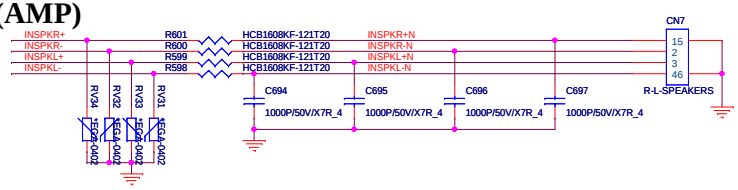
EC A07



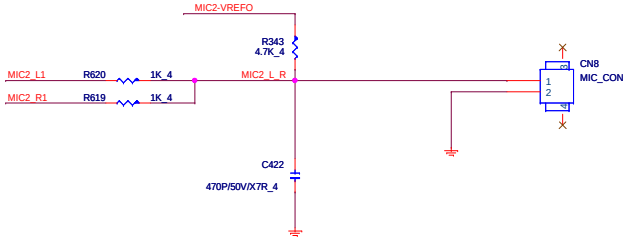
System MIC(AMP)



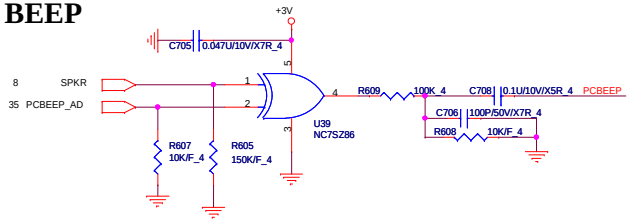
Speaker(AMP)



INTERNAL MIC



PC BEEP



PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALC269/MIC/Line out	1A

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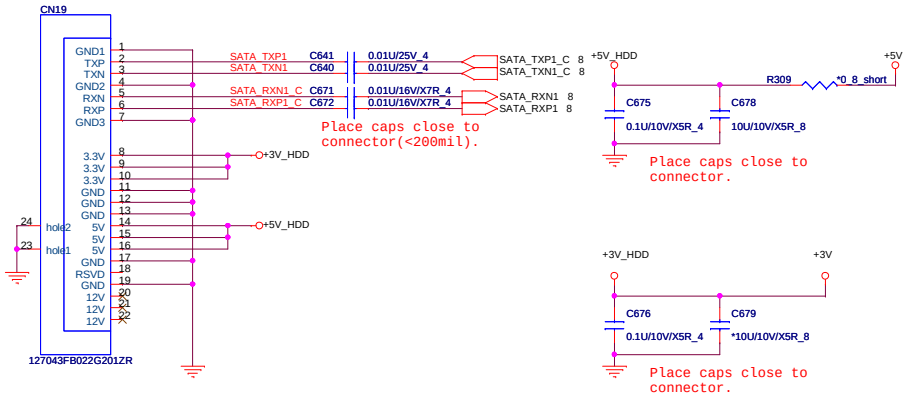
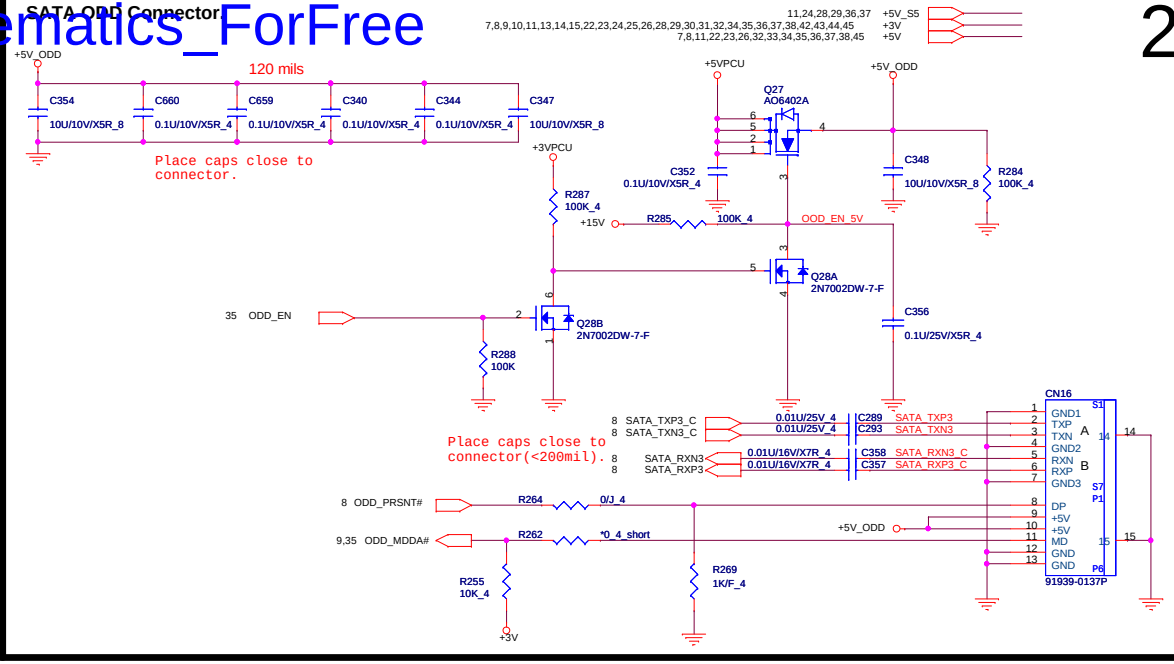
Schematics_ForFree

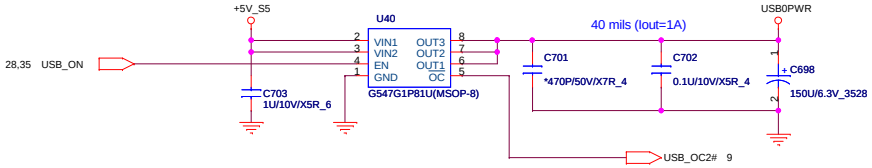
SATA HDD Connector.

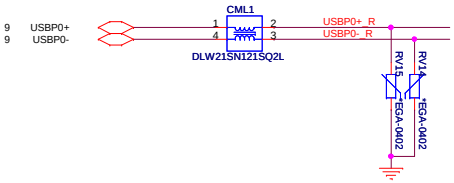


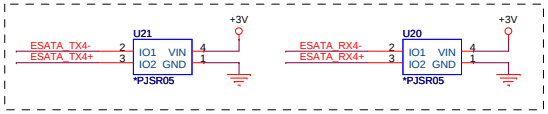
SATA ODD Connector



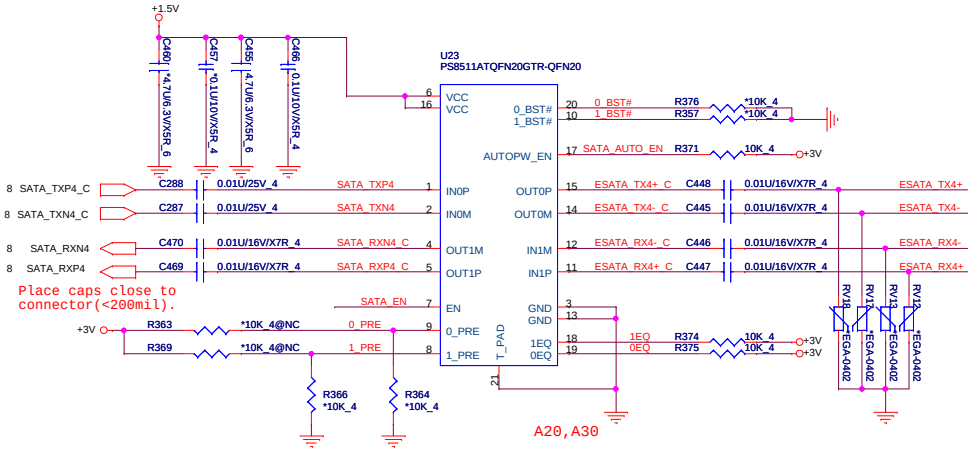
USB + E-SATA







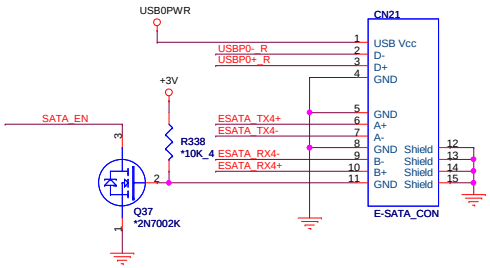
E-SATA RE-DRIVER



All straps of PS8511A have int. PL 150Kohm.

EN	AUTO_EN	0/1EQ	0/1EQ	0/1_BST#	0/1_BST#	0/1_PRE	0/1_PRE	Function
0	X	X	X	X	X	X	X	Standby
1	0	X	X	X	X	X	X	disable auto power saving
1	1	X	X	X	X	X	X	enable auto power saving
1	X	0	X	X	X	X	X	Short and medium length
1	X	X	1	X	X	X	X	Long length
1	X	X	X	0	X	X	X	Output :800~1200 mVpp
1	X	X	X	X	1	X	X	Output :400~700 mVpp
1	X	X	X	X	X	0	X	Pre-emphasis disabled
1	X	X	X	X	X	X	1	Pre-emphasis enabled

USB 0



PROJECT : KL6A

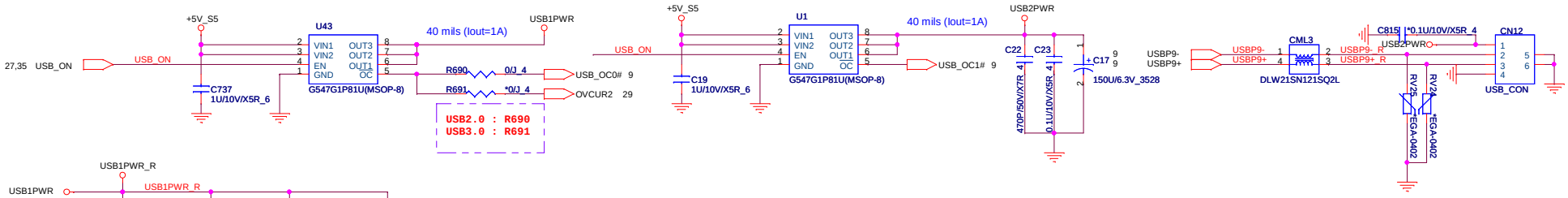
Quanta Computer Inc.

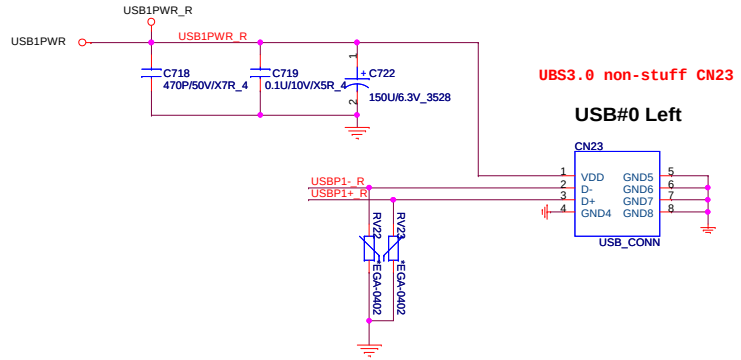
Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A

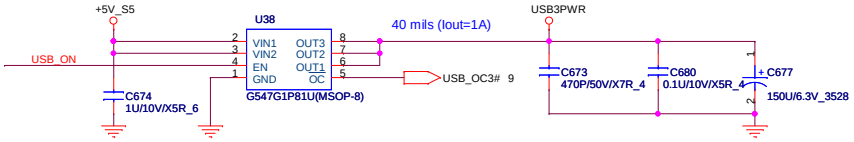
Date: Friday, October 29, 2010 Sheet 27 of 47

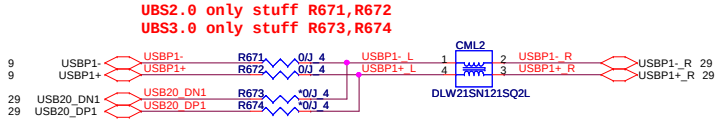
USB2.0*3

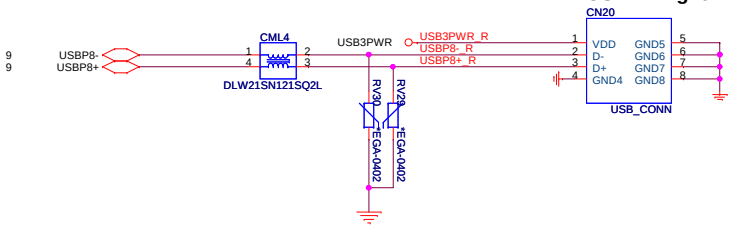
USB#1 Daughter board



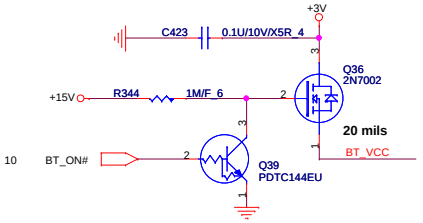


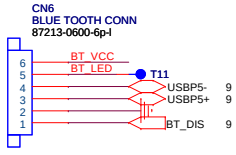






BLUETOOTH





PROJECT : KL6A			
Quanta Computer Inc.			
Size	Document Number BT/USBX3		Rev 1A
Date: Friday, October 29, 2010		Sheet 28 of 47	

Schematics_ForFree

REAR USB PORT X1

USB3.0 PORT1

SUY USB3.0: DFHS09FR063

C754, C752 close to CN24

U47

VL800 / VL801 QFN88
VL800 4PORT
VL801 2PORT

Near PCIEx Slot

For debug only.
Don't connect to system SMBus

Remove power for VL801

SPI Flash ROM

MX25L512MC-12G

Copy From ZN7

ESD

U46

*RClamp0544.TBT
msop10-4_9-5

X'tal 25MHz

25MHz/20pF/30ppm

BG625000486

XTL-5_3X3_2-3_8-1_2H

Crystal foot print must be reserved in case 25MHz clock from clock generator is not stable enough.

For USB3.0

Remove SUSD turn on switch (From PCU to SUS)
(Used +3V_S5 power plane)

Power circuit (+1.05_SUS)

For USB3.0

U48
G9661-25ADJF11U

0.6A

0.8V

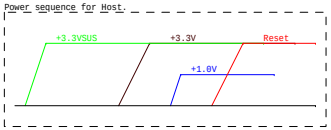
Vout =0.8(1+R1/R2)

For +3V_SUS (Power for wake up)

For +3V_RUN

For +1.05_SUS (Power for wake up)

Power sequence for Host.



PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
C	USB3.0 *1	1A

Date: Friday, October 29, 2010 Sheet 29 of 47

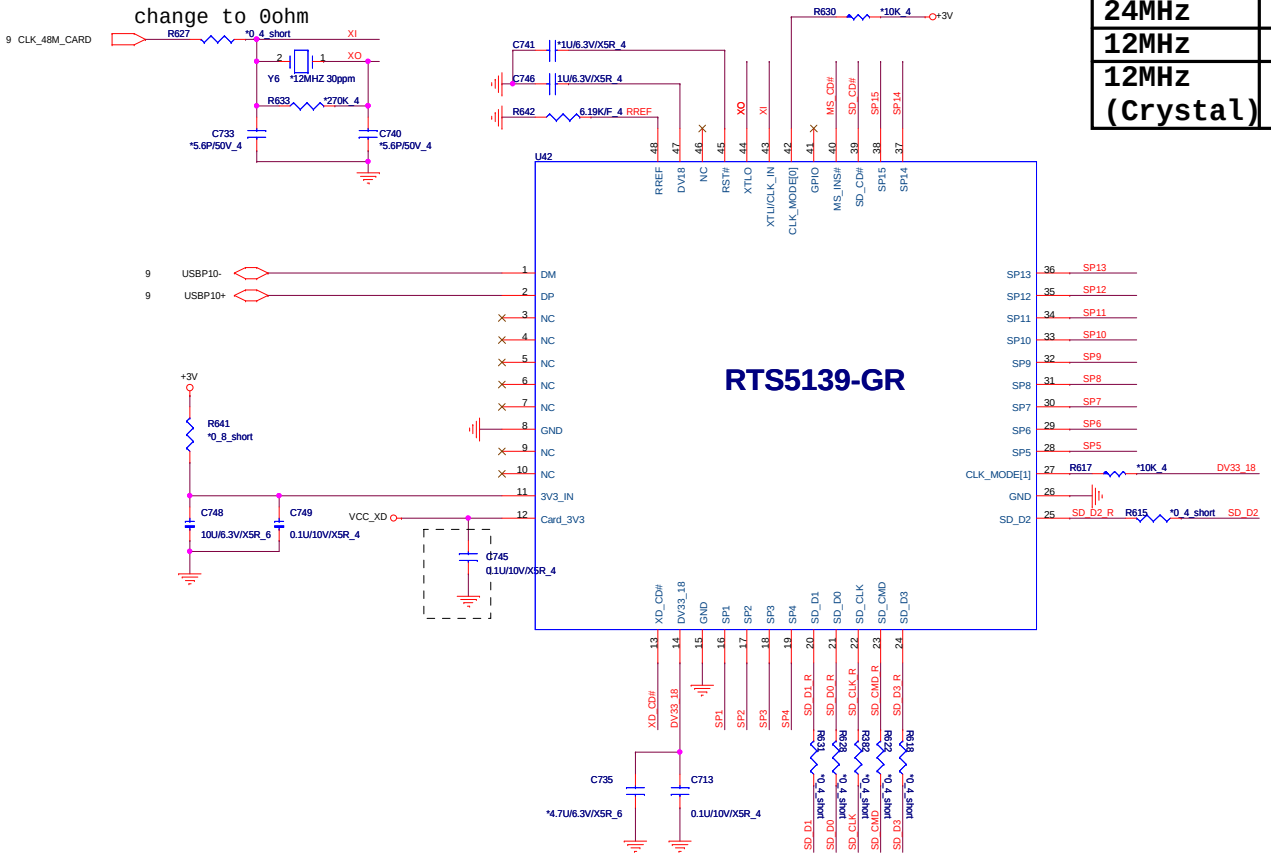
Clock Mode strap	R9287	R9307
48MHz	X	X
24MHz	X	O
12MHz	O	X
12MHz (Crystal)	O	O

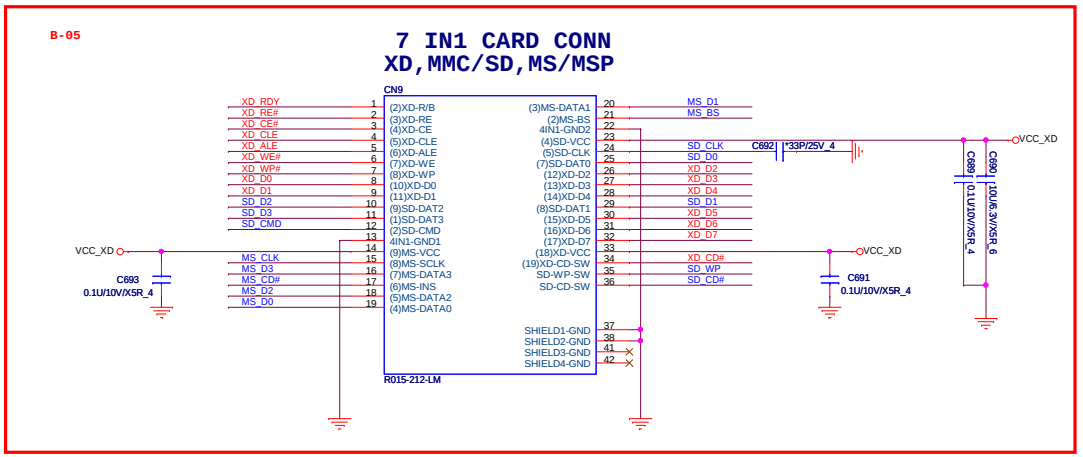
Note:

SD/MMC	MS	XD
SP1 SD_D7		XD_RDY
SP2 SD_D6		XD_RE#
SP3 SD_D5		XD_CE#
SP4 SD_D4		XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15 SD_WP		XD_D7

For RTS5139

SD,MS 4bit only





PROJECT : KL6A

Quanta Computer Inc.

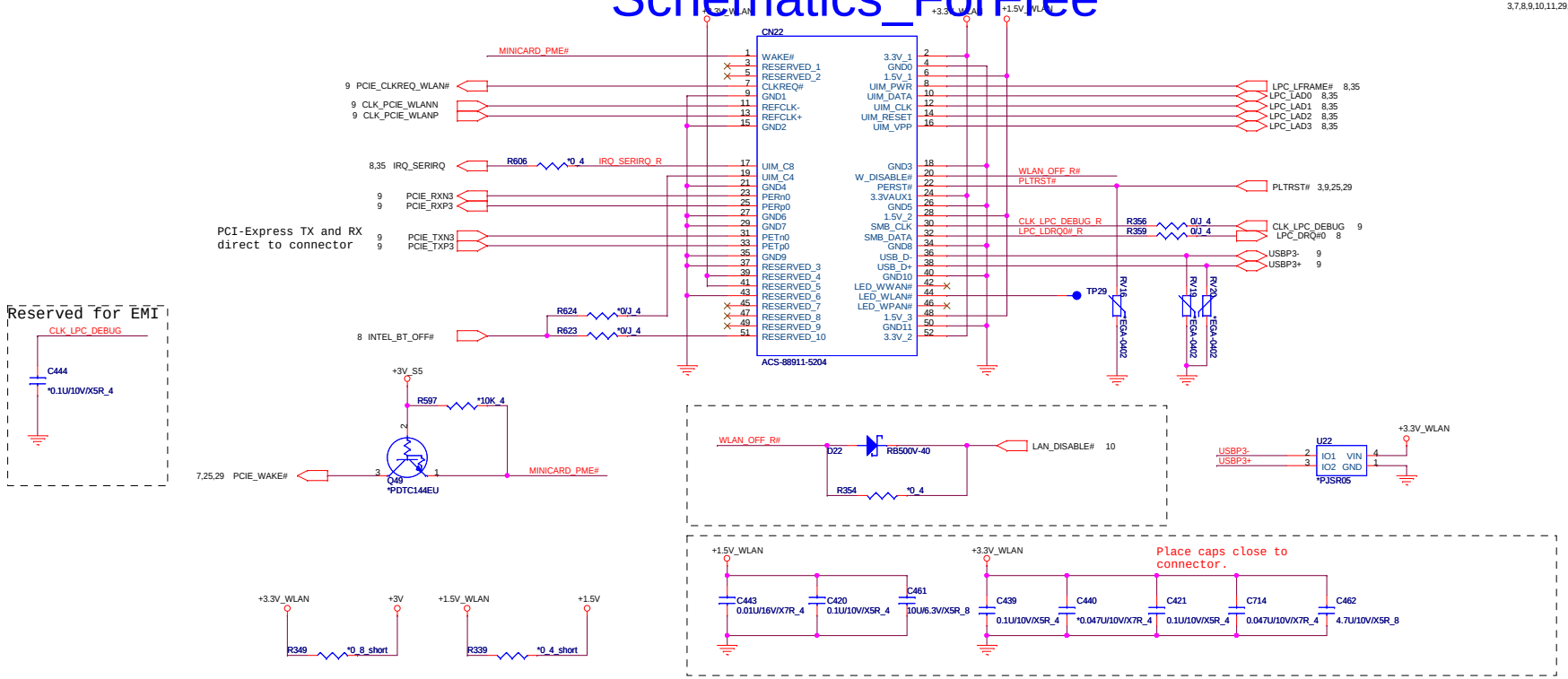
Size	Document Number	Rev
Custom	Card Reader (RTS5159)	1A

Date: Friday, October 29, 2010 Sheet 30 of 47

MiniCard WLAN connector

Schematics_ForFree

7,8,9,10,11,13,14,15,22,23,24,25,26,27,28,29,30,32,34,35,36,37,38,42,43,44,45 +3V
11,27,37 +1.5V
3,7,8,9,10,11,29,34,37 +3V_S5



PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-Card WLAN	1A
Date: Friday, October 29, 2010	Sheet 31 of 47	

FAN CONTROL

Schematics_ForFree

NOTE: Place C670 near Q47

NOTE: Place C744 near Q52

NOTE: Place C77 near U5

NOTE: Place C648 near Q45

NOTE: Place C62 near U5

Q47 SST3904

C670 *100P/50V/X7R_4

DDR3

Q52 SST3904

C744 *100P/50V/X7R_4

C77 2200P/50V/X7R_4

WLAN-ONFI

Q45 SST3904

C648 *100P/50V/X7R_4

CPU

C63 2200P/50V/X7R_4

R35 22_4 +3V_FAN

C62 0.1U/10V/X5R_4

U5 EMC2103-2

T_PAD DP2/DN3 DN2/DP3 TRIP_SET SHDN_SEL

DN DP VDD GPIO1 GPIO2 ALERT# SYS_SHDN# SMDATA

GND PWM TACH SMCLK

R51 2.05K_4

R53 6.8K/F_4

R42 10K_4 R47 10K_4 R55 10K_4 R63 10K_4 R65 10K_4 R64 10K_4

R66 10K_4

+5V R586 *0_8_short +5V_FAN

C667 1U/10V/X5R_6

C663 0.1U/10V/X5R_4

D4 RB500V-40

C816 *100P/50V/X7R_4

C817 *100P/50V/X7R_4

CN17 FAN_CON

+5V_FAN FAN_PWM FANSIG

Q11 2N7002 MB_CLK1 9,18,34,35

Q10 2N7002 MB_DATA1 9,18,34,35

Q6 2N7002 SYS_SHDN# 40,45

RV1 *EGA-0402

D3 *DIS@RB500V-40 VGA_OVT# 18,35

MB_ALRET# R37 *0_4 TEMP_ALERT# 10,35

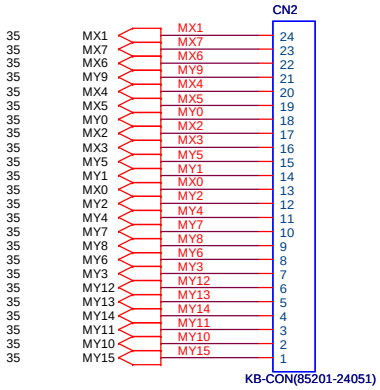
PROJECT : KL6A

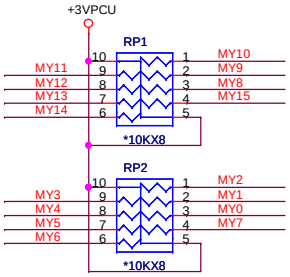
Quanta Computer Inc.

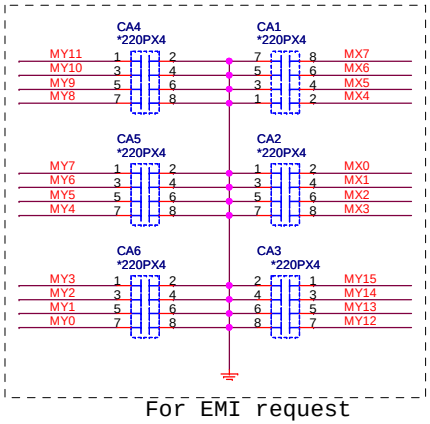
Size	Document Number	Rev
Custom	FAN /THERMAL	1A

Date: Friday, October 29, 2010 Sheet 32 of 47

KEYBOARD



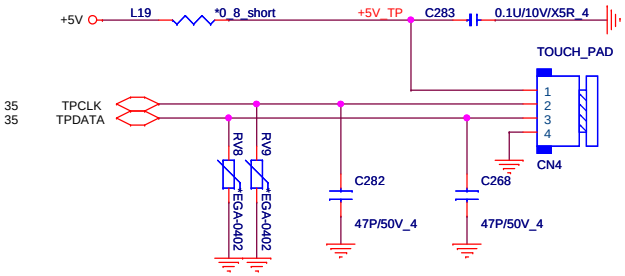




For EMI request

7,8,11,22,23,26,27,32,34,35,36,37,38,45 +5V
7,8,24,25,27,34,35,37,38,40,41 +3VPCU

Touch pad



PROJECT : KL6A		
Quanta Computer Inc.		
Size: Custom	Document Number: K/B, T/P	Rev: 1A
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Schematics_ForFree

3,7,8,9,10,11,29,31,37 +3V_S5
7,8,10,11,13,14,15,22,23,24,25,26,27,28,29,30,31,32,35,36,37,38,42,43,44,45 +3V

VGA UMA/DIS SWITCH

+3V_S5
R385 100K_4
35 VGA_SWITCH#
SW2
DIS@VGA_SWITCH
C481 DIS@0.1U/10V/X5R_4

RF ON/OFF SWITCH

+3V_S5
R384 100K_4
35 RF_SW#
SW1
RF_SLIDE_SWITCH
C479 0.1U/10V/X5R_4

VGA

9 DIS_BULE_LED
Q53 DIS@PDTC144EU
DIS_BULE_LED# R638 DIS@100_6 DIS_BULE_LED#_R
LED3 DIS@RIGHT-ANGLE-WHITE_LED
+3V

RF

9 RF_ON
Q54 PDTC144EU
RF_ON# R639 100_6 RF_ON#_R
LED4 RIGHT-ANGLE-WHITE_LED
+3V

TP LED

35 TP_LED#
R388 100_6 TP_LED#_R
LED1 RIGHT-ANGLE-WHITE_LED
+3V

Battery

35 BATLED_GREEN_LED#
35 BATLED_AMBER_LED#
R637 100_6 BATLED_GREEN_LED#_R
R636 100_6 BATLED_AMBER_LED#_R
LED2 WHITE AMBER RIGHT-ANGLE-LED
+3V_S5

Power/suspend LED

35 PWR_WHITE
Q15 PDTC144EU
PWR_WHITE# R640 100_6 PWR_WHITE#_R
LED5 RIGHT-ANGLE-WHITE_LED
+3VPCU

CAPACITANNCE BUTTON BOARD

9,18,32,35 MB_CLK1
9,18,32,35 MB_DATA1
35 MMB_SM_INT#
Q56 2N7002
Q57 2N7002
+3V
+5V
R286 *0_6_short
R283 *0_6_short
R281 *0_4
C819 C820 C351 C355 C353 RV10 RV11
Slide bar 2.0 CONN CN5

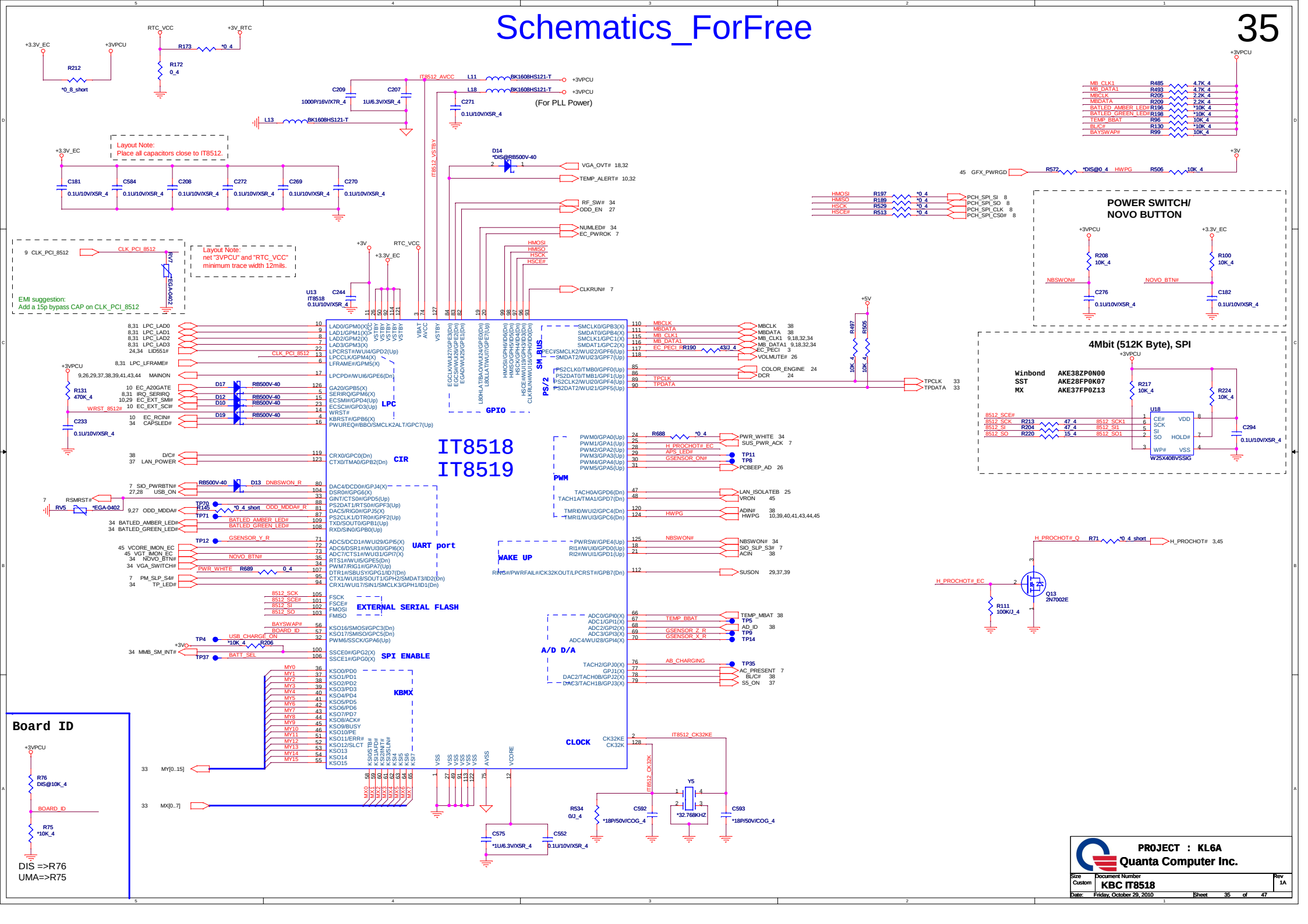
POWER BOARD

HDD
NUMLED#
CAPSLED#
35 NBSWON#
35 NOVO_BTN#
24,35 LID551#
8 SATA_ACT#
35 NUMLED#
35 CAPSLED#
+3V R105 *0_6_short
C193 0.1U/10V/X5R_4
+3VPCU
PWR_WHITE#
CN3 Connector-FPC/FFC
RV2 RV4 RV3 C202 C191 C205 C189 C204 C188 C192 C190

CCD BOARD

9 USBP2-
9 USBP2+
C821 *0.1U/10V/X5R_4
+3V R401 *0_6_short
L33 DLW21SN121SQ2L
USBP2- R
USBP2+ R
CN13 USB_CON
RV27 RV28 FOR ESD

PROJECT : KL6A		
Quanta Computer Inc.		
Size: Custom	Document Number: B TO B CON/LED	Rev: 1A
Date: Friday, October 29, 2010	Sheet 34 of 47	


IT8518
IT8519
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512
(For PLL Power)
POWER SWITCH/
NOVO BUTTON
4Mbit (512K Byte), SPI
Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13
Board ID
DIS =>R76
UMA=>R75
PROJECT : KL6A
Quanta Computer Inc.
KBC IT8518
Friday, October 29, 2010

Schematics_ForFree

CPU BKT

Screw for ME

36

WLAN

HOLE18 H-TC217BC142D102P2

HOLE19 H-TC217BC75I75D35P2

SMT NUT H=4/7mm

VGA

HOLE16 DIS@H-TC5_5BC4I3D3P2

HOLE17 DIS@H-TC5_5BC4I3D3P2

SMT NUT H=4/7mm

HOLE9 *C142D102N

HOLE15 AGND *HG-TC276BC315D106P2

HOLE13 *HG-TC276BC315D106P2

HOLE12 *HG-TC276BC315D106P2

HOLE11 *HG-TC276BC315D106P2

HOLE14 *HG-TC276BC315D106P2

HOLE8 *HG-TC276BC315D106P2

HOLE5 *HG-TC276BC315D106P2

HOLE6 *HG-TC276BC315D106P2

HOLE4 *H-TC276BC315D106P2

HOLE3 *H-TC276BC315D106P2

HOLE2 *H-TC276BC315D106P2

HOLE10 *H-BS236X150D59PB

HOLE7 *H-BC197D59PB

HOLE20 *Spad-re1010x45np

HOLE21 *Spad-re1010x45np

HOLE22 *spad-kl6-1np

HOLE23 *spad-kl6-2np

HOLE24 *spad-re160x774np

HOLE25 *spad-re225x460np

EMI suggestion

VIN	VIN	VIN	VIN	VIN	VIN	VIN	VIN	VIN	+5V	+VCC_GFX	+VCC_GFX
C367	C54	C31	C415	C296	C20	C406	C405	C50	C807	C808	C809
*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	0.1U/25V/X5R_4	0.1U/25V/X5R_4	2200P/50V/X7R_4

B-08

+5V_S5	+3V	+3V	+1.05V_PCH	+1.05V_PCH	+1.5V_SUS	GFX_CORE	VIN	VIN	+3V	+VCC_CORE	VIN
SC822	*0.1U/25V/X5R_4	SC823	*0.1U/25V/X5R_4	SC824	*0.1U/25V/X5R_4	SC825	*0.1U/25V/X5R_4	SC834	*0.1U/25V/X5R_4	SC835	*0.1U/25V/X5R_4
SC826	*0.1U/25V/X5R_4	SC827	*0.1U/25V/X5R_4	SC828	*0.1U/25V/X5R_4	SC829	*0.1U/25V/X5R_4	SC838	*0.1U/25V/X5R_4	SC837	*0.1U/25V/X5R_4
SC830	*0.1U/25V/X5R_4	SC831	*0.1U/25V/X5R_4					SC841	*0.1U/25V/X5R_4		
SC832	*0.1U/25V/X5R_4	SC833	*0.1U/25V/X5R_4					SC844	*0.1U/25V/X5R_4		
SC869	*0.1U/25V/X5R_4	SC870	*0.1U/25V/X5R_4					SC847	*0.1U/25V/X5R_4		
								SC850	*0.1U/25V/X5R_4		
VIN		+1.5V_SUS	+3V	+5V	+5V_S5	+5V_S5	+1.5V_SUS	VIN	+5V		
SC839	0.1U/25V/X5R_4	SC840	*0.1U/25V/X5R_4	SC865	*0.1U/25V/X5R_4	SC854	*0.1U/25V/X5R_4	SC866	*0.1U/25V/X5R_4		
SC842	0.1U/25V/X5R_4	SC843	*0.1U/25V/X5R_4	SC868	*0.1U/25V/X5R_4						
SC845	0.1U/25V/X5R_4	SC846	*0.1U/25V/X5R_4								
SC848	0.1U/25V/X5R_4	SC849	*0.1U/25V/X5R_4								
SC851	0.1U/25V/X5R_4	SC852	*0.1U/25V/X5R_4								
SC855	*0.1U/25V/X5R_4	SC856	*0.1U/25V/X5R_4								
SC857	0.1U/25V/X5R_4	SC858	*0.1U/25V/X5R_4								
SC859	*0.1U/25V/X5R_4	SC860	*0.1U/25V/X5R_4								
SC861	0.1U/25V/X5R_4	SC862	*0.1U/25V/X5R_4								
SC863	0.1U/25V/X5R_4	SC864	*0.1U/25V/X5R_4								
		SC867	*0.1U/25V/X5R_4								
HDMIC_5V											
SC876	*0.1U/25V/X5R_4										
SC872	*0.1U/25V/X5R_4										
SC873	*0.1U/25V/X5R_4										
SC874	*0.1U/25V/X5R_4										
SC875	*0.1U/25V/X5R_4										

ESD suggestion

PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	HOLD & SKEW	1A
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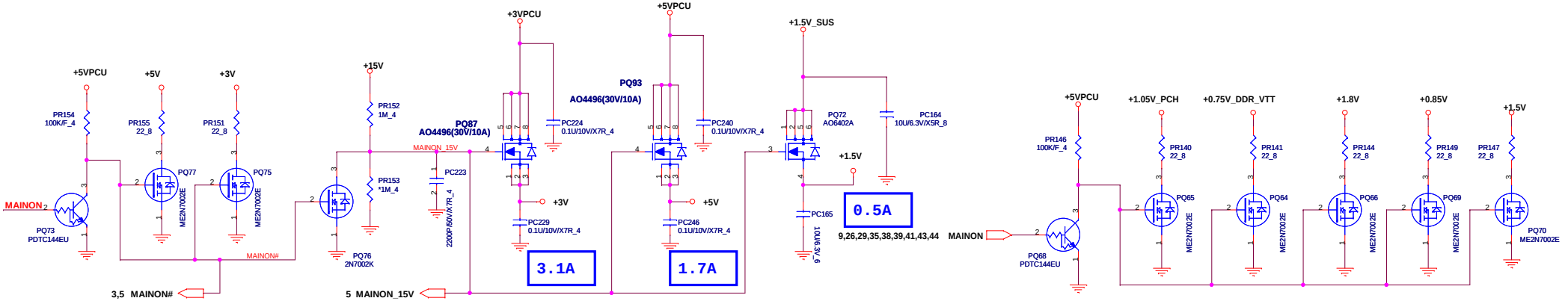
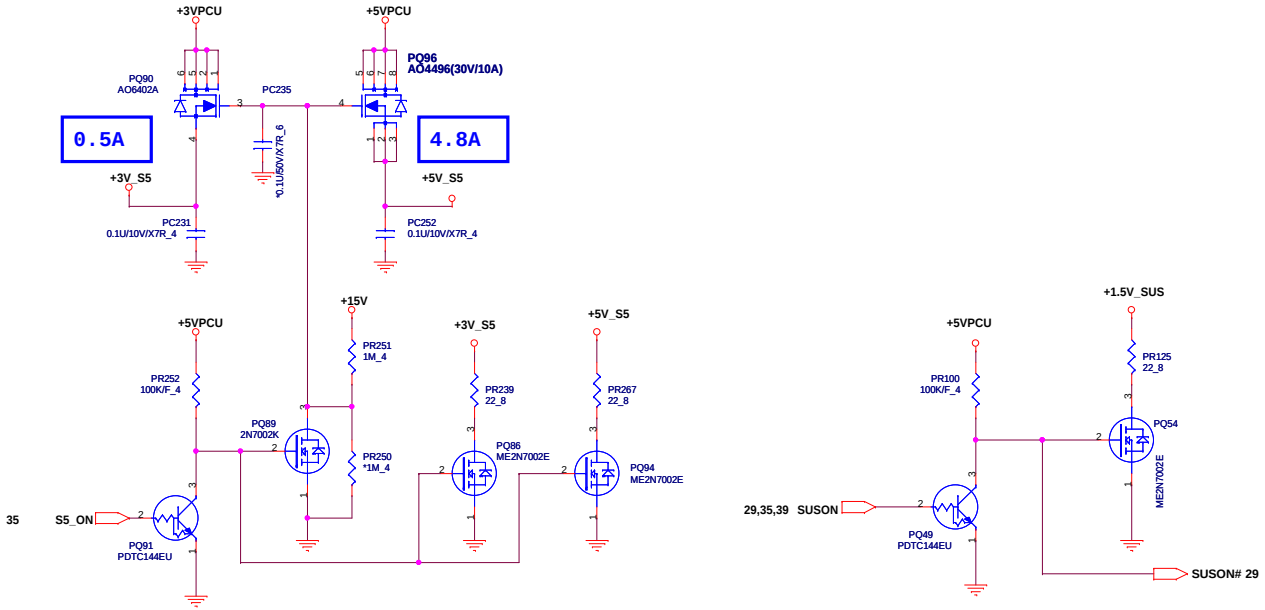
Schematics_ForFree

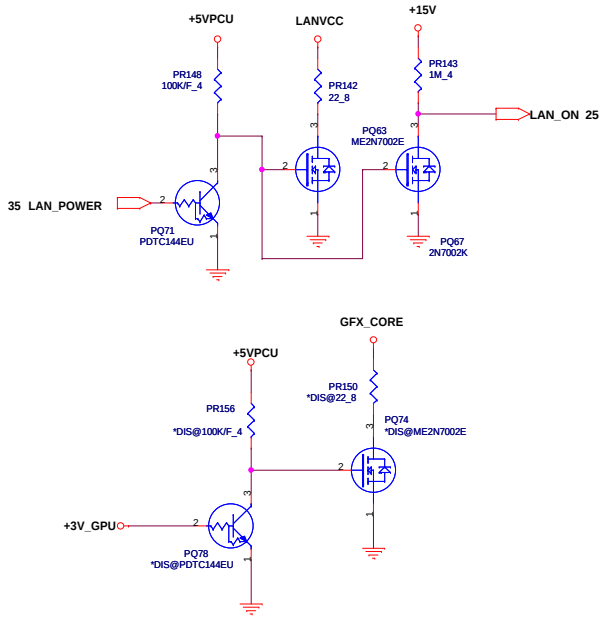
+3V, +5V,+1.5V



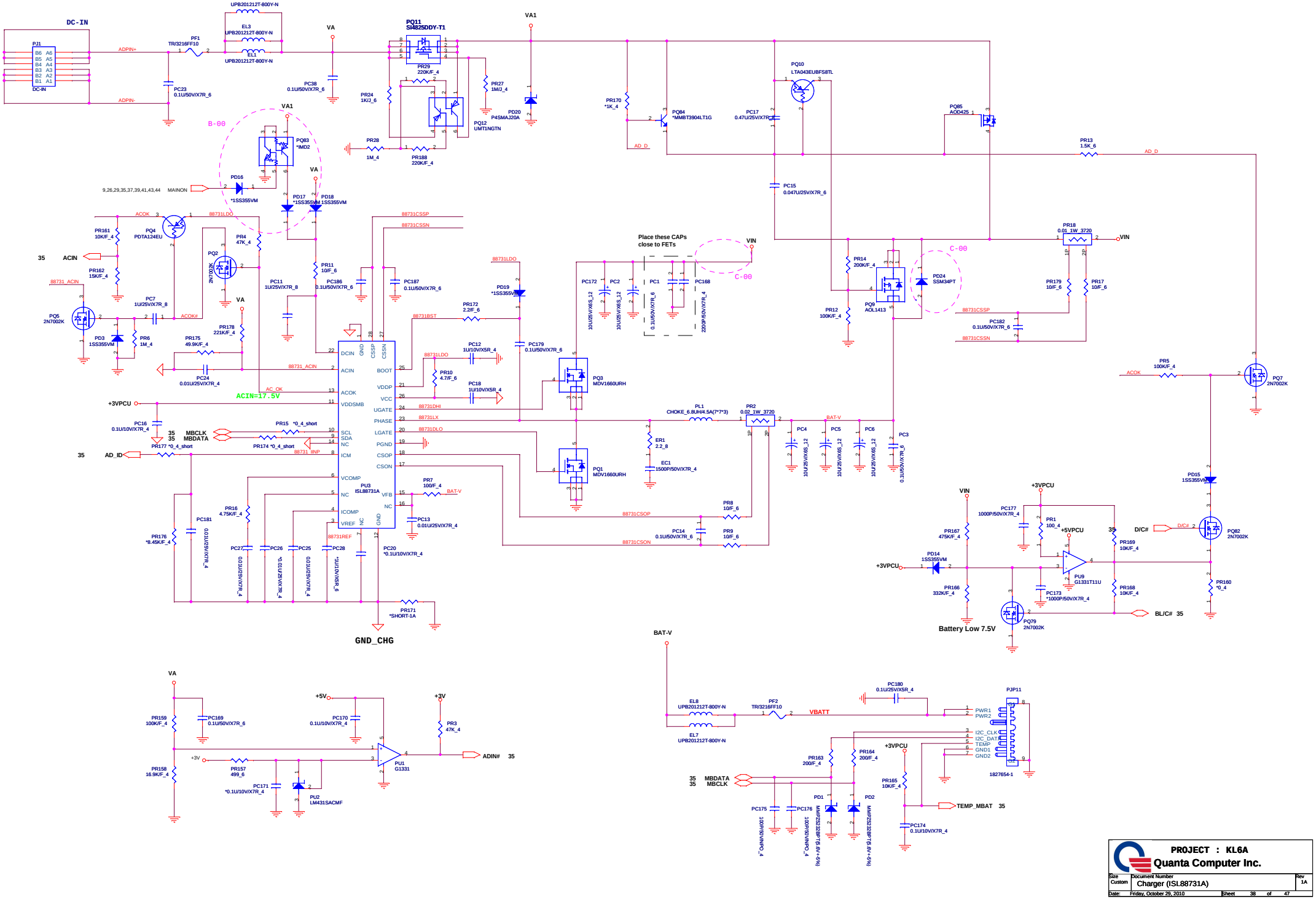
3V_S5, 5V_S5



LANVCC



PROJECT : KL6A		
Quanta Computer Inc.		
Size: Custom	Document Number: Discharge	Rev: 1A
Date: Friday, October 29, 2010	Sheet 37 of 47	


DC-IN
PJ1
DC-IN
ADPIN+
ADPIN-
PF1
TR/3216FF10
EL2
UPB201212T-800Y-N
EL3
UPB201212T-800Y-N
EL1
UPB201212T-800Y-N
PC23
0.1U/50V/X7R_6
VA
PC38
0.1U/50V/X7R_6
PQ11
SI4825DDY-T1
PR29
220K/F_4
PR24
1K/J_6
PR28
1M_4
PR188
220K/F_4
PQ12
UMT1NGTN
PR27
1M/J_4
PD20
P4SMAJ20A
VA1
PQ83
*IMD2
B-00
PD16
*1SS355VM
PD17
*1SS355VM
PD18
1SS355VM
9,26,29,35,37,39,41,43,44
MAINON
ACOK
88731LDO
PQ4
PDTA124EU
PR161
10K/F_4
PR162
15K/F_4
35
ACIN
88731_ACIN
PQ5
2N7002K
PD3
1SS355VM
PR6
1M_4
PC7
1U/25V/X7R_8
ACOK#
PR178
221K/F_4
PR175
49.9K/F_4
PC24
0.01U/25V/X7R_4
PQ2
2N7002K
PR4
47K_4
PR11
10F_6
PC186
0.1U/50V/X7R_6
PC11
1U/25V/X7R_8
88731CSSP
88731CSSN
PC187
0.1U/50V/X7R_6
88731BST
PR172
2.2/F_6
PC12
1U/10V/X5R_4
PC18
1U/10V/X5R_4
PR10
4.7/F_6
88731DHI
88731LX
88731DLO
PC179
0.1U/50V/X7R_6
PD19
*1SS355VM
+3VPCU
PC16
0.1U/10V/X7R_4
35
MBCLK
35
MBDATA
PR15
*0_4_short
PR174
*0_4_short
PR177
*0_4_short
35
AD_ID
88731_IINP
AC_OK
ACIN=17.5V
PU3
ISL88731A
DCIN
ACIN
ACOK
VDDSMB
GND
CSSP
CSSN
BOOT
VDDP
VCC
UGATE
PHASE
LGATE
PGND
CSOP
CSON
SCL
SDA
NC
ICM
VCOMP
NC
ICOMP
VREF
NC
GND
VFB
NC
PR7
100/F_4
BAT-V
PC13
0.01U/25V/X7R_4
88731REF
PC20
*0.1U/10V/X7R_4
PR171
*SHORT-1A
GND_CHG
PR16
4.75K/F_4
PC181
0.01U/25V/X7R_4
PR176
*8.45K/F_4
PC27
0.01U/25V/X7R_4
PC26
*0.01U/25V/X7R_4
PC25
0.01U/25V/X7R_4
PC28
*1U/10V/X5R_6
Place these CAPs
close to FETs
VIN
C-00
PC172
10U/25V/X6S_12
PC2
10U/25V/X6S_12
PC1
0.1U/50V/X7R_6
PC168
220P/50V/X7R_4
PQ3
MDV1660URH
PQ1
MDV1660URH
PL1
CHOKE_6.8UH/4.5A(7*7*3)
ER1
2.2_8
EC1
1500P/50V/X7R_4
PR2
0.02_1W_3720
BAT-V
PC4
10U/25V/X6S_12
PC5
10U/25V/X6S_12
PC6
10U/25V/X6S_12
PC3
0.1U/50V/X7R_6
88731CSOP
88731CSON
PC14
0.1U/50V/X7R_6
PR8
10F_6
PR9
10F_6
PR170
*1K_4
PQ84
*MMBT3904LT1G
AD_D
PQ10
LTA043EUBFS8TL
PC17
0.47U/25V/X7R_6
PQ85
AOD425
PR13
1.5K_6
PC15
0.047U/25V/X7R_6
PR14
200K/F_4
PQ9
AOL1413
PD24
SSM34PT
PR12
100K/F_4
PR18
0.01_1W_3720
PR179
10F_6
PR17
10F_6
PC182
0.1U/50V/X7R_6
PR5
100K/F_4
PQ7
2N7002K
PD15
1SS355VM
PQ82
2N7002K
D/C#
PR169
10K/F_4
PR168
10K/F_4
PR160
*0_4
BL/C#
35
PC177
1000P/50V/X7R_4
PR1
100_4
+5VPCU
PU9
G1331T11U
PC173
*1000P/50V/X7R_4
PR167
475K/F_4
PD14
1SS355VM
PR166
332K/F_4
PQ79
2N7002K
Battery Low 7.5V
VA
PR159
100K/F_4
PC169
0.1U/50V/X7R_6
PR158
16.9K/F_4
+5V
PC170
0.1U/10V/X7R_4
+3V
PR157
499_6
PC171
*0.1U/10V/X7R_4
PU2
LM431SACMF
PR3
47K_4
PU1
G1331
ADIN#
35
BAT-V
EL8
UPB201212T-800Y-N
EL7
UPB201212T-800Y-N
PF2
TR/3216FF10
VBATT
PC180
0.1U/25V/X5R_4
PJP11
PWR1
PWR2
I2C_CLK
I2C_DAT
TEMP
GND1
GND2
1827654-1
PR163
200/F_4
PR164
200/F_4
+3VPCU
PR165
10K/F_4
35
MBDATA
35
MBCLK
PD1
PD2
MMBZ5232BPT(5.6V~+5%)
PC175
100P/50V/NPO_4
PC176
100P/50V/NPO_4
TEMP_MBAT
35
PC174
0.1U/10V/X7R_4
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Quanta Computer Inc.
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Custom
Document Number
Charger (ISL88731A)
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+0.75V_DDR_VTT
TDC : 0.6A

+1.5VSUS
Fs=400K
TDC :19A(Imax)
OCP : 23A

PU7
RT8207LGQW

PQ57
AON6428L

PQ60
AON6718L

PQ56
*AON6718L

PL9
1.0uH/PCMC104T-1R0MN

5.5A

PQ19
DIS@AON6428L

3.9A

DIS@AO4496(30V/10A)
PQ35

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Quanta Computer Inc.			
Size: Custom	Document Number: DDR3/0.75V(RT8207LGQW)		Rev: 1A
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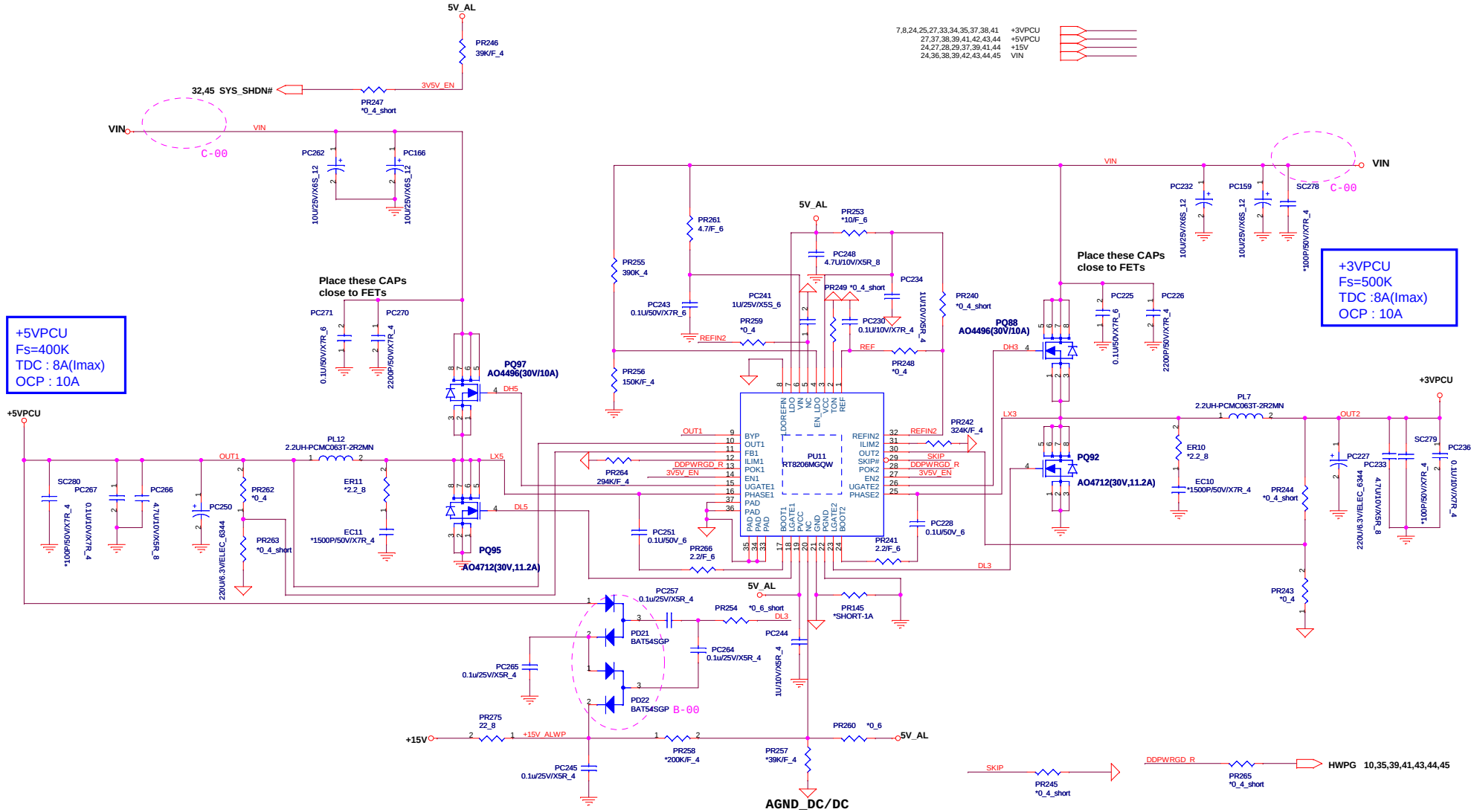
+5VPCU
Fs=400K
TDC : 8A(Imax)
OCP : 10A
+3VPCU
Fs=500K
TDC :8A(Imax)
OCP : 10A
Place these CAPs close to FETs
Place these CAPs close to FETs
PQ97 AO4496(30V/10A)
PQ95 AO4712(30V,11.2A)
PQ88 AO4496(30V/10A)
PQ92 AO4712(30V,11.2A)
PU11 RT8206MGQW
PL12 2.2UH-PCMC063T-2R2MN
PL7 2.2UH-PCMC063T-2R2MN
5V_AL
VIN
+15V
AGND_DC/DC
SYS_SHDN#
3V5V_EN
+15V_ALWP
DDPWRGD_R
SKIP
HWPG 10,35,39,41,43,44,45
7,8,24,25,27,33,34,35,37,38,41 +3VPCU
27,37,38,39,41,42,43,44 +5VPCU
24,27,28,29,37,39,41,44 +15V
24,36,38,39,42,43,44,45 VIN
PROJECT : KL6A
Quanta Computer Inc.
3V/5V (RT8206MGQW)
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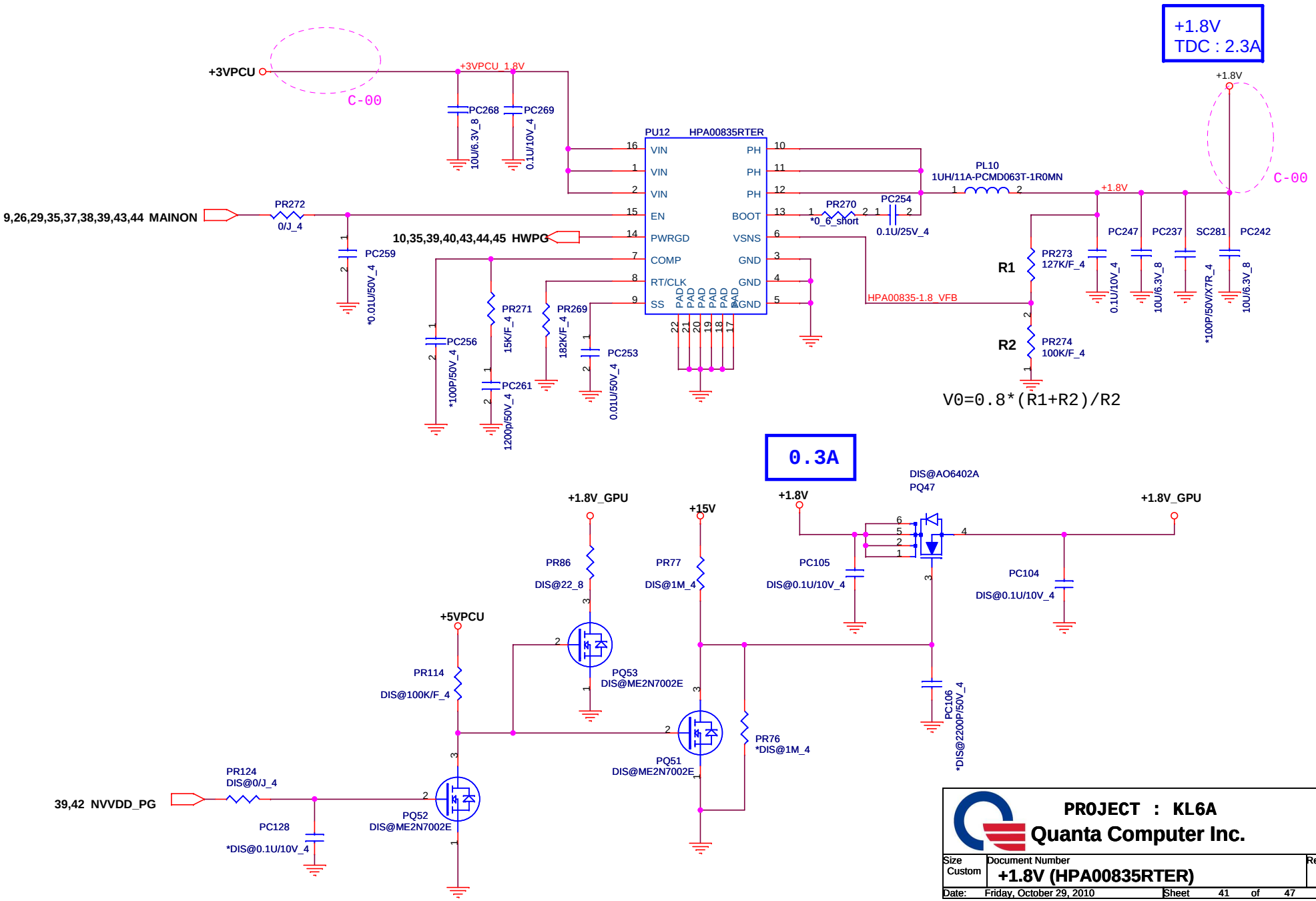
+1.8V
TDC : 2.3A
+3VPCU
C-00
+3VPCU_1.8V
PC268
10U/6.3V_8
PC269
0.1U/10V_4
PU12
HPA00835RTER
VIN
VIN
VIN
EN
PWRGD
COMP
RT/CLK
SS
PH
PH
PH
BOOT
VSNS
GND
GND
AGND
PAD
9,26,29,35,37,38,39,43,44 MAINON
PR272
0/J_4
10,35,39,40,43,44,45 HWPG
PC259
*0.01U/50V_4
PR271
15K/F_4
PR269
182K/F_4
PC256
*100P/50V_4
PC261
1200p/50V_4
PC253
0.01U/50V_4
PL10
1UH/11A-PCMD063T-1R0MN
PR270
*0_6_short
PC254
0.1U/25V_4
HPA00835-1.8_VFB
R1
PR273
127K/F_4
R2
PR274
100K/F_4
PC247
PC237
SC281
PC242
0.1U/10V_4
10U/6.3V_8
*100P/50V/X7R_4
10U/6.3V_8
V0=0.8*(R1+R2)/R2
0.3A
DIS@AO6402A
PQ47
+1.8V_GPU
+15V
+1.8V
+1.8V_GPU
PR86
DIS@22_8
PR77
DIS@1M_4
PC105
DIS@0.1U/10V_4
PC104
DIS@0.1U/10V_4
+5VPCU
PR114
DIS@100K/F_4
PQ53
DIS@ME2N7002E
PQ51
DIS@ME2N7002E
PR76
*DIS@1M_4
PC106
*DIS@2200P/50V_4
39,42 NVVDD_PG
PR124
DIS@0/J_4
PC128
*DIS@0.1U/10V_4
PQ52
DIS@ME2N7002E
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Quanta Computer Inc.
Size
Custom
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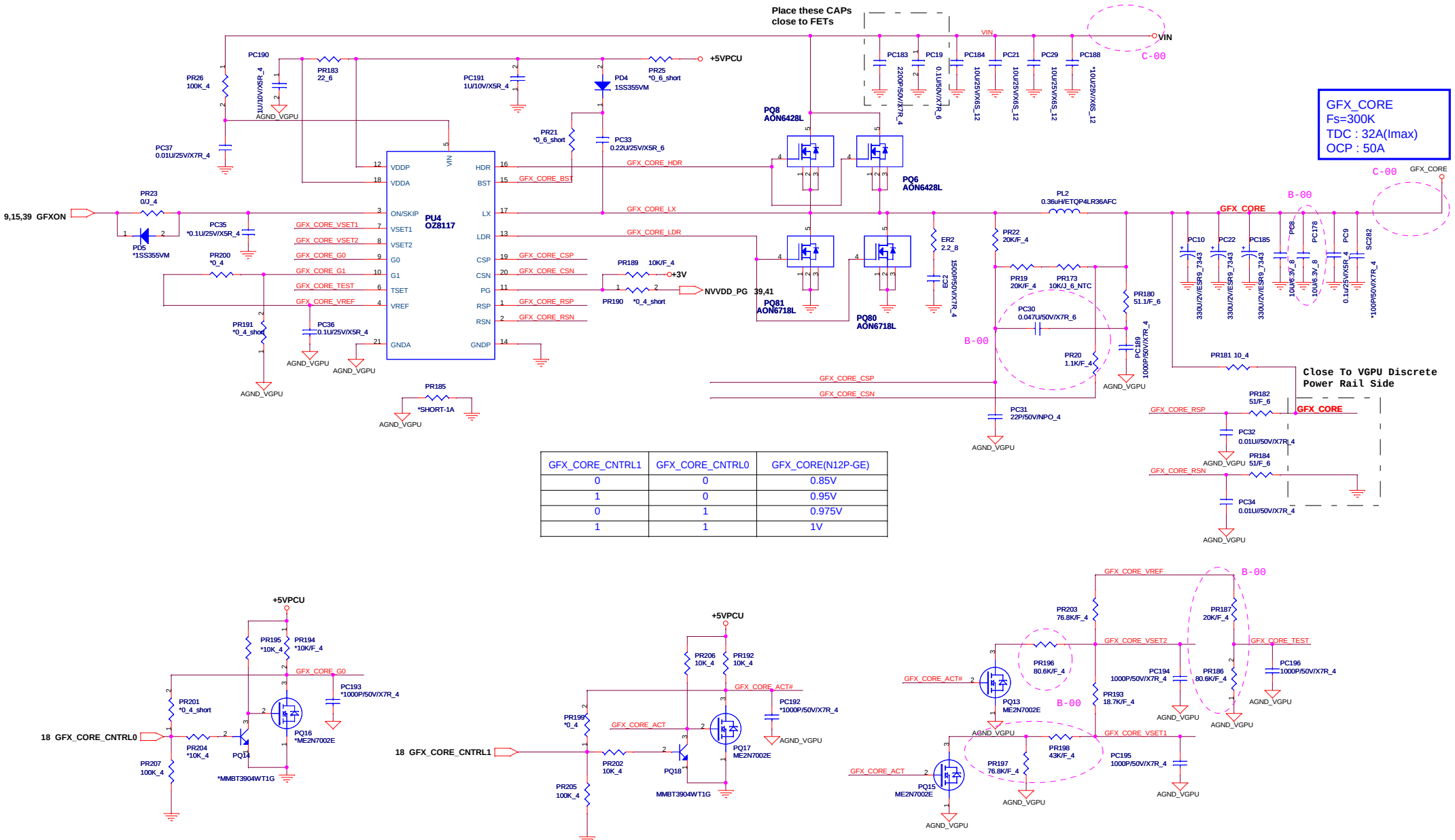

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	GFX_CORE(N12P-GE)
0	0	0.85V
1	0	0.95V
0	1	0.975V
1	1	1V

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Quanta Computer Inc.	
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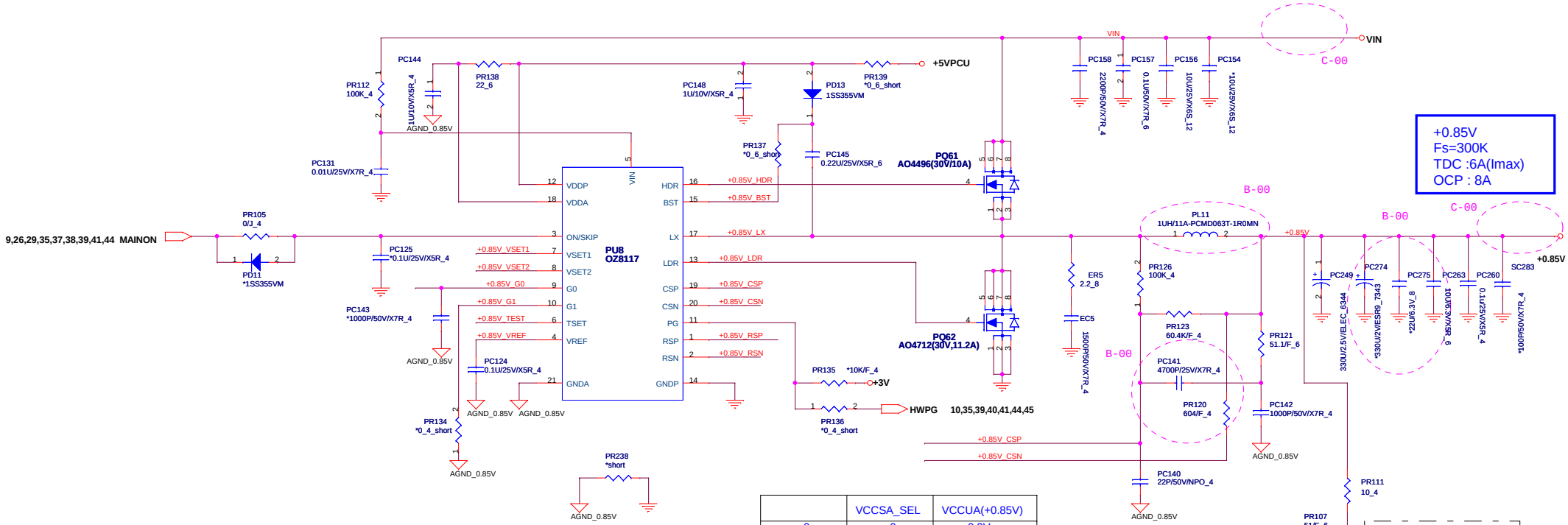
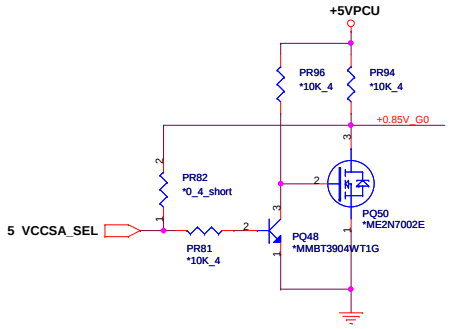
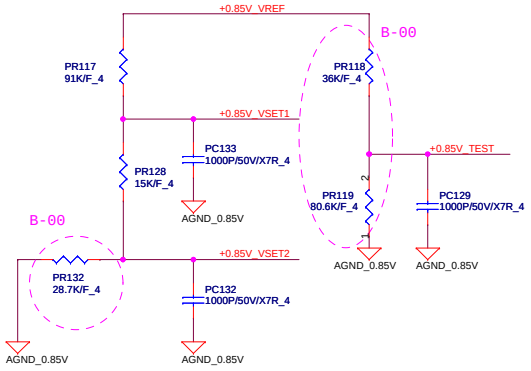
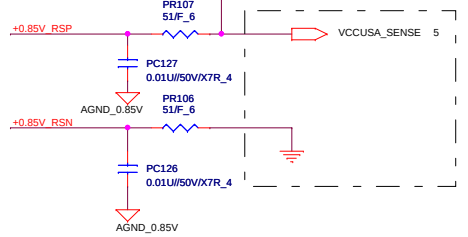


	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V







GND Close To Sandy Bridge Processor
(POWER) Side

Quanta Computer Inc.	PROJECT : KL6A		
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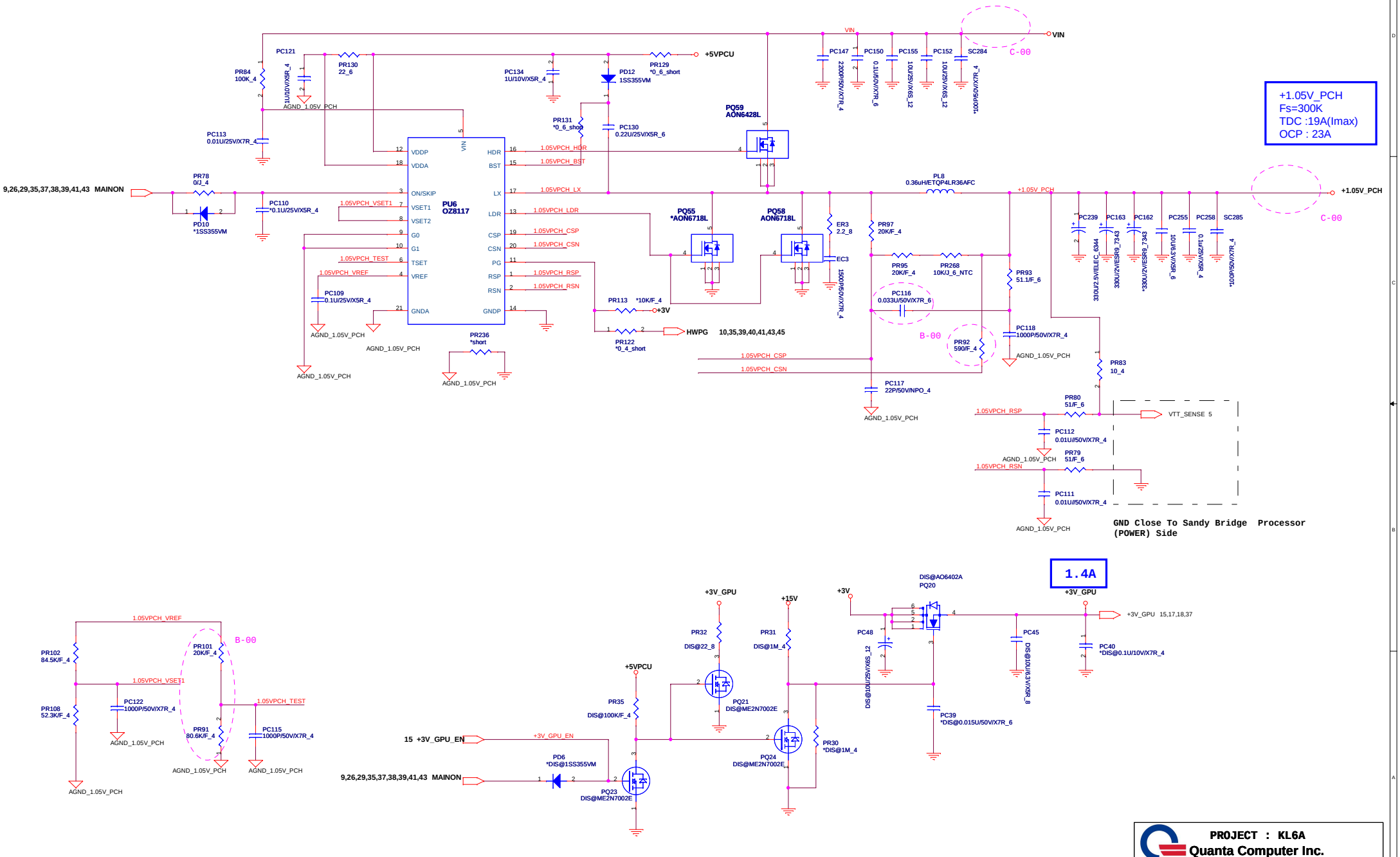
+1.05V_PCH
Fs=300K
TDC :19A(Imax)
OCP : 23A
PU6
OZ8117
PQ59
AON6428L
PQ55
*AON6718L
PQ58
AON6718L
PL8
0.36uH/ETQP4LR36AFC
9,26,29,35,37,38,39,41,43 MAINON
+1.05V_PCH
+5VPCU
VIN
+3V
HWPG 10,35,39,40,41,43,45
1.05VPCH_HDR
1.05VPCH_BST
1.05VPCH_LX
1.05VPCH_LDR
1.05VPCH_CSP
1.05VPCH_CSN
1.05VPCH_RSP
1.05VPCH_RSN
1.05VPCH_VSET1
1.05VPCH_TEST
1.05VPCH_VREF
AGND_1.05V_PCH
VTT_SENSE 5
GND Close To Sandy Bridge Processor (POWER) Side
1.4A
+3V_GPU
+3V_GPU 15,17,18,37
15 +3V_GPU_EN
+3V_GPU_EN
+15V
9,26,29,35,37,38,39,41,43 MAINON
DIS@AO6402A
PQ20
PQ21
DIS@ME2N7002E
PQ24
DIS@ME2N7002E
PQ23
DIS@ME2N7002E
PD6
*DIS@1SS355VM
PD10
*1SS355VM
PD12
1SS355VM
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Quanta Computer Inc.
+1.05_PCH (OZ8115)
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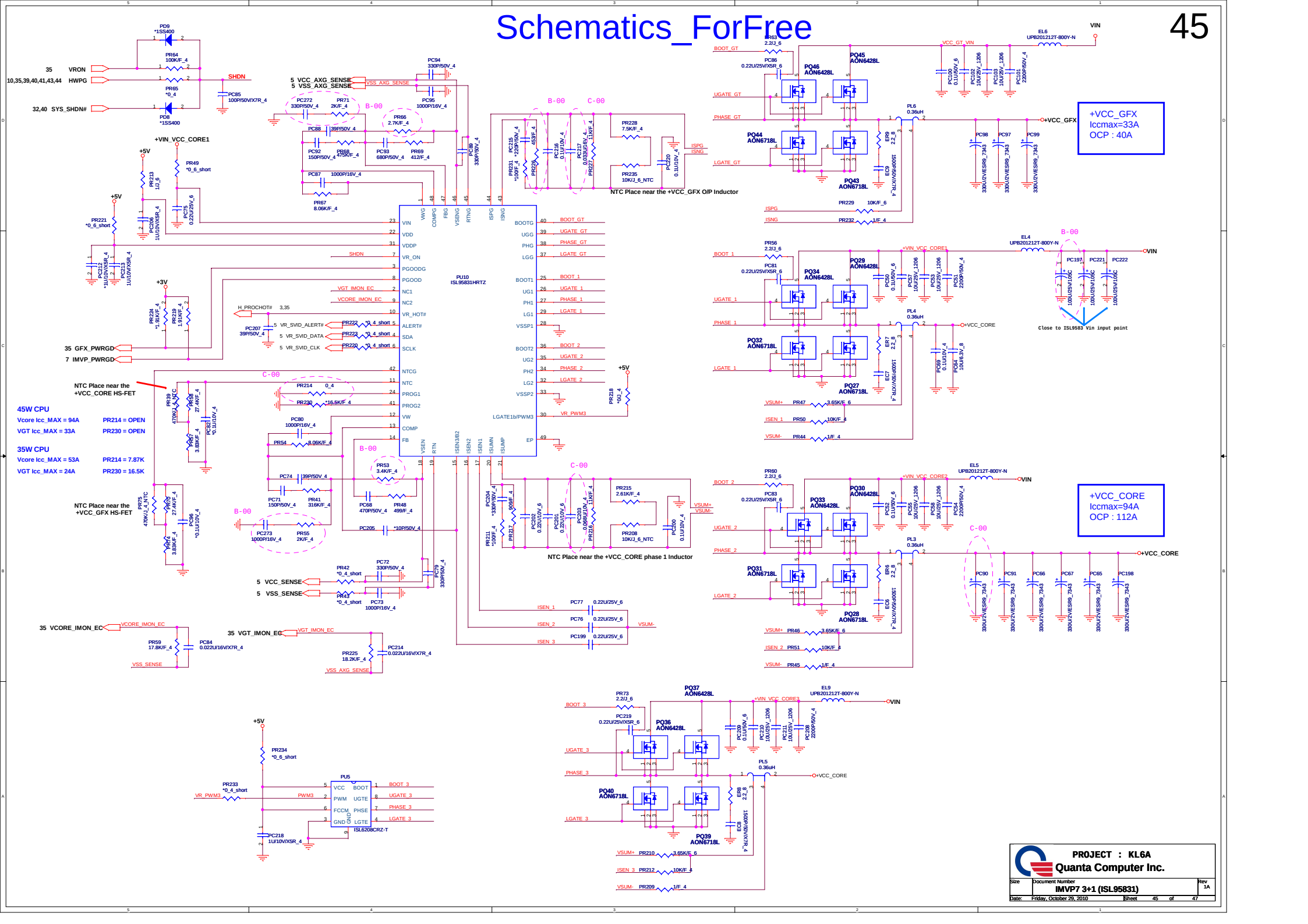
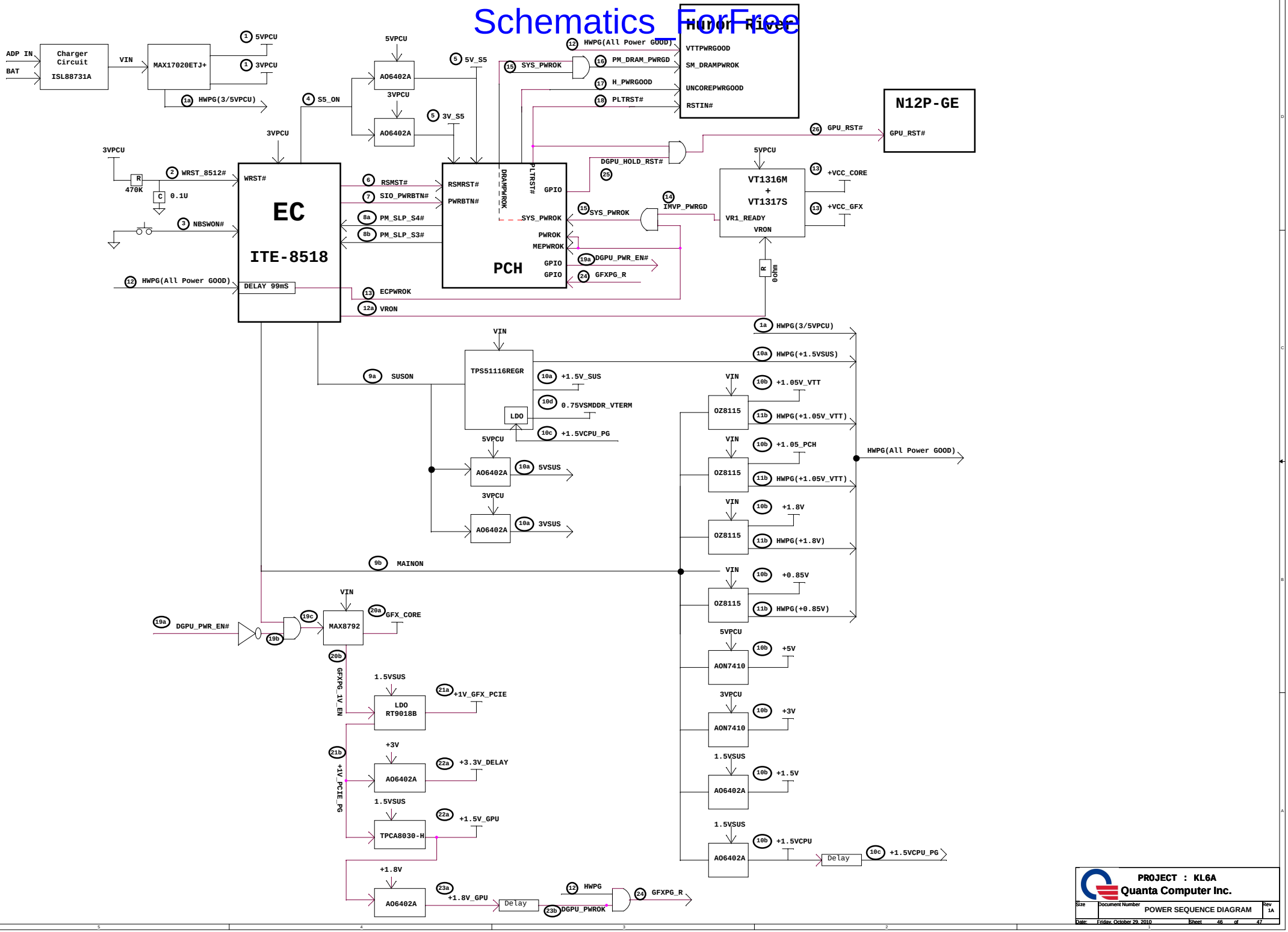


Schematics ForFree



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Quanta Computer Inc.

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	POWER SEQUENCE DIAGRAM	1A

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KL6A / Z470 Huron River Schematic EC Tracking Record A (for SIV --> SIT C)October 18, 2010

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EC #	Page	CMVC #	Description	Date	Part Affected
C-00	1~46		Remove 0ohm resistor	1018	
C-01	9		Remov 27MHz from PCH	1018	
C-02	28,32, 34,36		Add capacitor for ESD/EMI suggestion	1018	

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Custom	EC Tracking Record A	1A

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