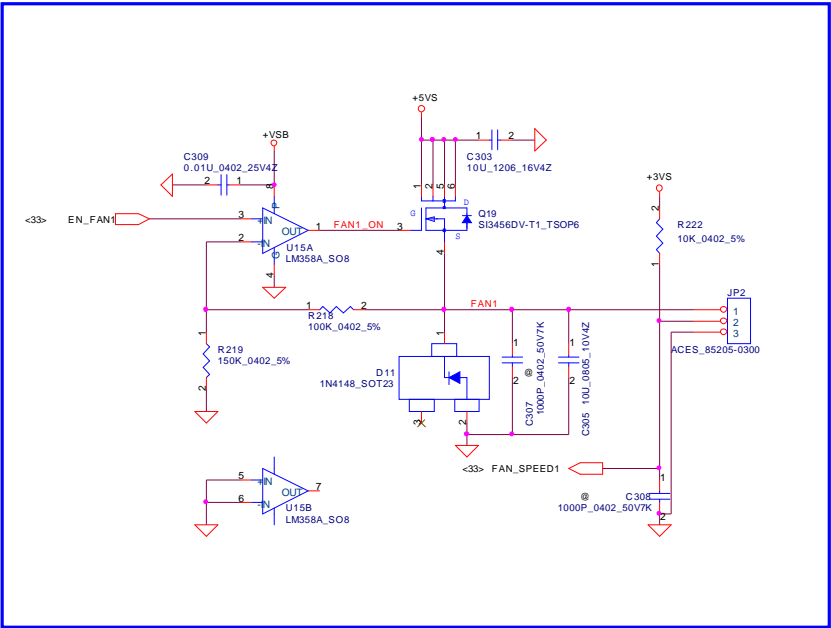
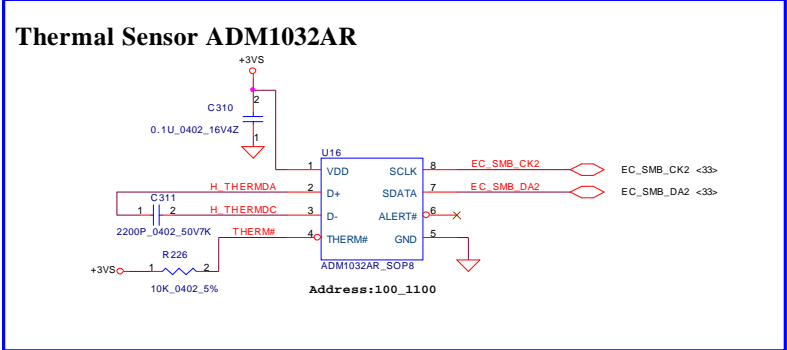
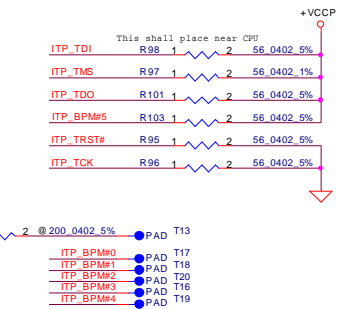
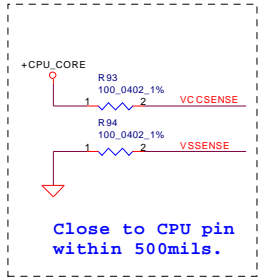
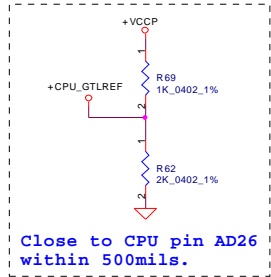


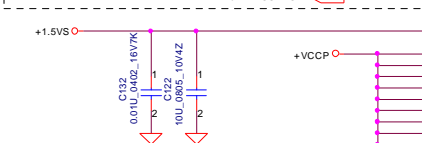
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil



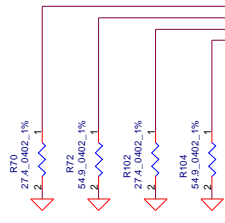
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title Yonah CPU in mFCPGA479	
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Size	Document Number	Customer		Rev	
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Date	Monday, November 28, 2005	Sheet	4	of 45	



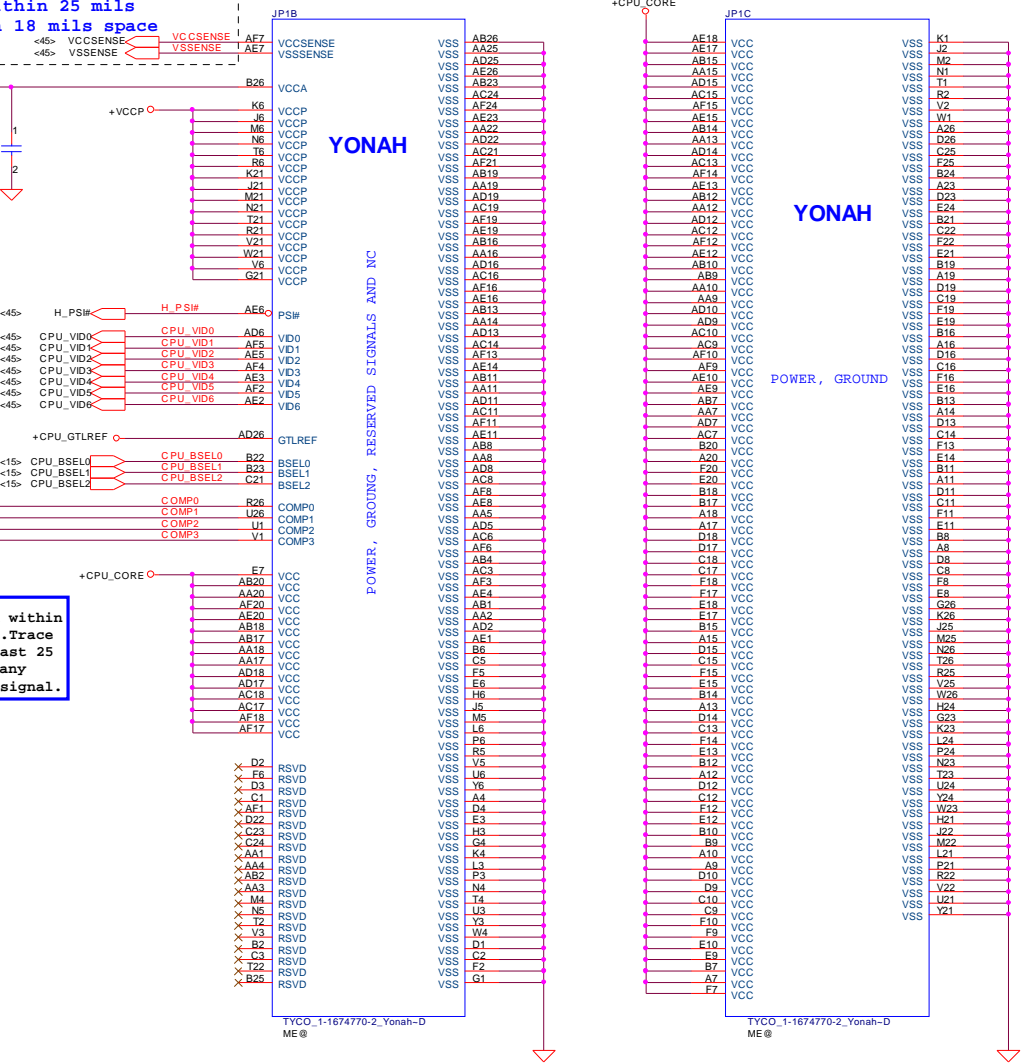
Length match within 25 mils
The trace width 18 mils space
7 mils



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

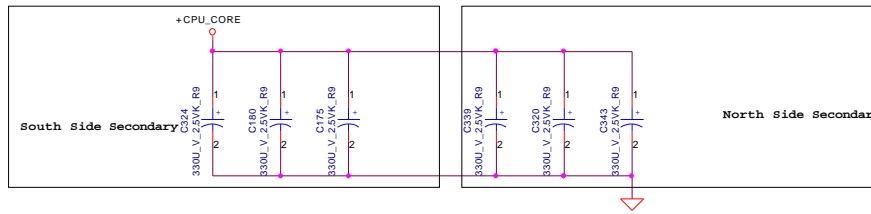
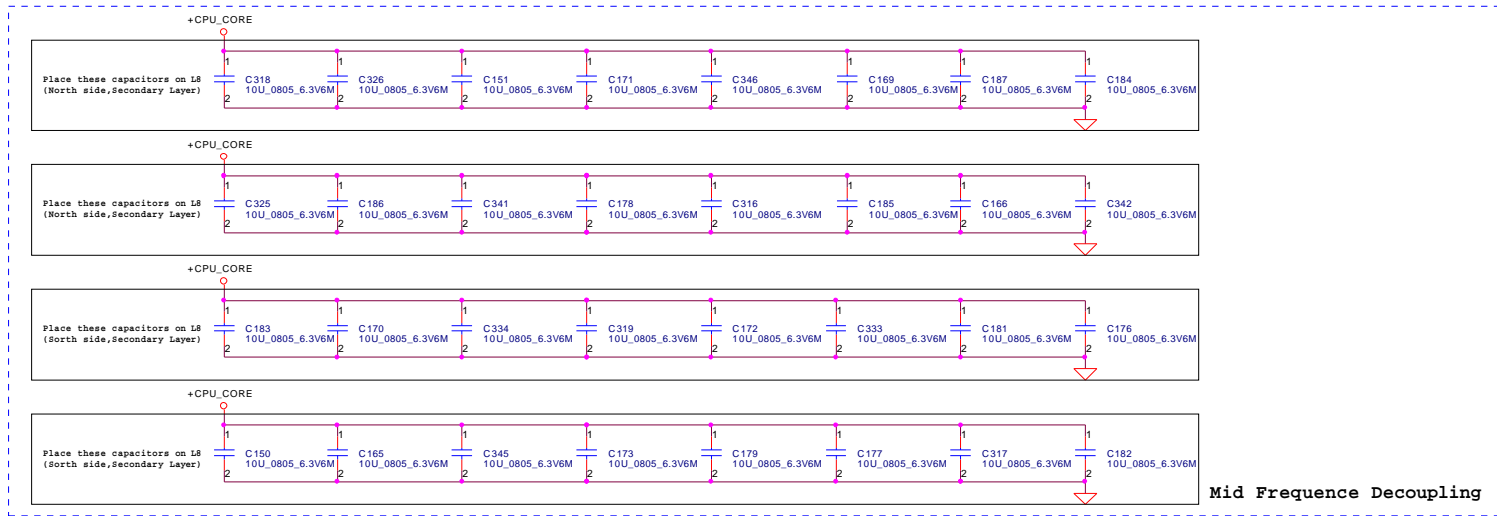


Resistor placed within
0.5" of CPU pin. Trace
should be at least 25
mils away from any
other toggling signal.

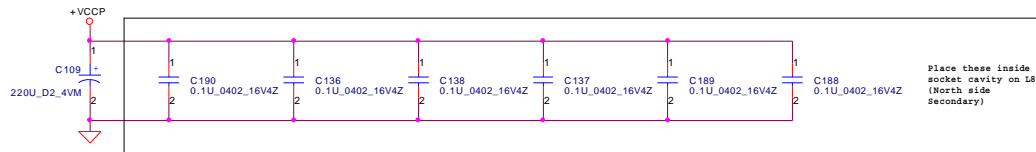


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Compal Electronics, Inc.		
Yonah CPU in mFCPGA479		
Size	Document Number	Rev
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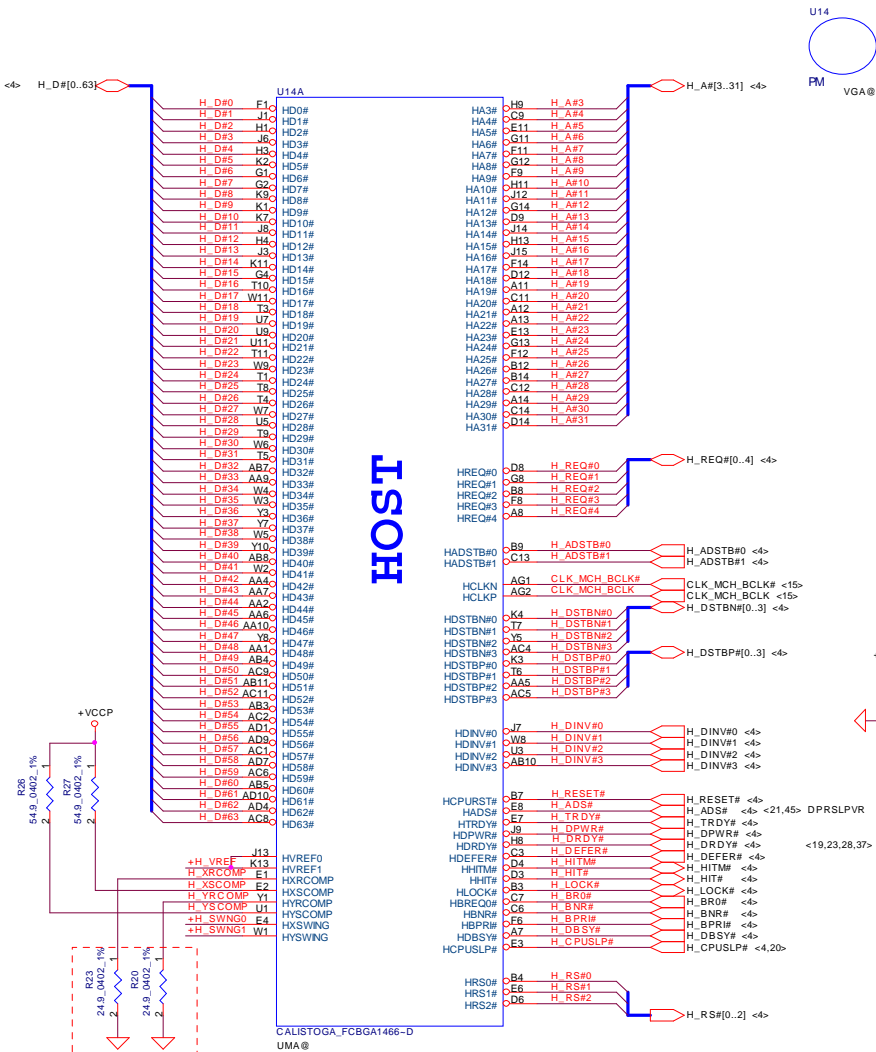


ESR <= 1.5m ohm
Capacitor > 1980uF

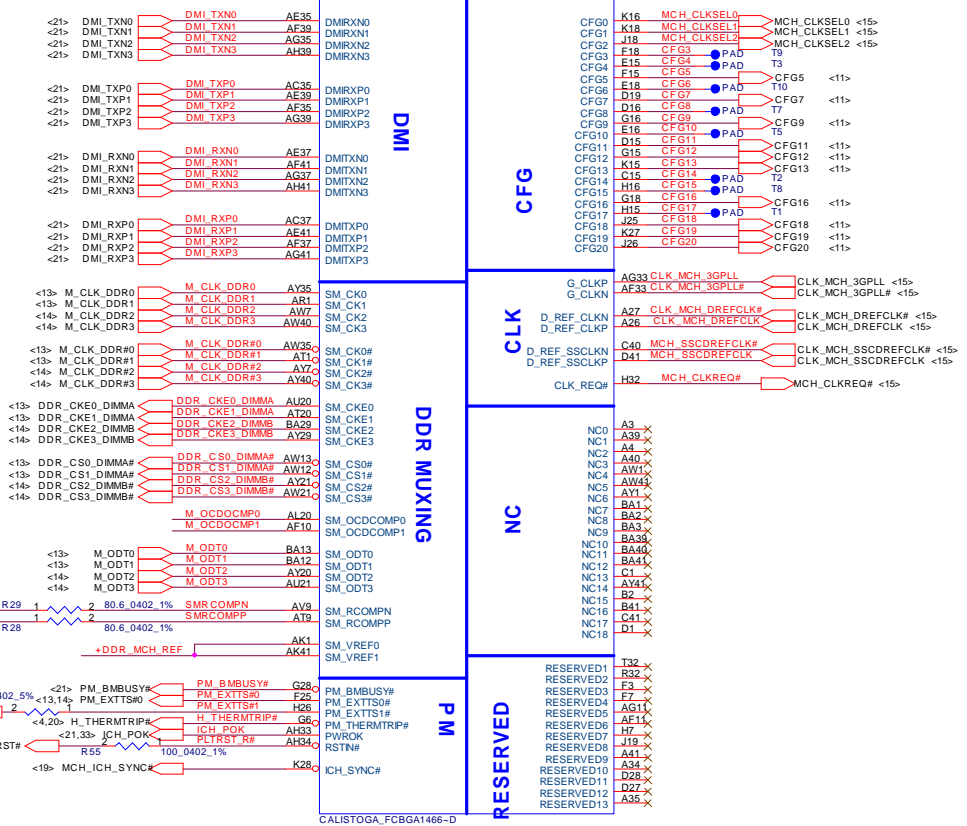


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Compal Electronics, Inc.		
CPU Bypass capacitors		
Size	Document Number	Rev
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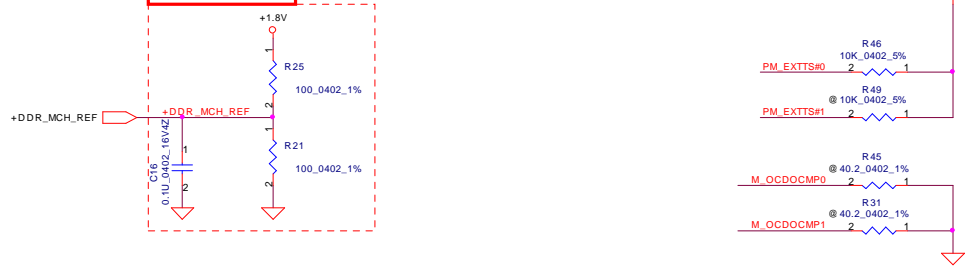
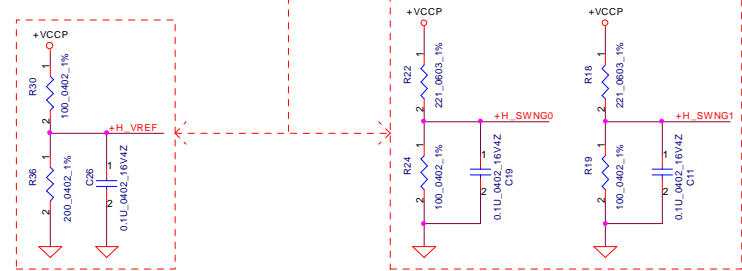


Description at page 15



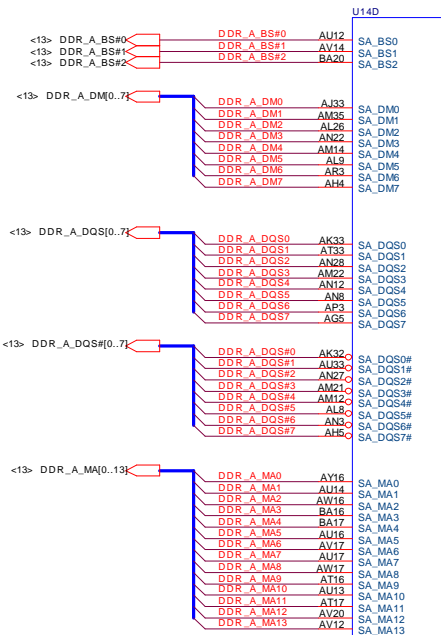
Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20.

Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 10/20.



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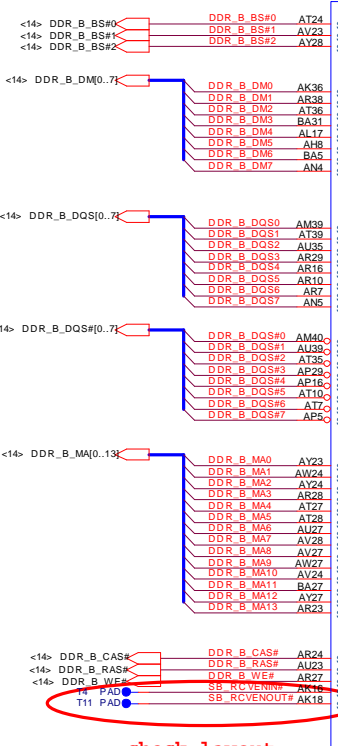
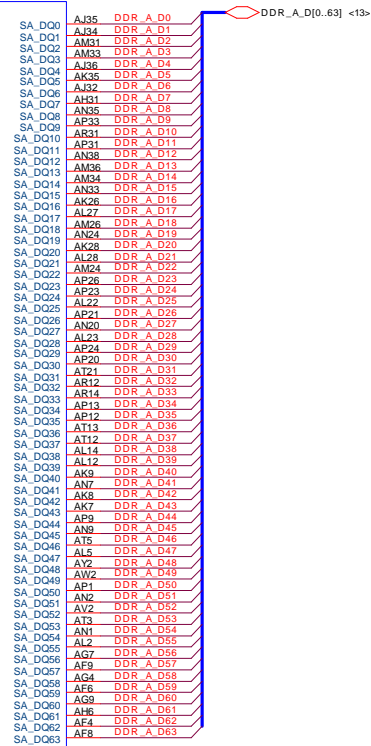
Compal Electronics, Inc.		
Calistoga (1/6)		
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	HGT30/31 LA-3061	0.1
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DDR SYS MEMORY A

CALISTOGA_FCBGA1466-D
UMA@

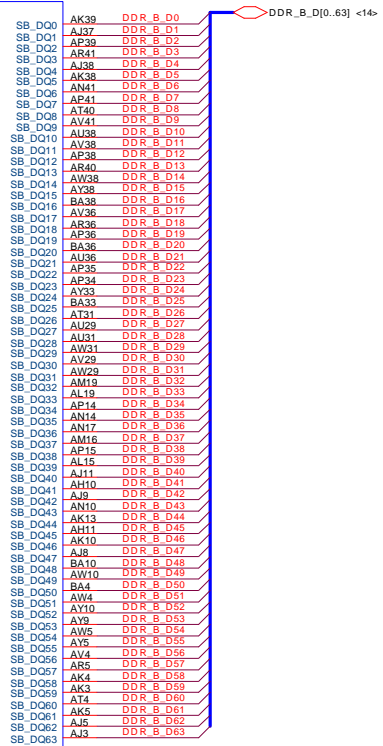
check layout



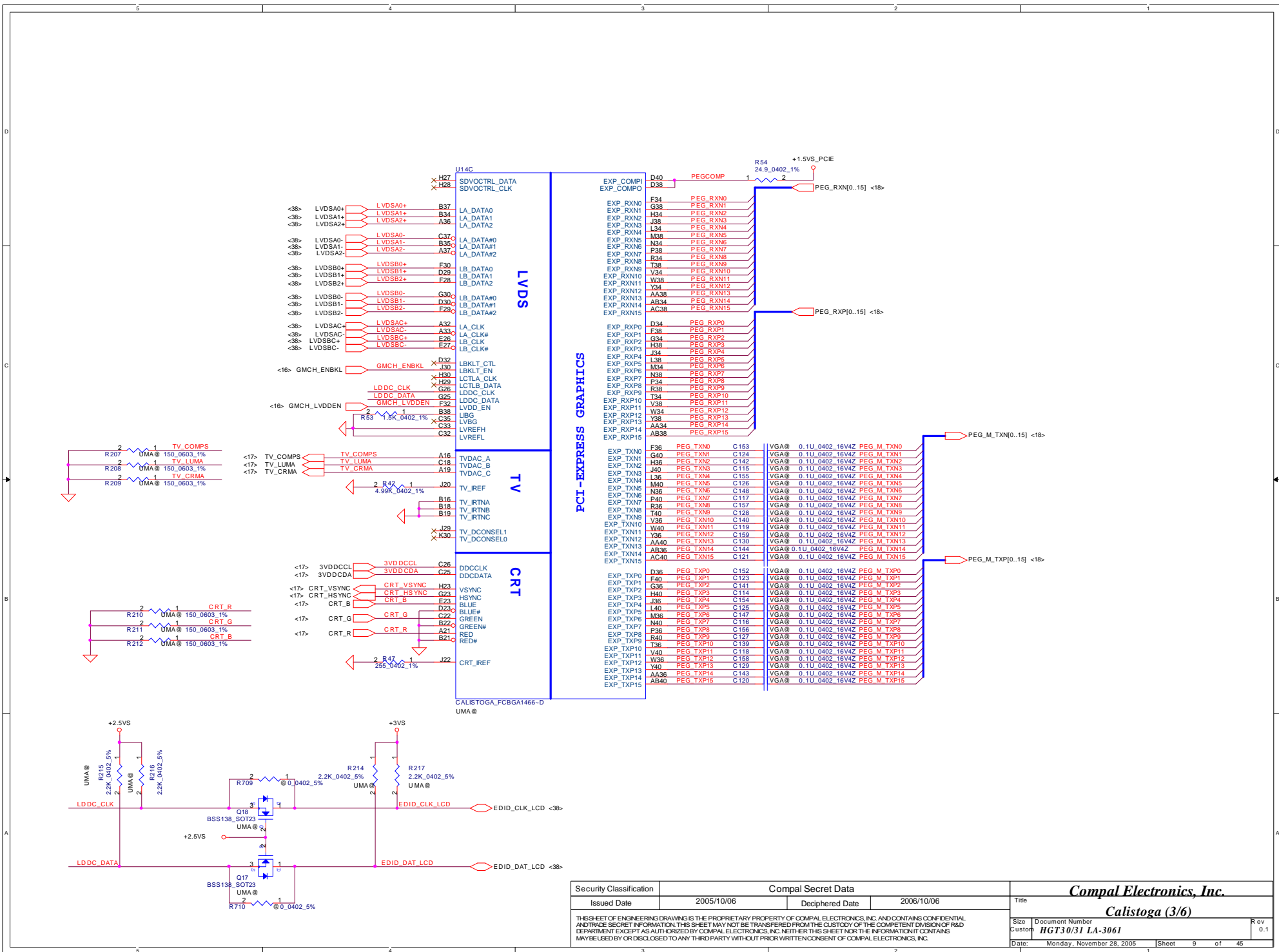
DDR SYS MEMORY B

CALISTOGA_FCBGA1466-D
UMA@

check layout

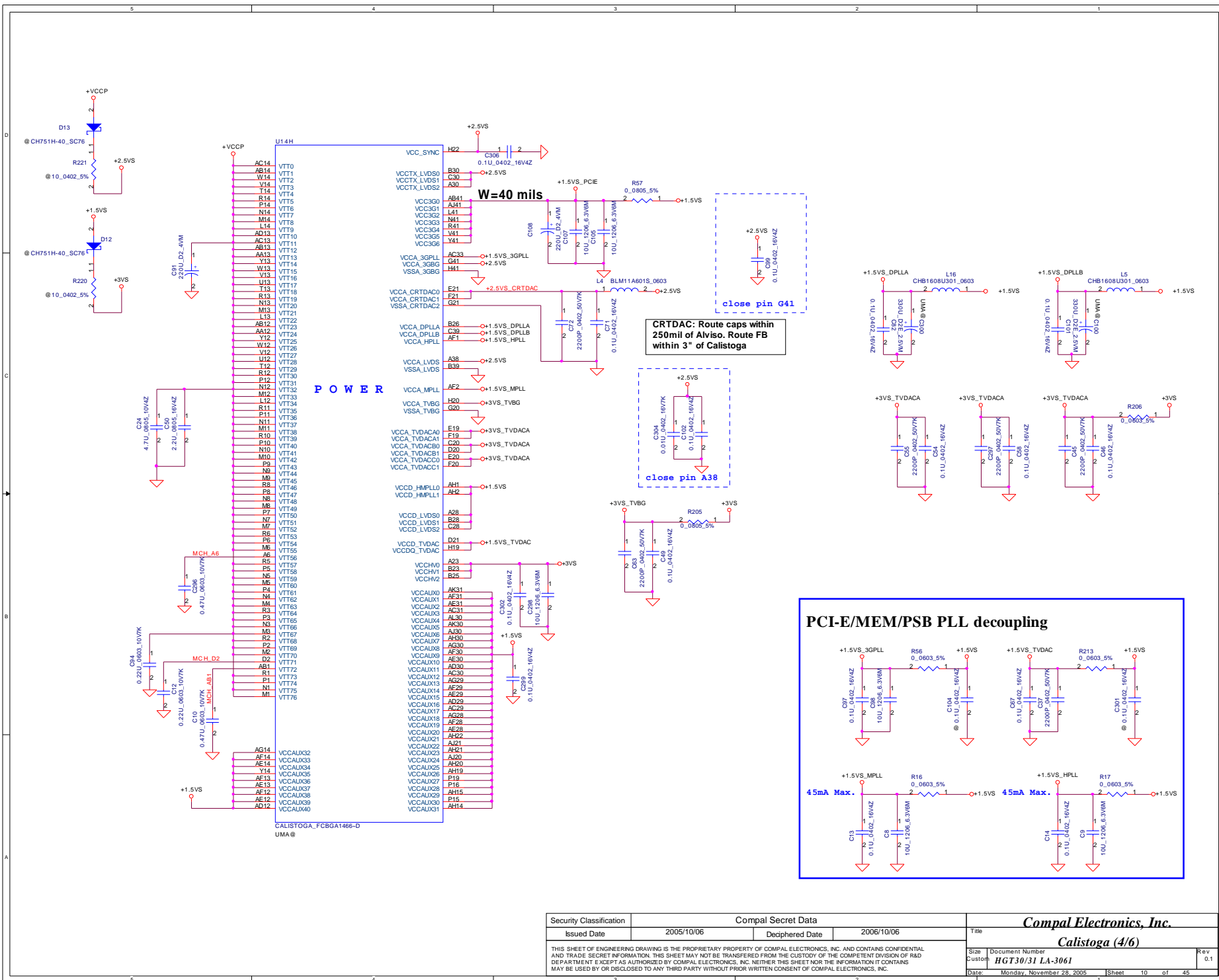


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Title Calistoga (3/6)		
Size	Document Number	Rev
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Date:	Monday, November 28, 2005	Sheet 9 of 45



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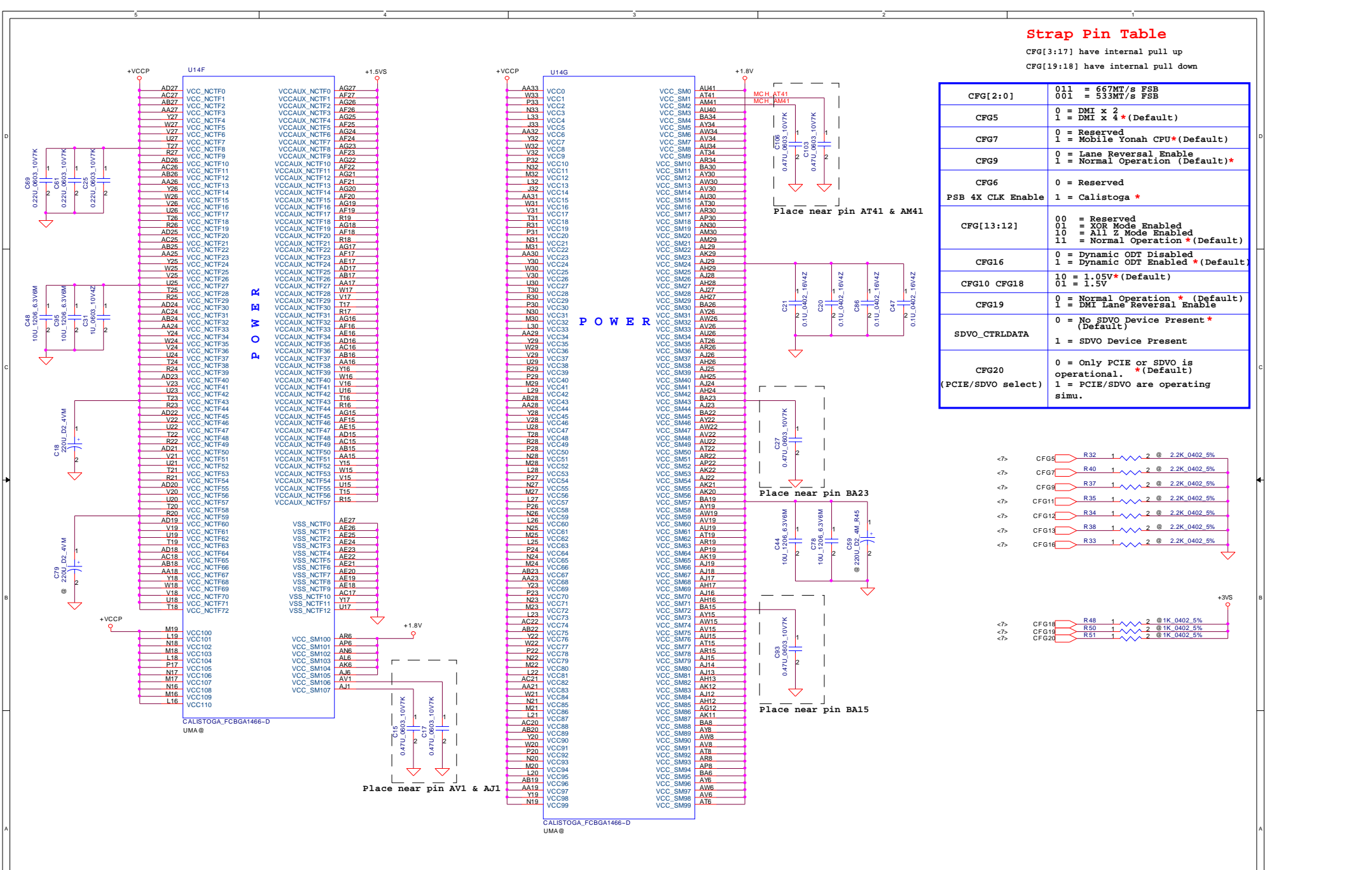
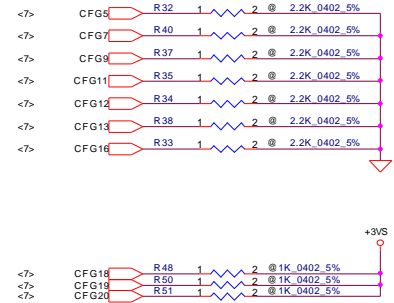
Title		Compal Electronics, Inc.	
		Calistoga (4/6)	
Size	Document Number	Rev	
Position	HGT30/31 LA-3061	0.1	
Date	Monday, November 28, 2005	Sheet	10 of 45

Strap Pin Table

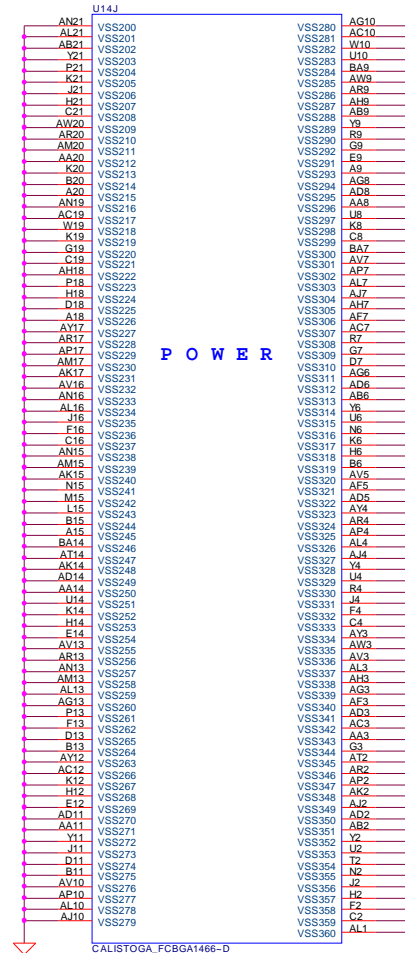
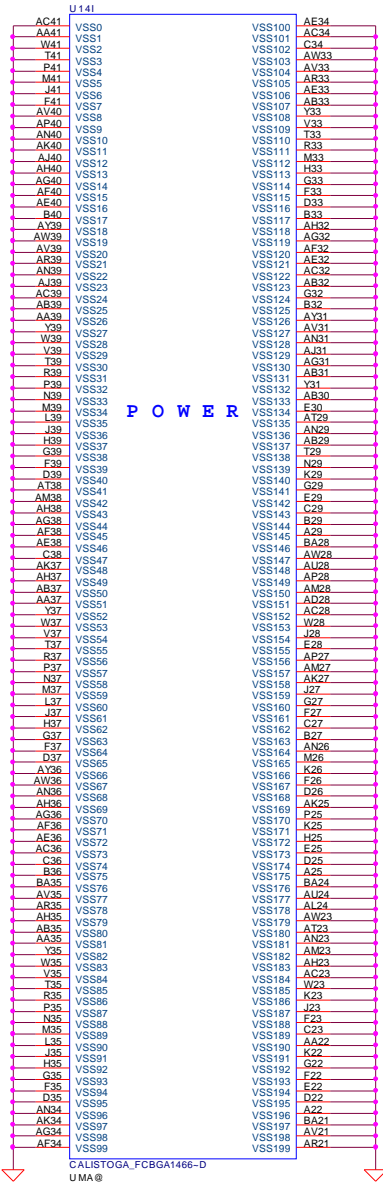
CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default) *
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG10 CFG18	10 = 1.05V * (Default) 01 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.

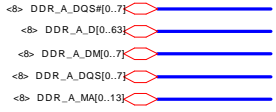


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Size	Document Number	Rev		
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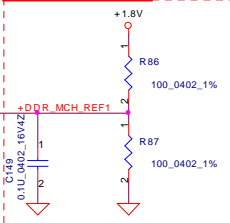


POWER

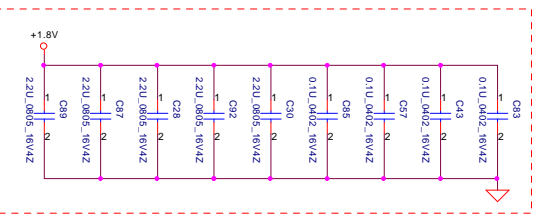
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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title
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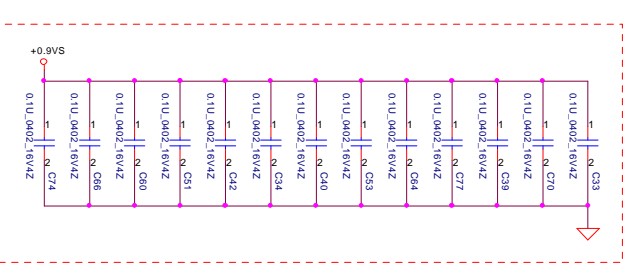
Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20.



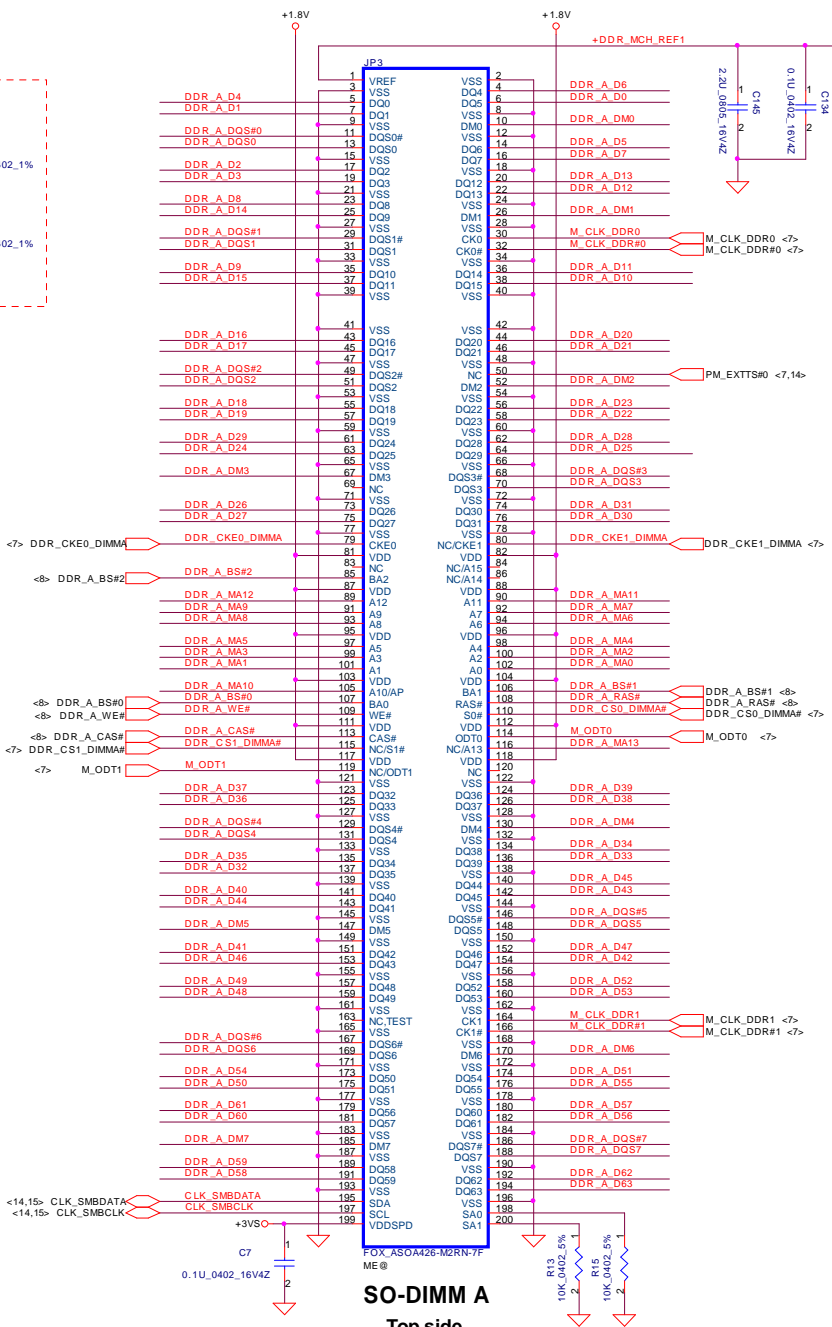
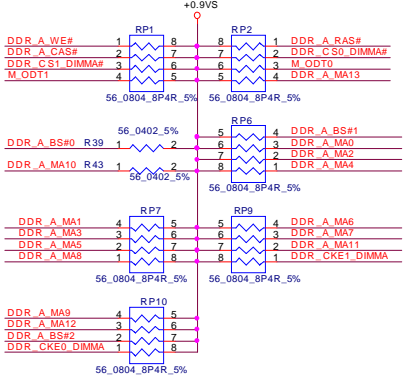
Layout Note:
Place near JP41



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



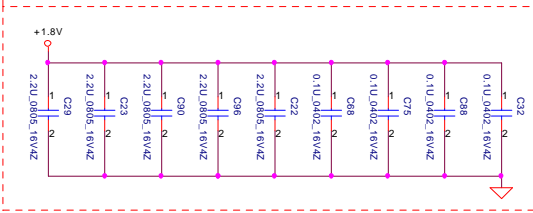
Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"



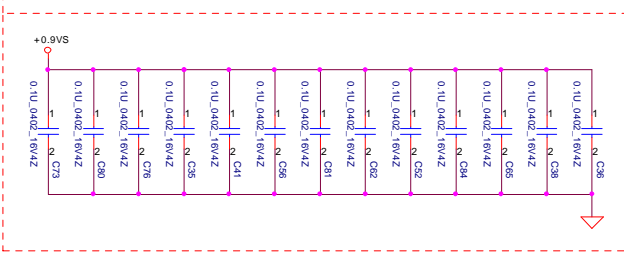
Security Classification	Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date
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- <8> DDR_B_DQS#[0..7]
- <8> DDR_B_D[0..63]
- <8> DDR_B_DM[0..7]
- <8> DDR_B_DQS[0..7]
- <8> DDR_B_MA[0..13]

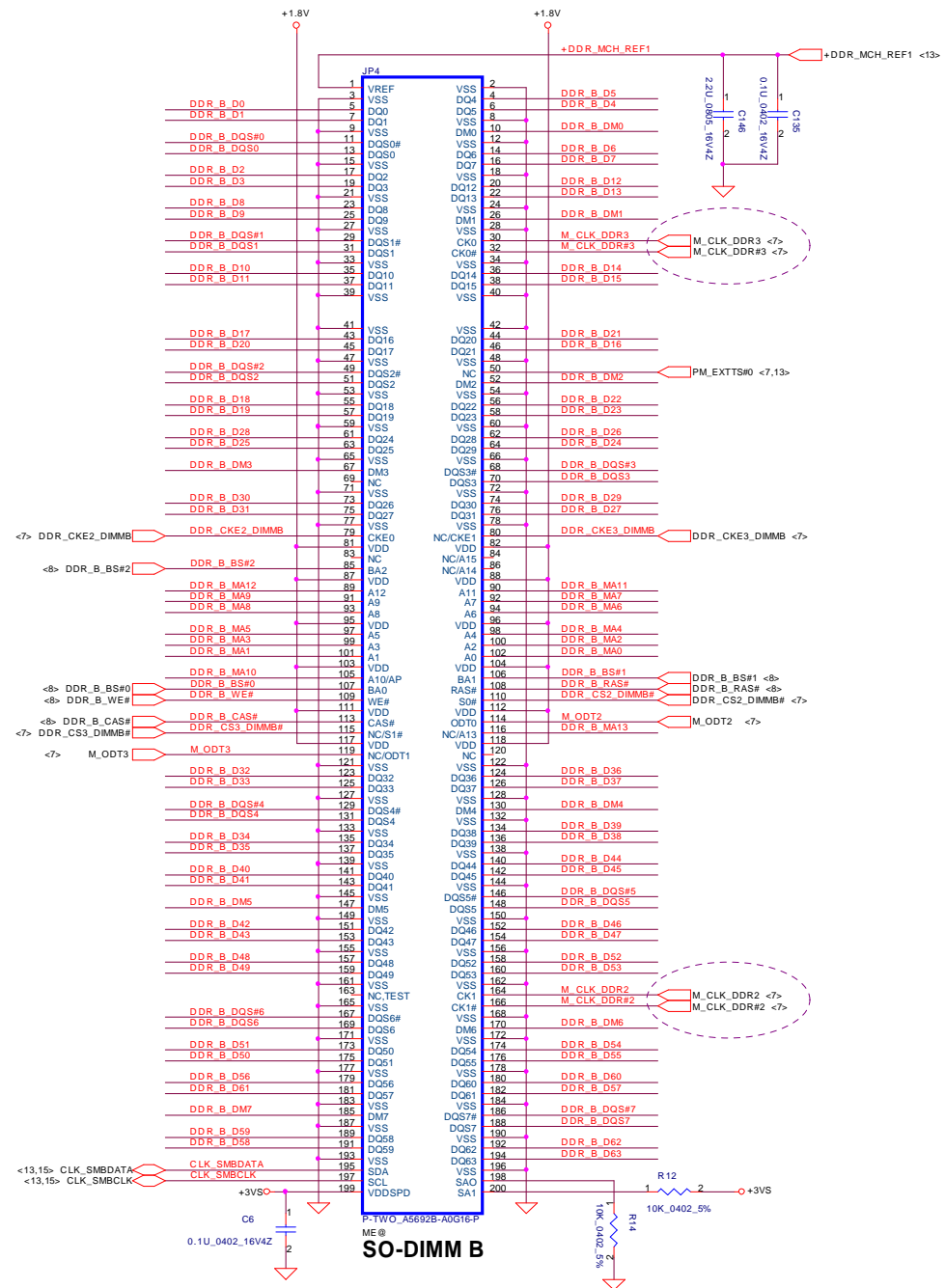
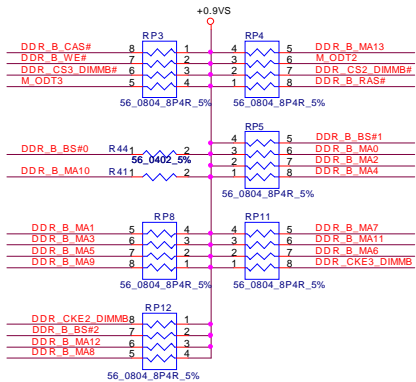
Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



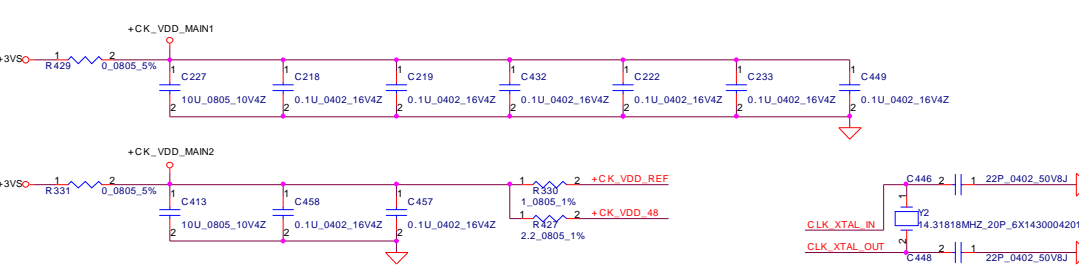
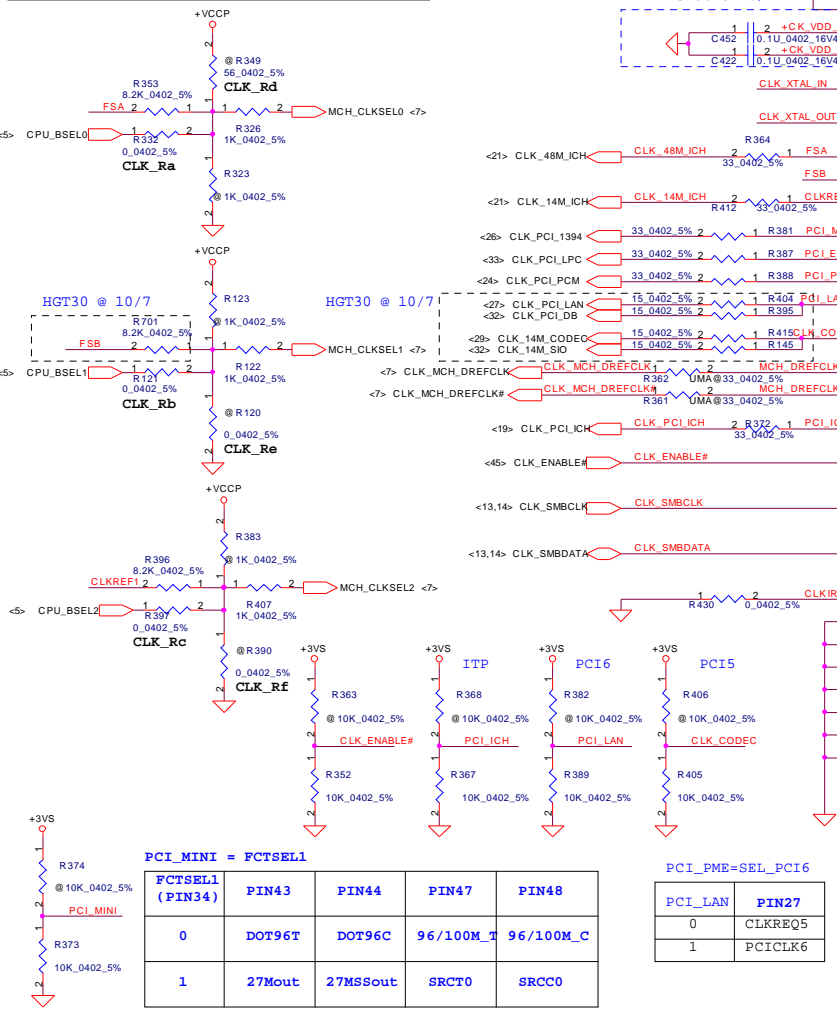
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				DDR2-SODIMM SLOT2	
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

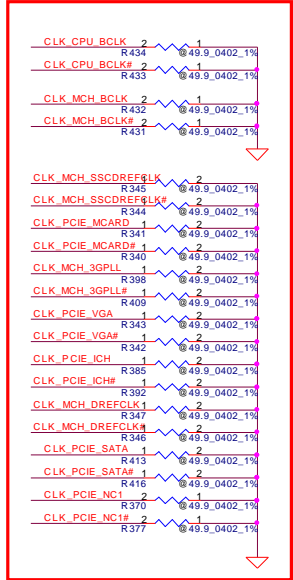
FSB Frequency Set:

CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
*(Default)	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
533MHz	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	Stuff	CLK_Rd	CLK_Re	CLK_Rf
667MHz	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	Stuff	CLK_Rd	CLK_Re	CLK_Rf



Place crystal within 500 mils of CK410

Place near U4
Place these components near each pin within 40 mils.



PCI_MINI = FCTSEL1

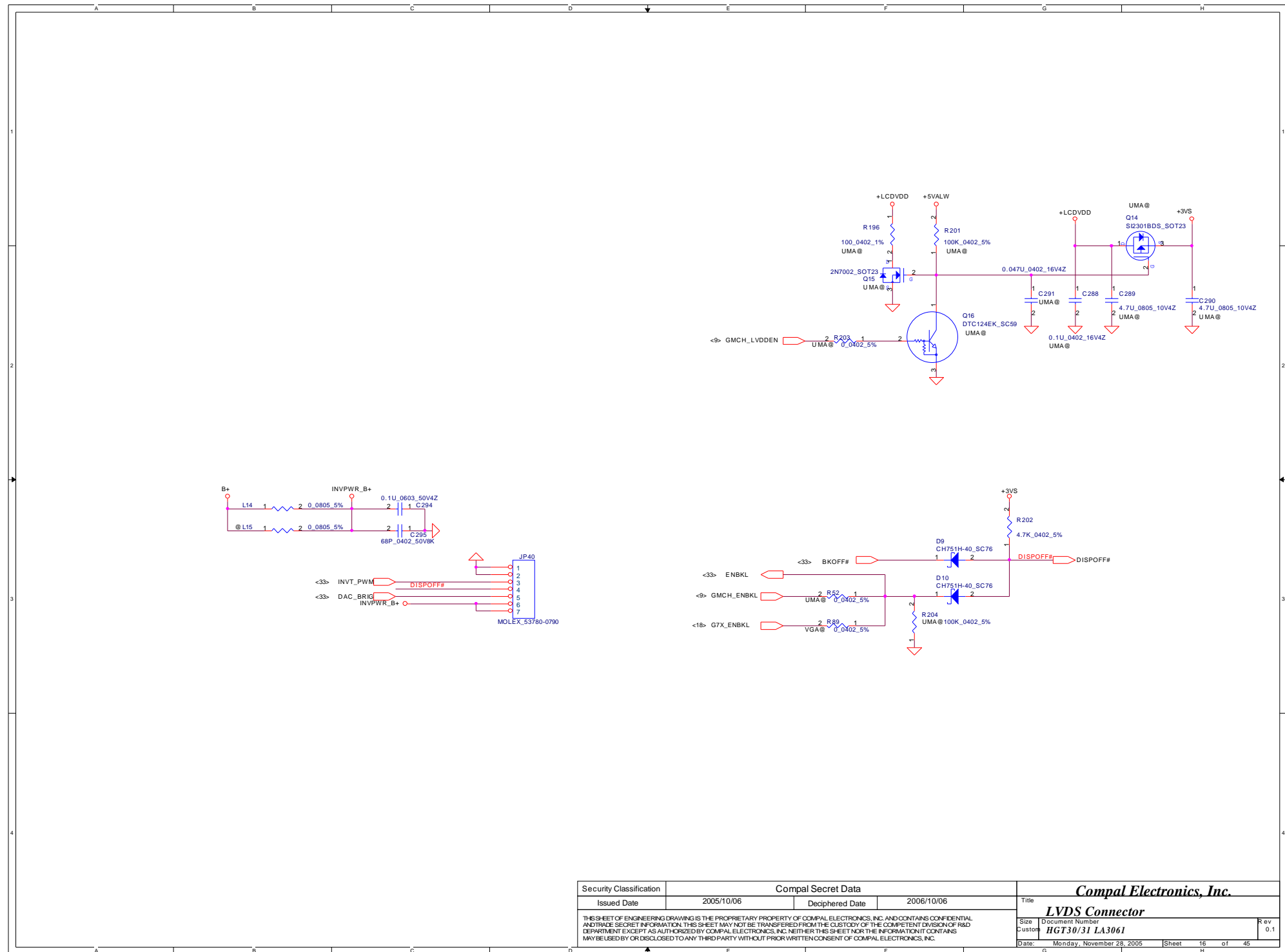
FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27Mout	27MSout	SRC0	SRCC0

PCI_PMB=SEL_PCI6

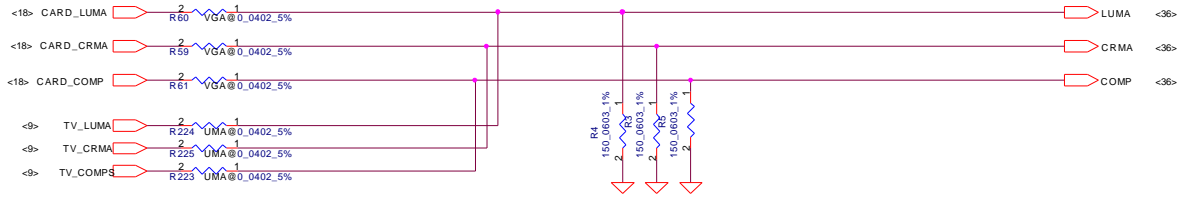
PCI_LAN	PIN27
0	CLKREQ5
1	PCICLK6

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Compal Electronics, Inc.			
Clock generator			
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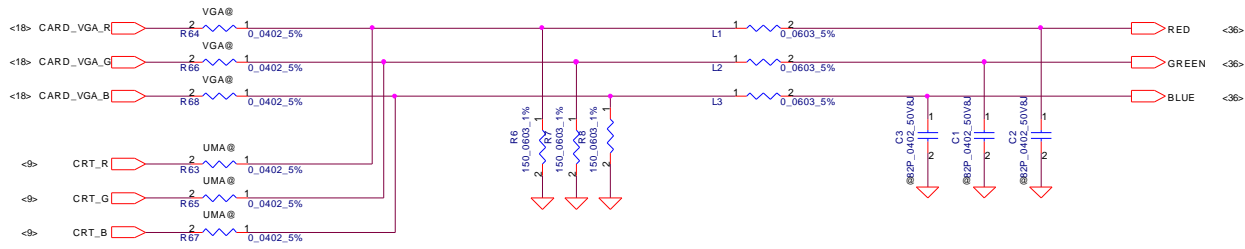


TV-OUT Conn.

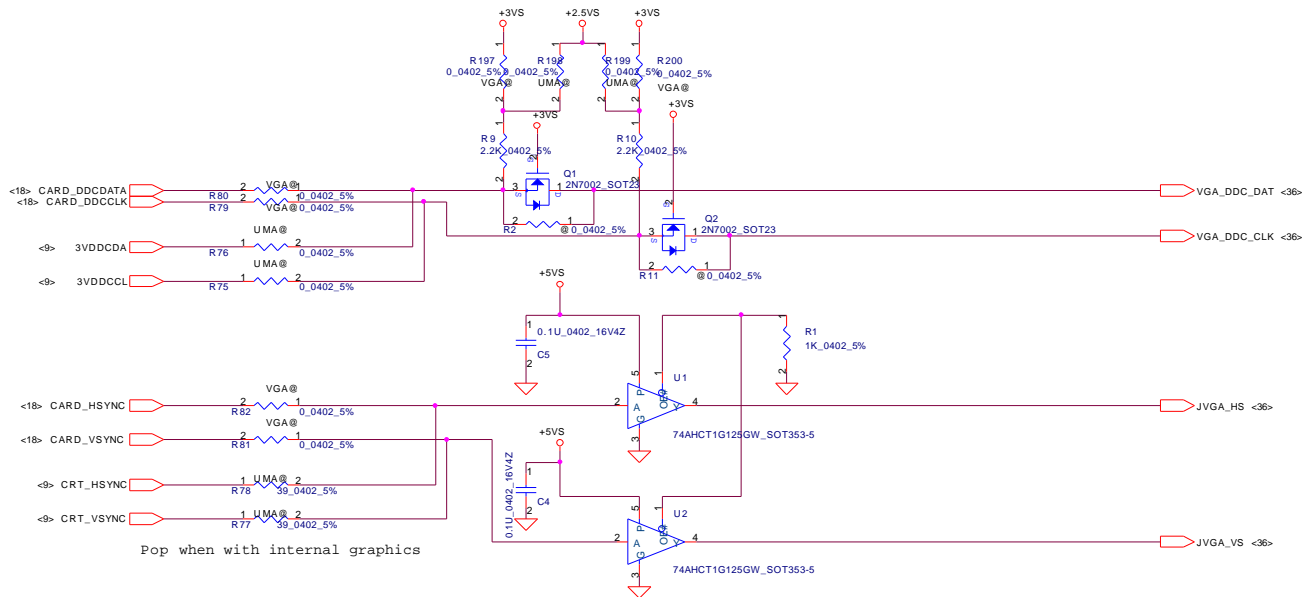


Pop when with internal graphics

CRT Conn.



Pop when with internal graphics



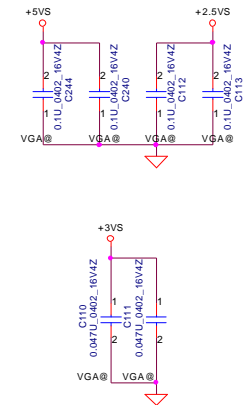
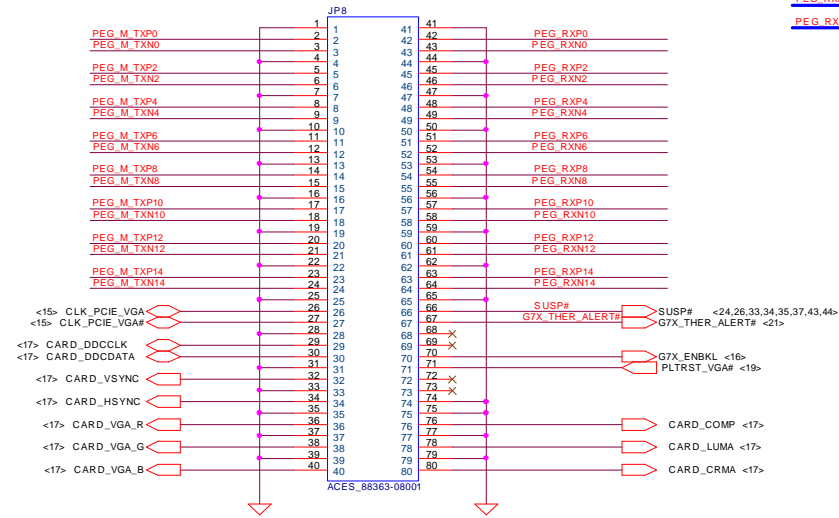
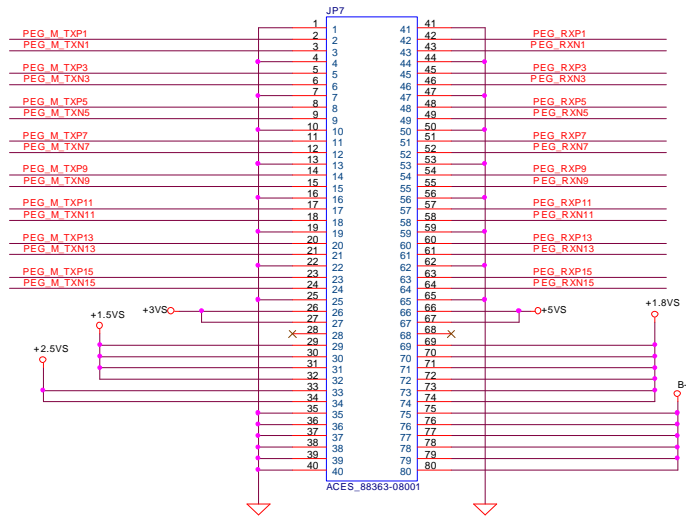
Pop when with internal graphics

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Compal Electronics, Inc.		
CRT & TVout		
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MAX. 4.06A @ 1.8V
 MAX. 130mA @ 2.5V
 MAX. 655mA @ 3.3V

PEG_M_TXP[0..15] PEG_M_TXP[0..15] <@>
 PEG_M_TXN[0..15] PEG_M_TXN[0..15] <@>
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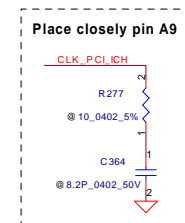
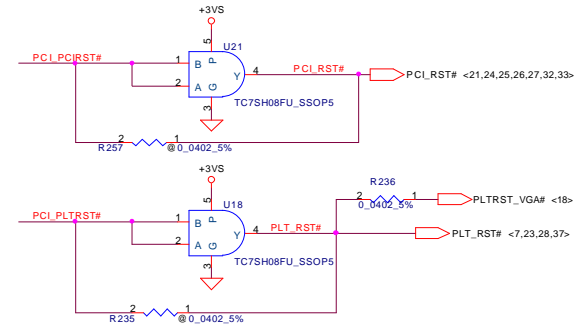
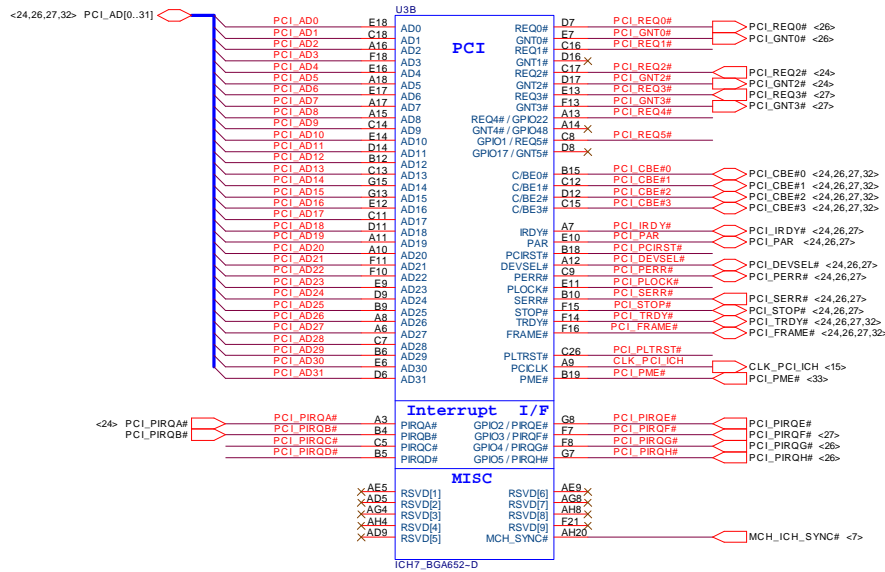
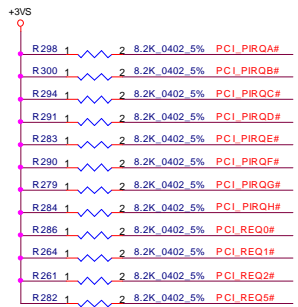
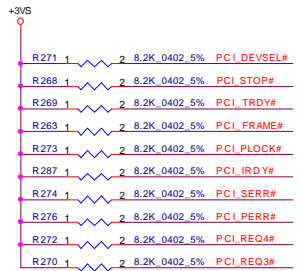


Compal Electronics, Inc.

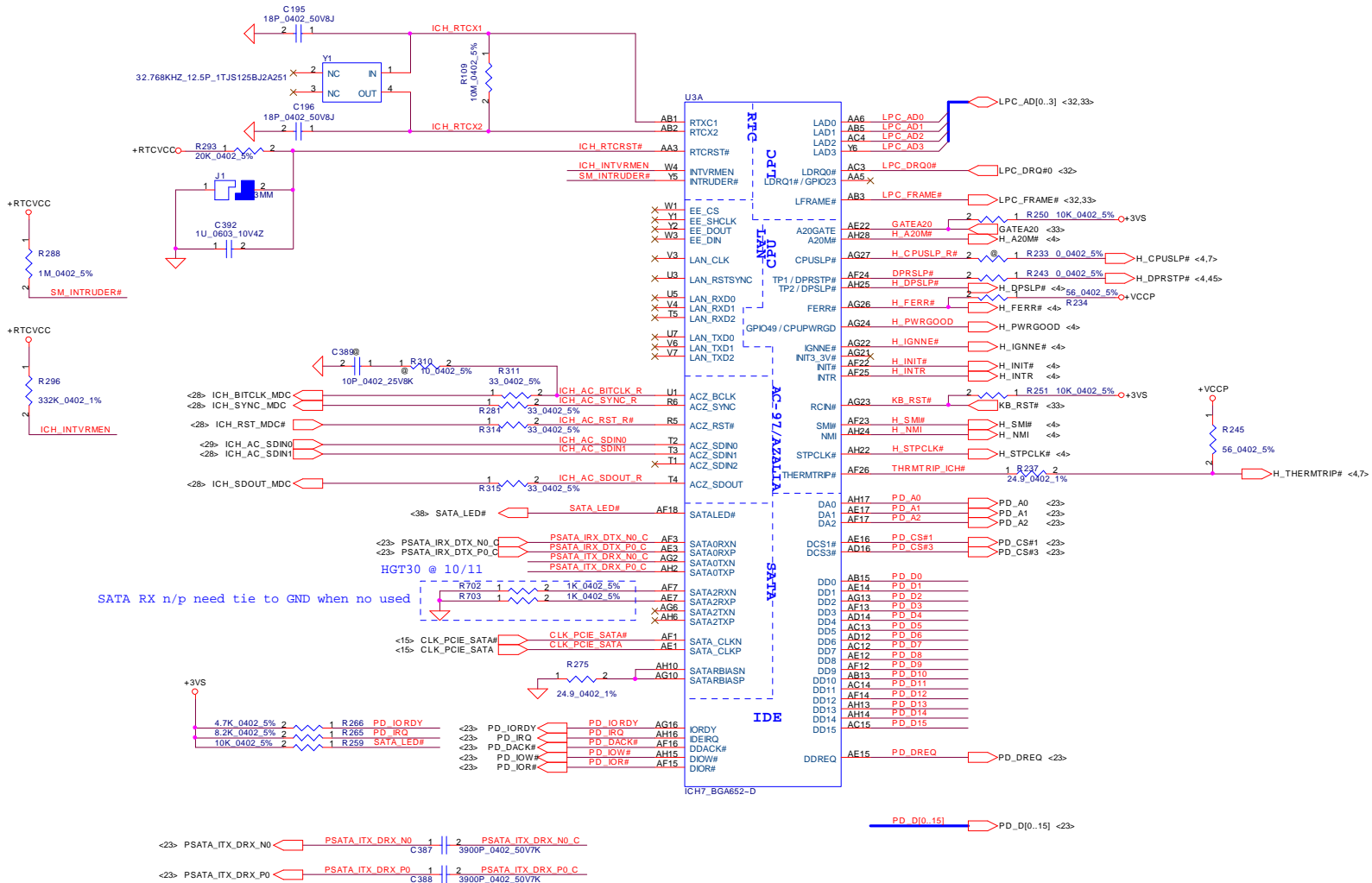
VGA/B connector

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Size	Document Number	HGT30/31 LA3061		
Customer				
Date:	Monday, November 28, 2005	Sheet	18	of 45

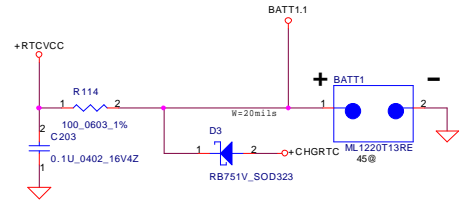
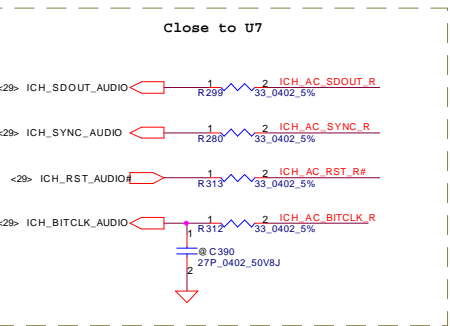
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				Rev 0.1

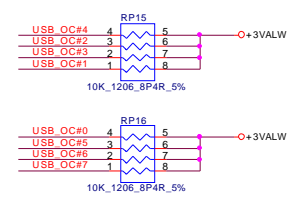
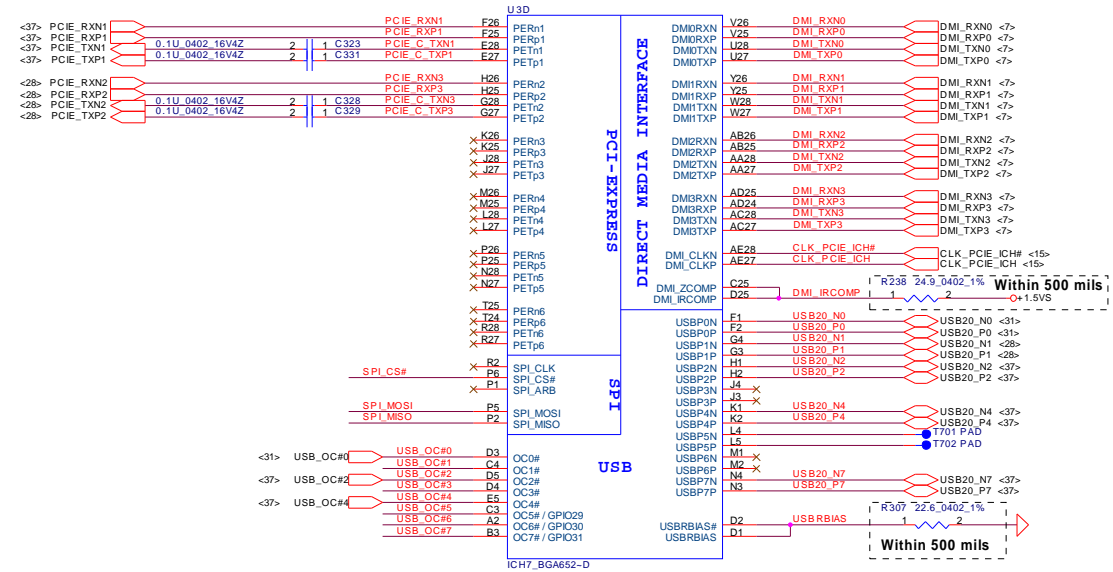
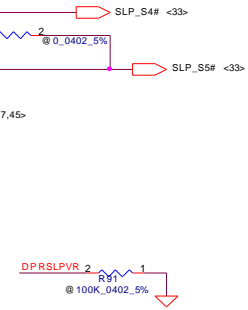
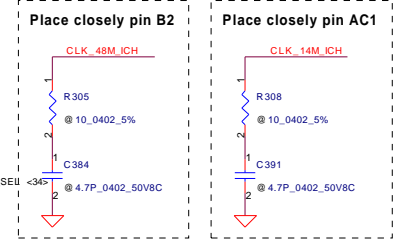
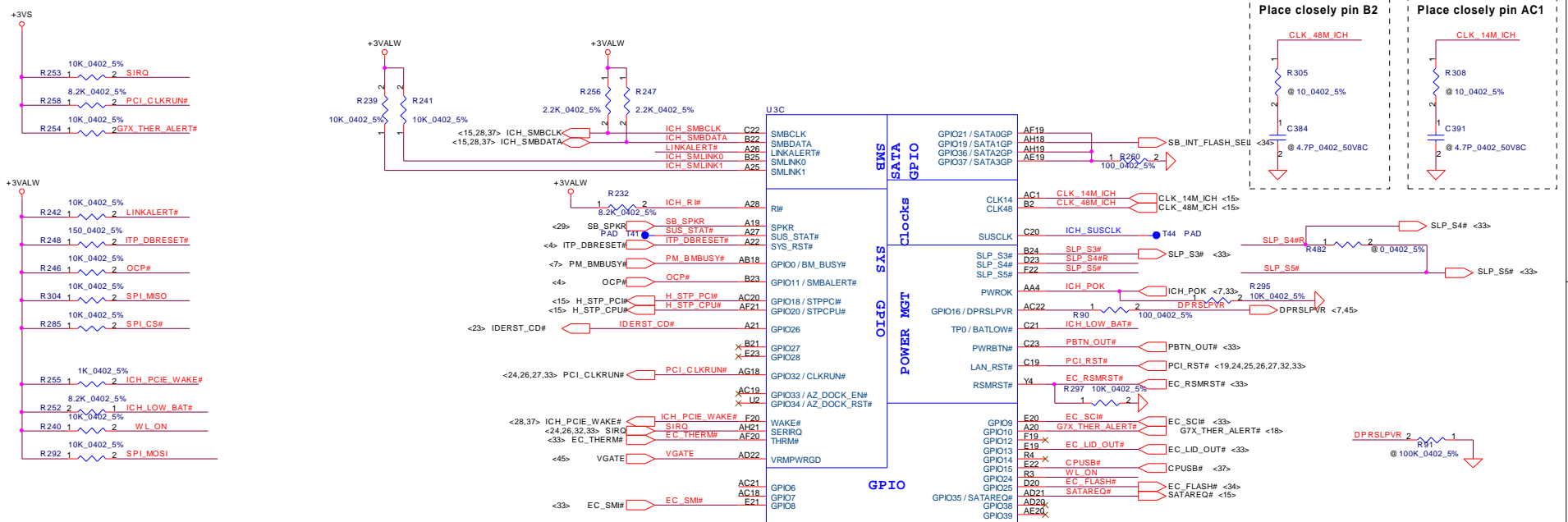


SATA RX n/p need tie to GND when no used

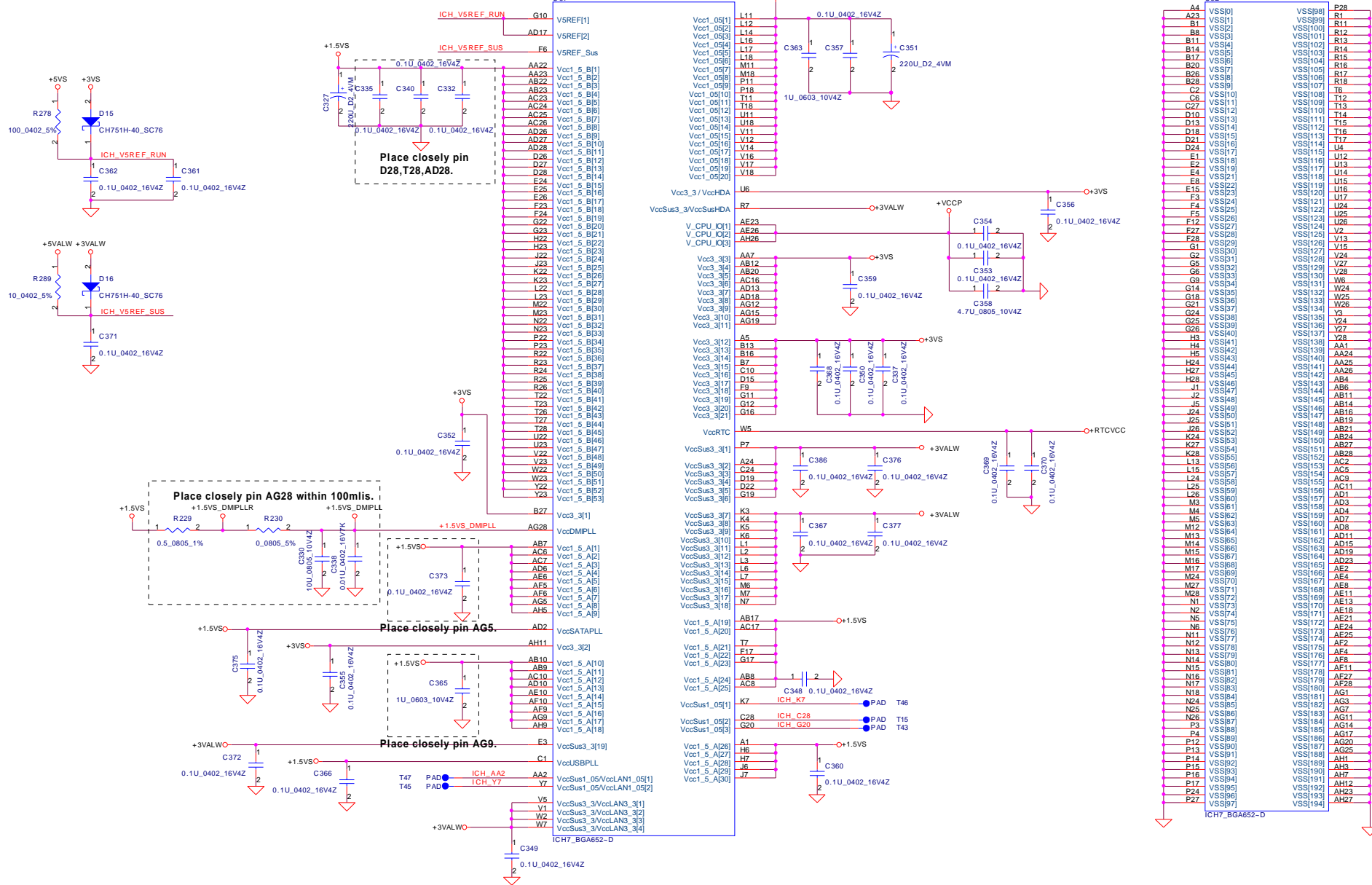


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ICH7-M(2/4)	
Title	Document Number
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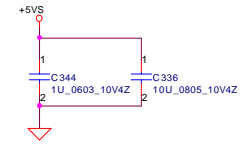
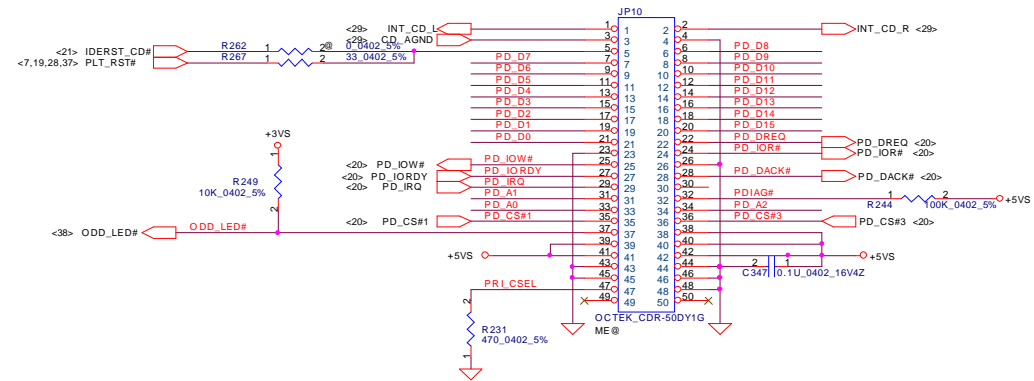
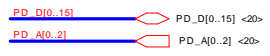
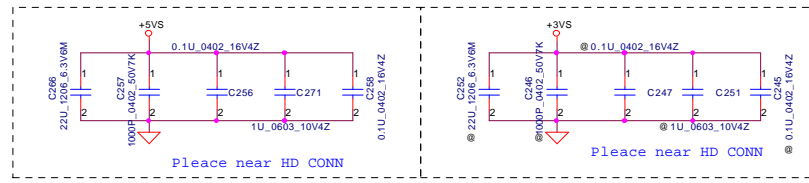
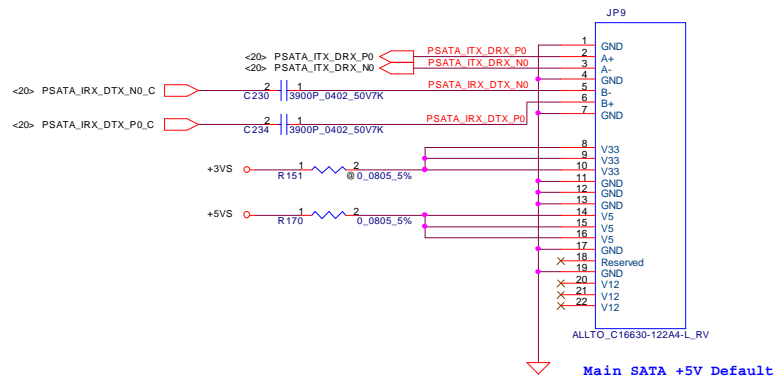


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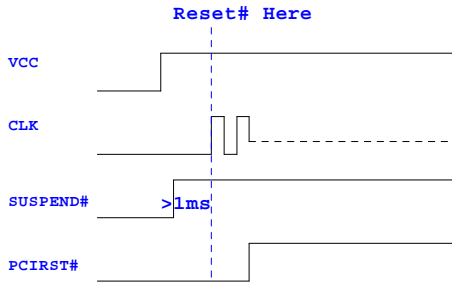
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Title	Document Number	Rev
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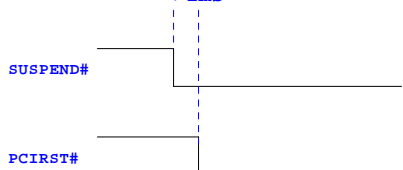


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Power on RESET#

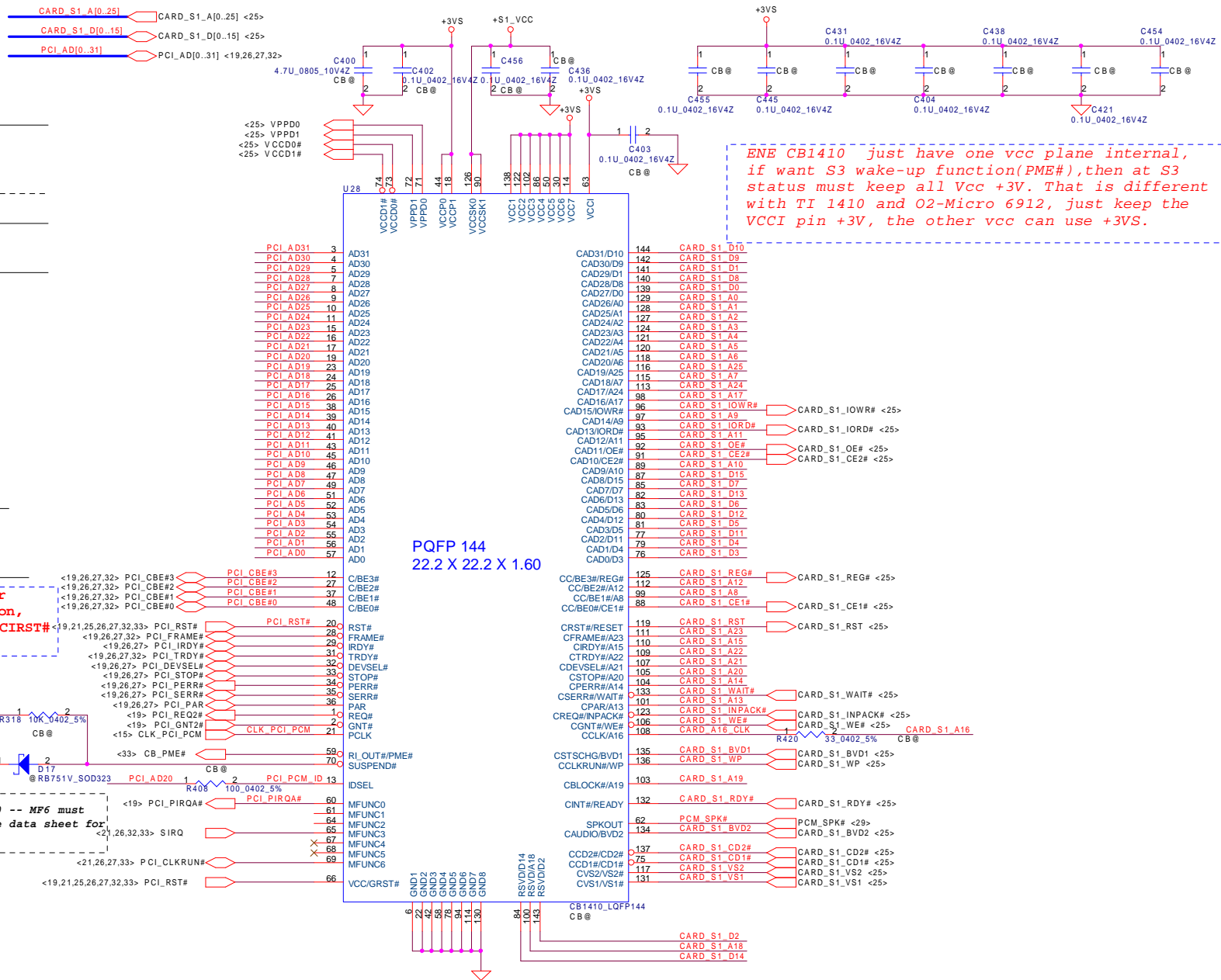


Entry S3



SUSPEND# will gate the PCIRST# or GRST#, so need S3 wake-up function, SUSPEND# must be LOW ahead the PCIRST# about 1ms.

Note: MF0 -- MF6 must refer the data sheet for design.



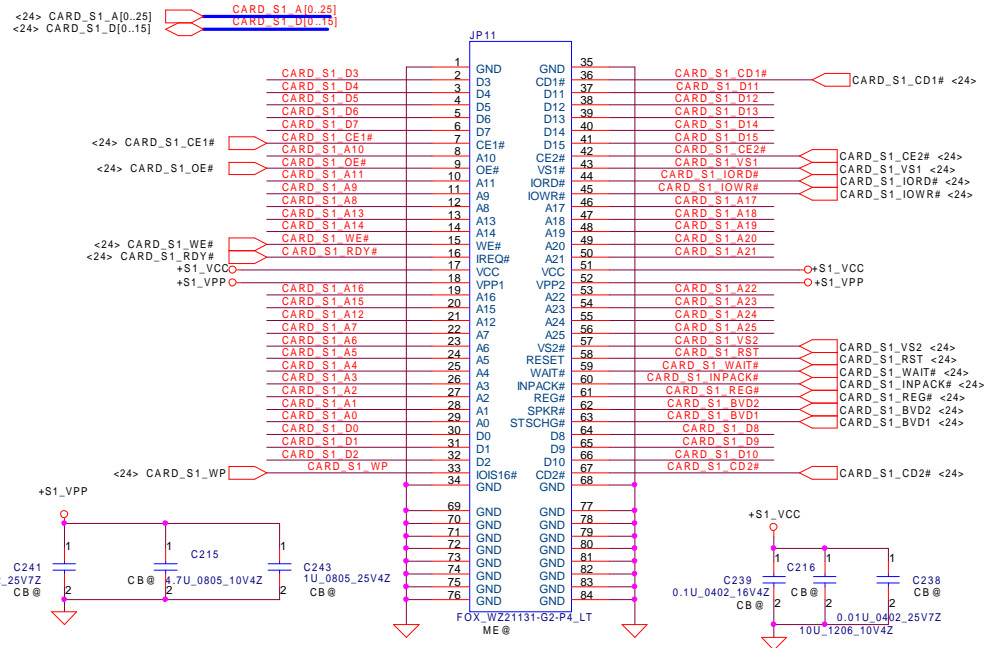
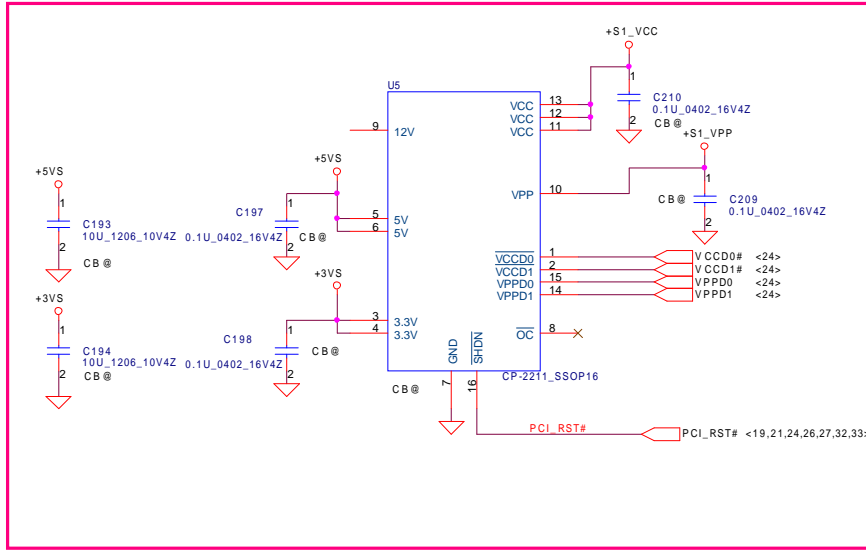
ENE CBI410 just have one vcc plane internal, if want S3 wake-up function(PM#), then at S3 status must keep all Vcc +3V. That is different with TI 1410 and O2-Micro 6912, just keep the VCCI pin +3V, the other vcc can use +3VS.

PQFP 144
22.2 X 22.2 X 1.60

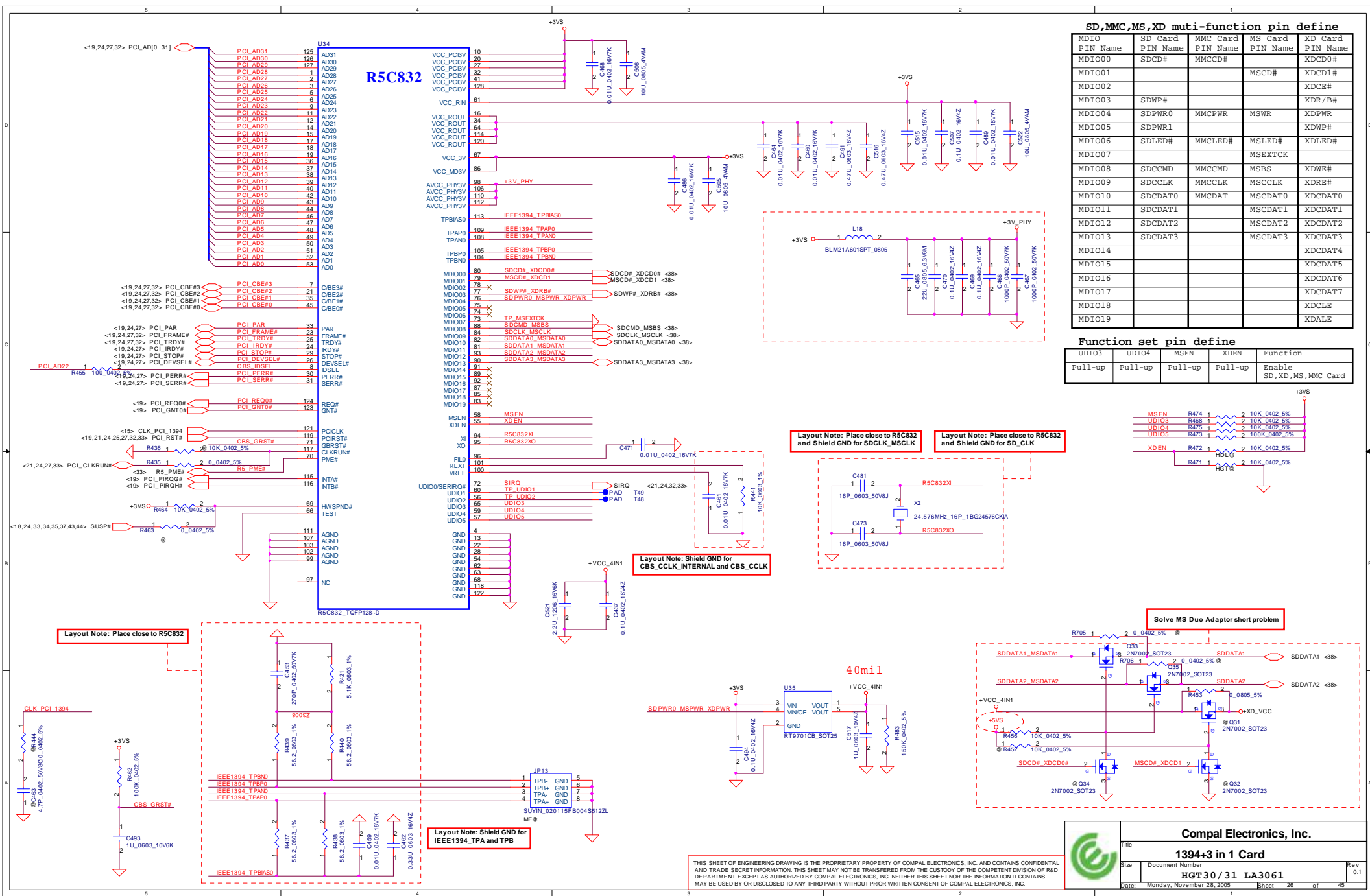
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CB ENE1410(One Solt)		
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PCMCIA Power Controller



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SD,MMC,MS,XD muti-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCB#
MDIO03	SDWP#			XDR/B#
MDIO04	SDPWR0	MMCPWR	MSWR	XDPWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLEB#	MSLED#	XDLED#
MDIO07			MSEXTC#	
MDIO08	SDCCMD	MMCCMD	MSB#	XDWE#
MDIO09	SDCLK	MMCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1		MSCDAT1	XDCDAT1
MDIO12	SDCDAT2		MSCDAT2	XDCDAT2
MDIO13	SDCDAT3		MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLE
MDIO19				XDALE

Function set pin define

UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD, XD, MS, MMC Card

Layout Note: Place close to R5C832 and Shield GND for SDCLK_MSLCK

Layout Note: Place close to R5C832 and Shield GND for SD_CLK

Layout Note: Shield GND for CBS_CCLK_INTERNAL and CBS_CCLK

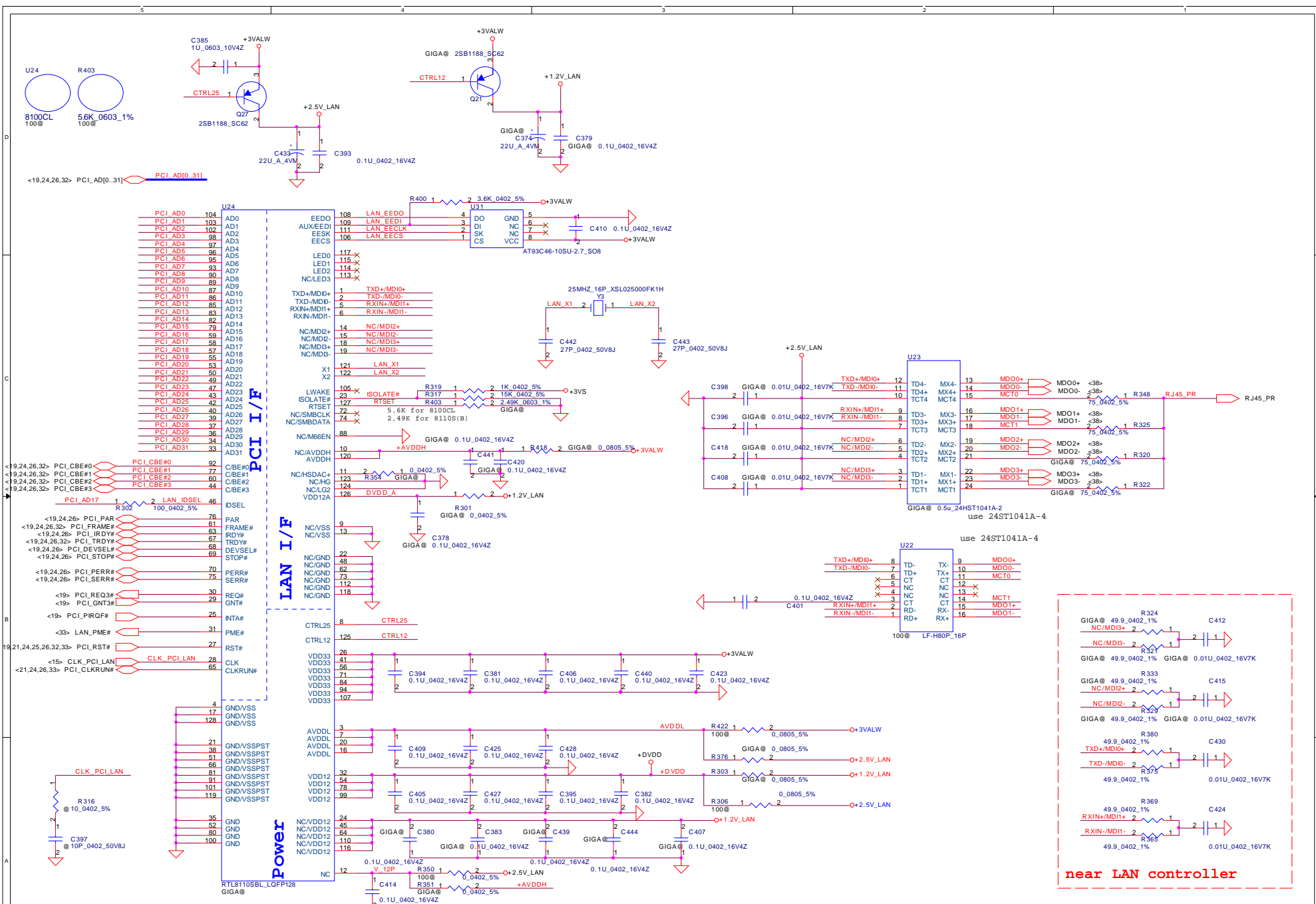
Solve MS Duo Adaptor short problem

40mil

Layout Note: Shield GND for IEEE1394_TPA and TPB

Compal Electronics, Inc.
1394+3 in 1 Card
 Title: 1394+3 in 1 Card
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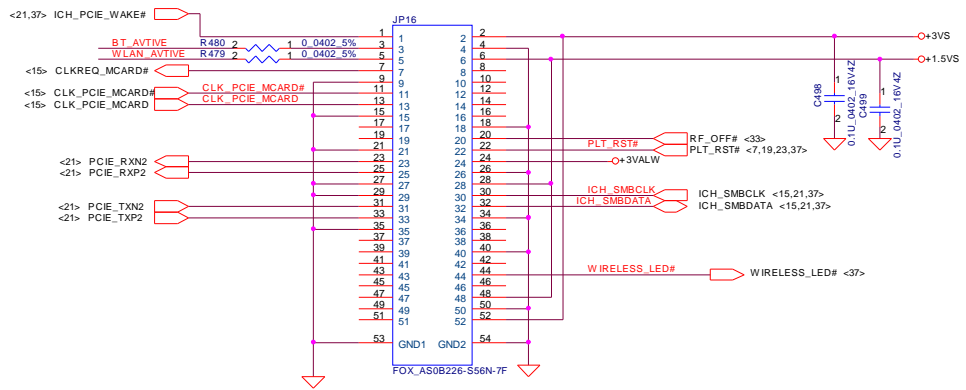
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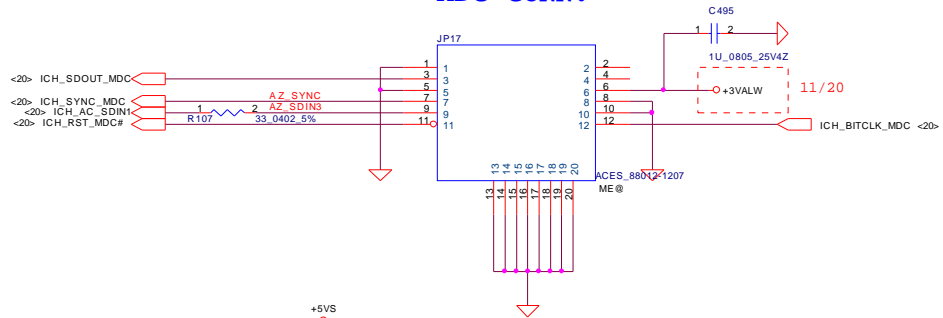
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LAN CONTROLLER		
Title	Document Number	Rev
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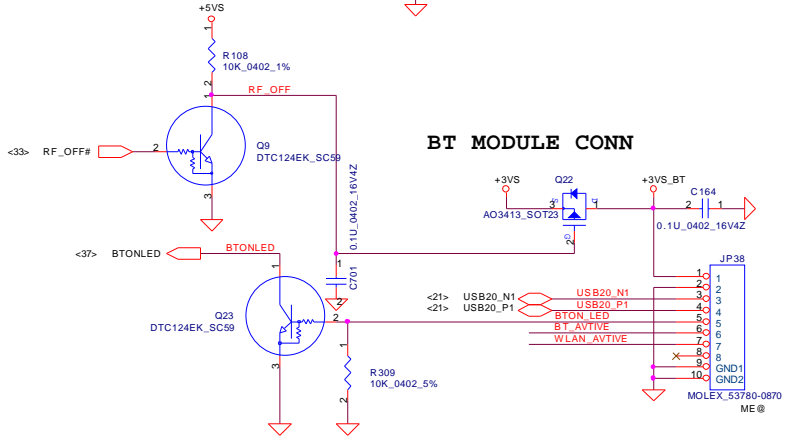
Mini-Express Card(Slot 1-WLAN)



MDC CONN.



BT MODULE CONN

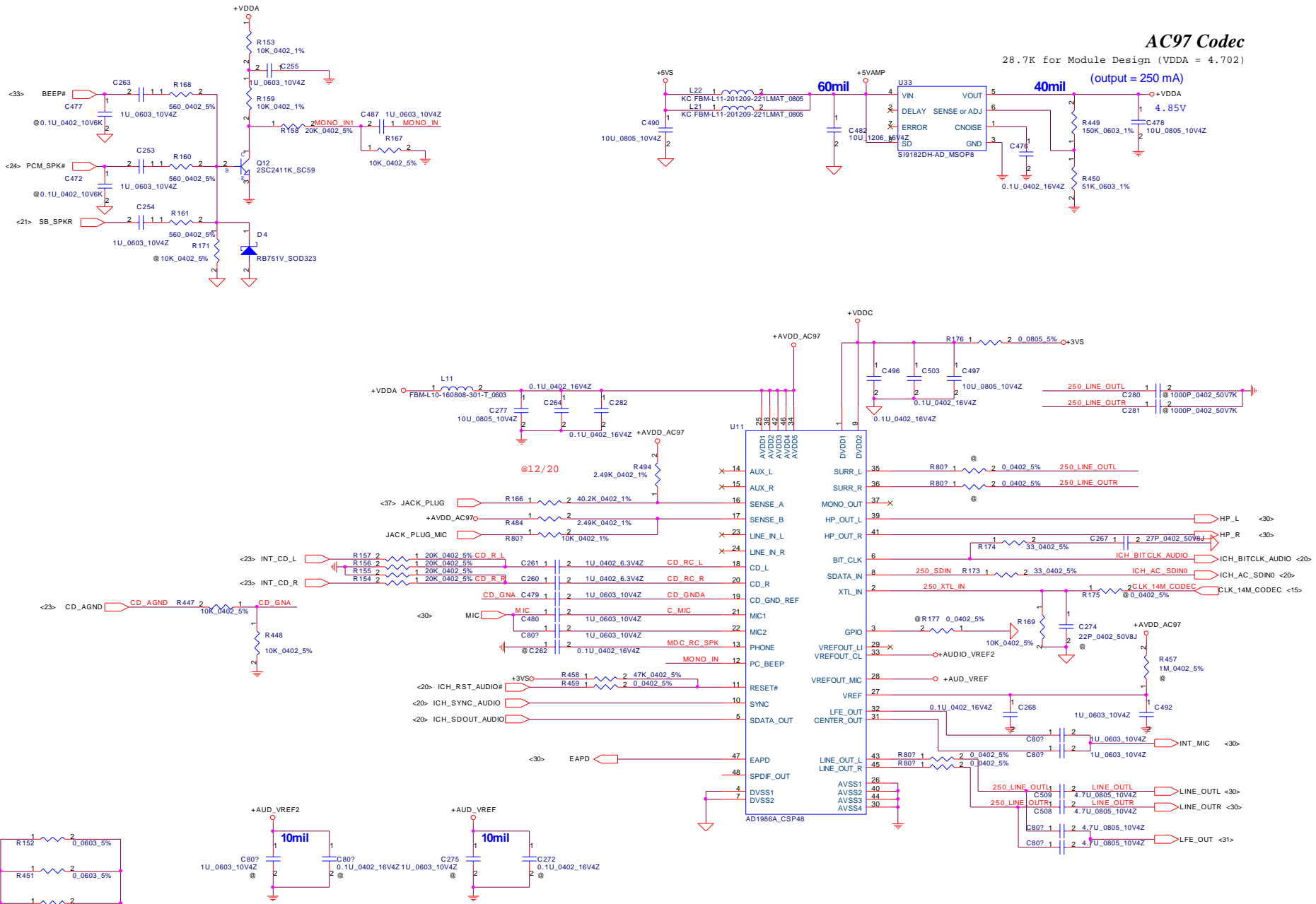


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Size	Document Number	Rev
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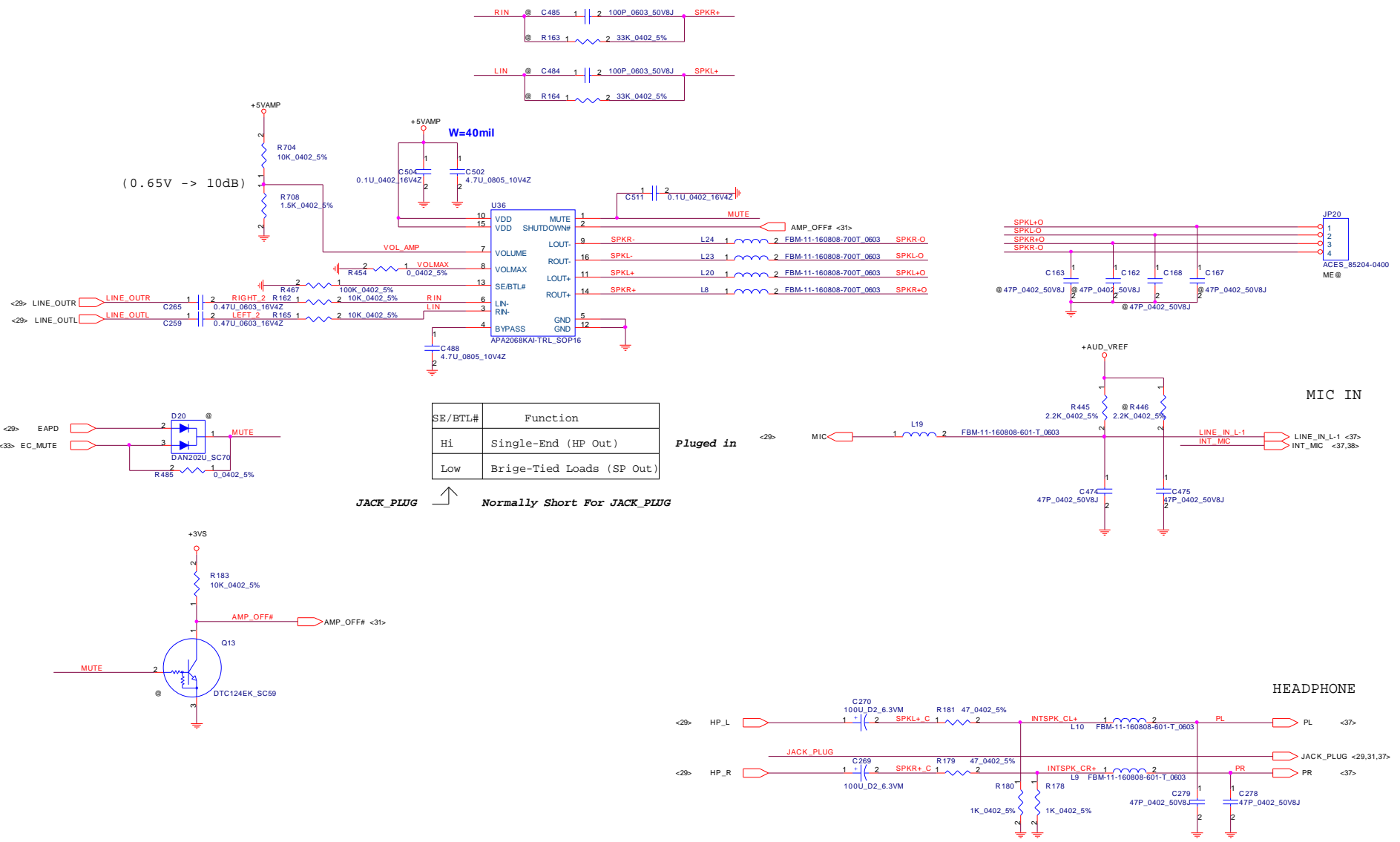
AC97 Codec

28.7K for Module Design (VDDA = 4.702)



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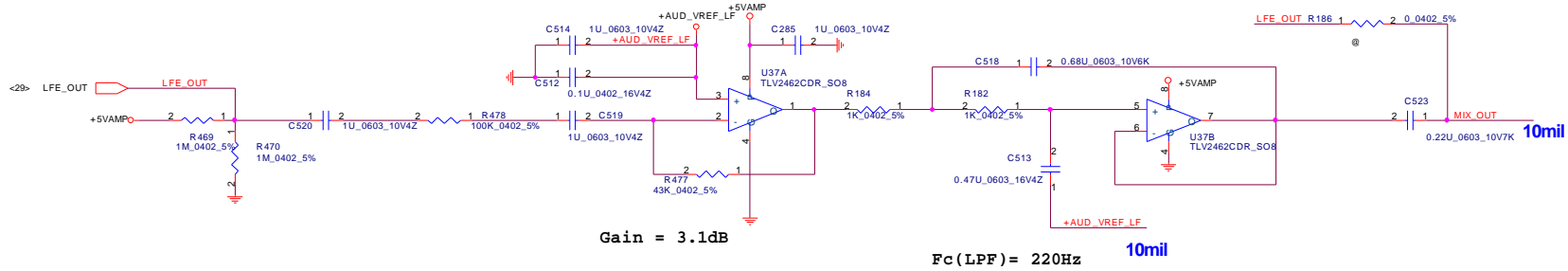
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AD1986 Codec		
Size	Document Number	Rev
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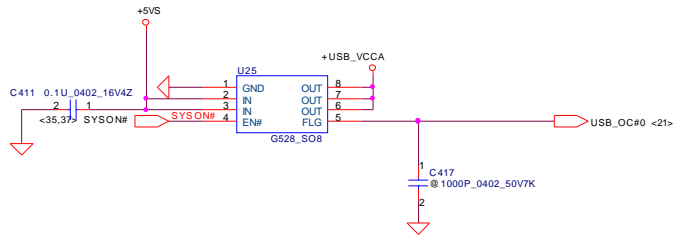
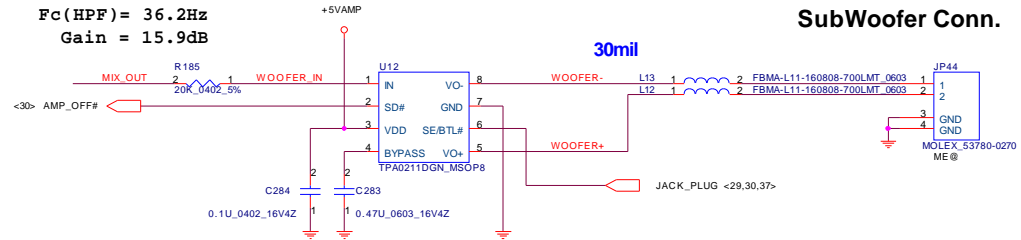
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SUBWOOFER (Reserved for C38)

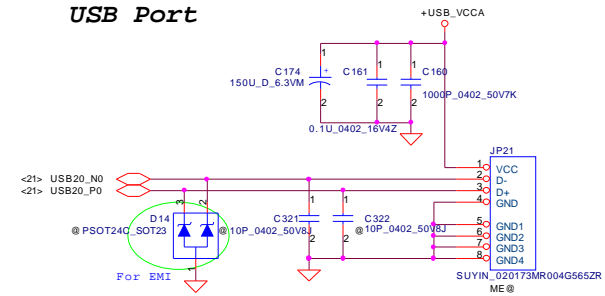
WOOFER@



Fc (HPF) = 36.2Hz
Gain = 15.9dB

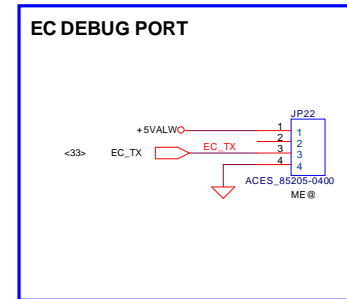
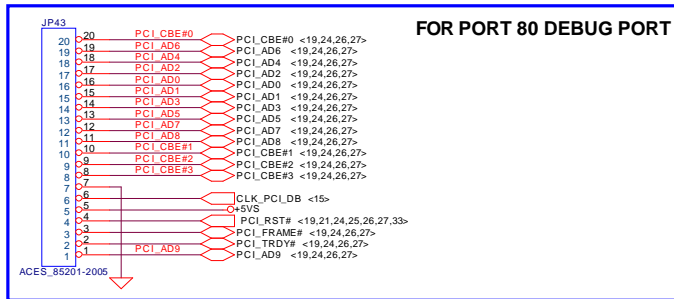
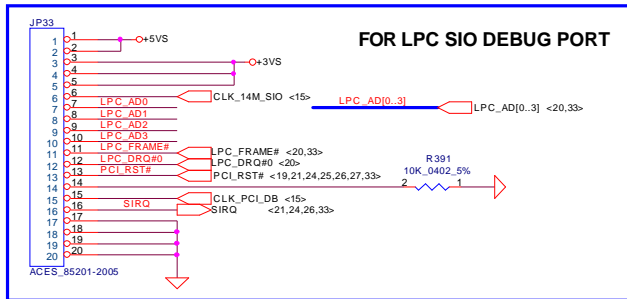
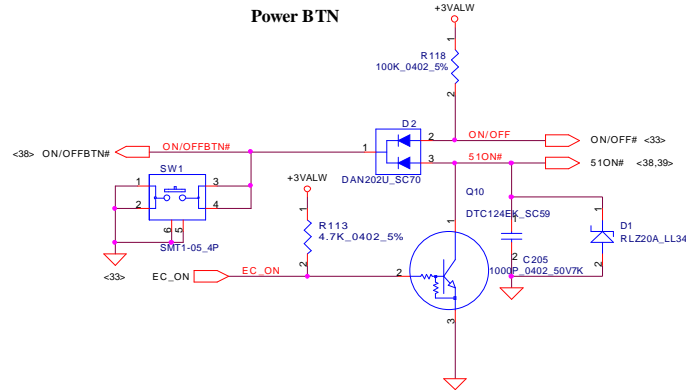
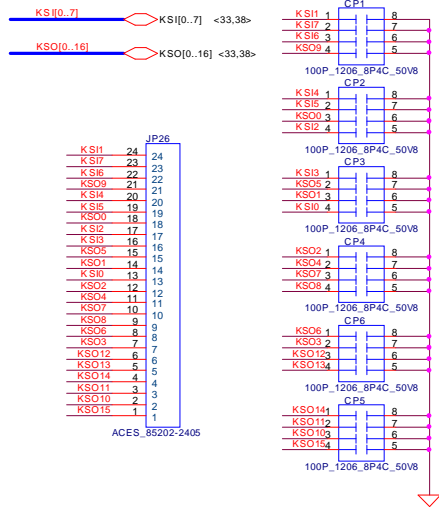


USB Port

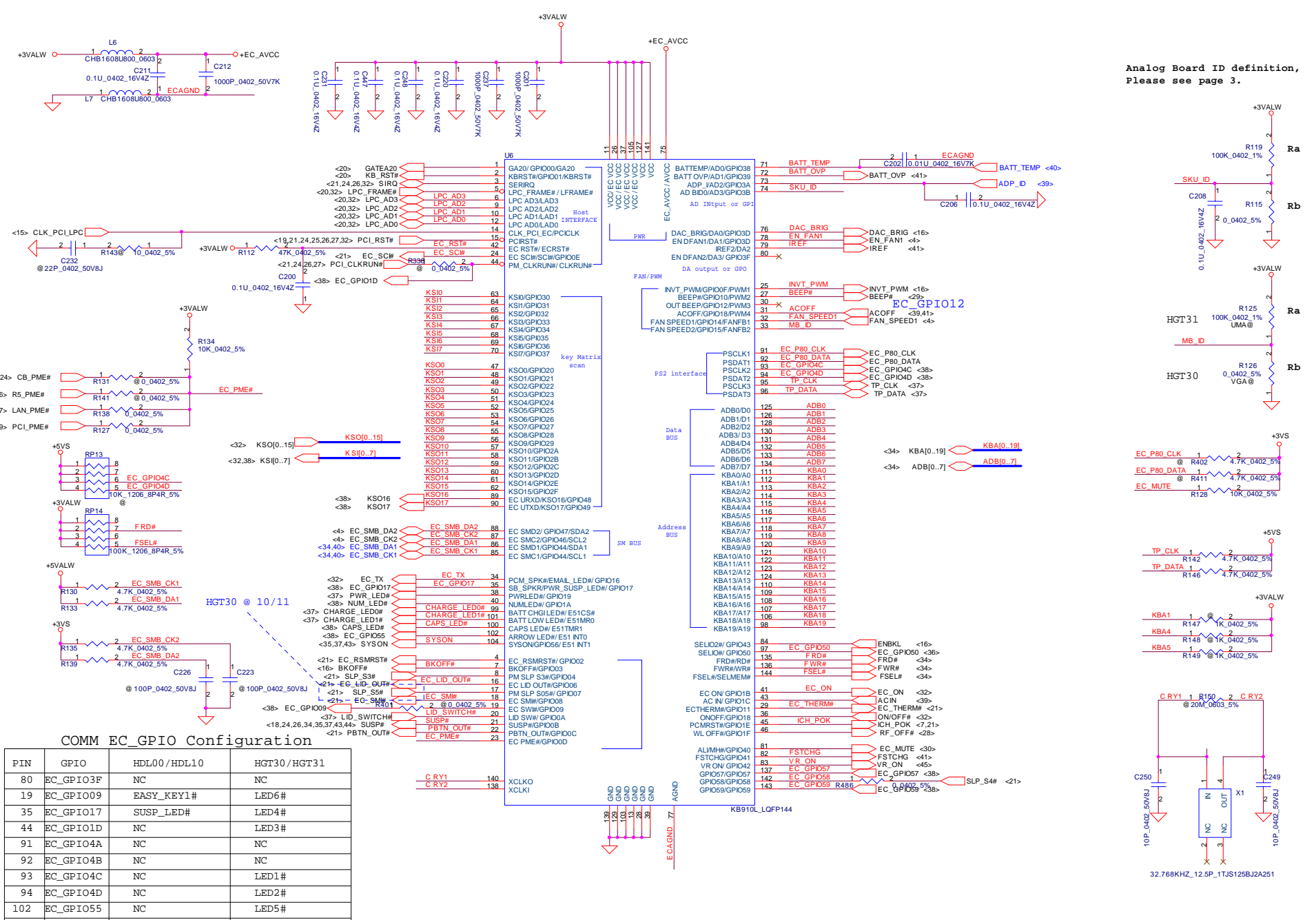


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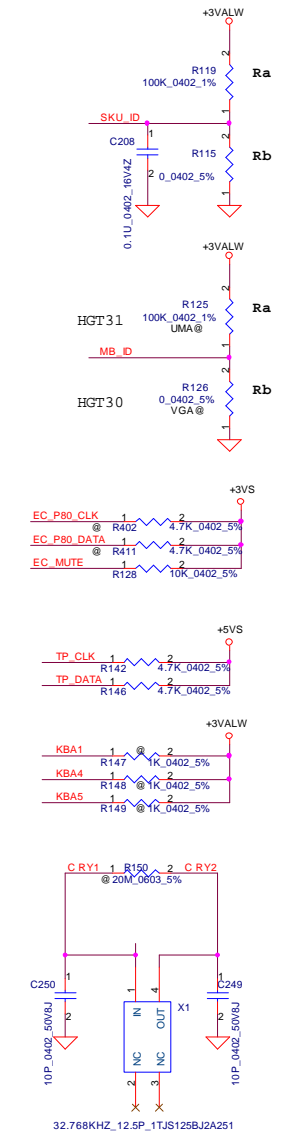
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Analog Board ID definition, Please see page 3.

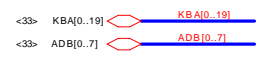
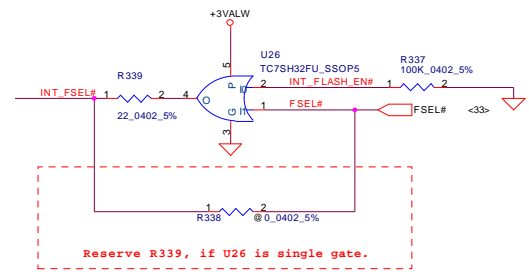
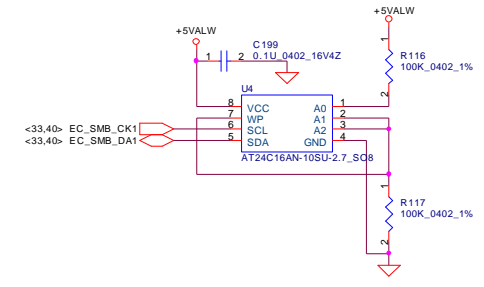
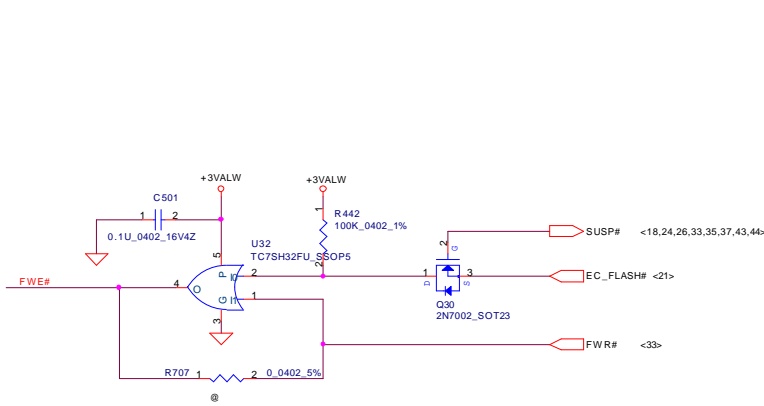


COMM EC_GPIO Configuration

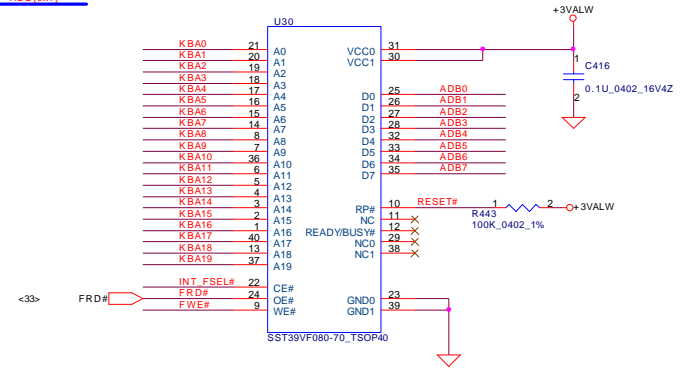
PIN	GPIO	HDL00/HDL10	HGT30/HGT31
80	EC_GPIO3F	NC	NC
19	EC_GPIO09	EASY_KEY1#	LED6#
35	EC_GPIO17	SUSP_LED#	LED4#
44	EC_GPIO1D	NC	LED3#
91	EC_GPIO4A	NC	NC
92	EC_GPIO4B	NC	NC
93	EC_GPIO4C	NC	LED1#
94	EC_GPIO4D	NC	LED2#
102	EC_GPIO55	NC	LED5#
97	EC_GPIO50	MEDIA#	MSSENS#
137	EC_GPIO57	VOL_UP#	NOVO_BTN#
142	EC_GPIO58	VOL_DOWN#	SLP_S4#
143	EC_GPIO59	KILL_SW#	WIRE_LAN_BTN#
30	EC_GPIO12	AMP_MUTE	NC

Security Classification		Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date	2006/10/06

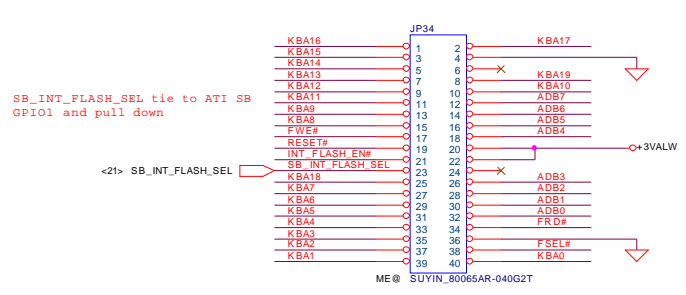
Compal Electronics, Inc.			
Title: ENE-KB910L			
Size	Document Number	Rev	
Cust#	HGT30/31 LA3061	0.1	
Date:	Mnday, November 28, 2006	Sheet	33 of 45



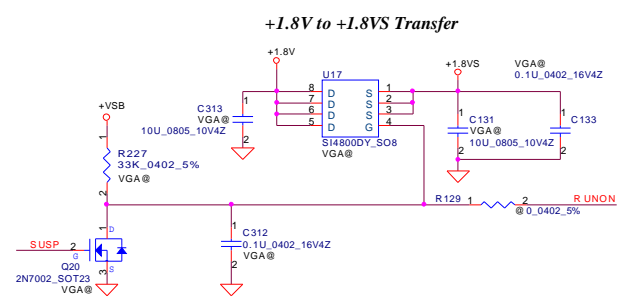
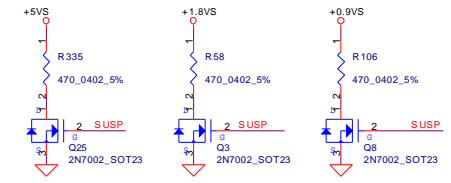
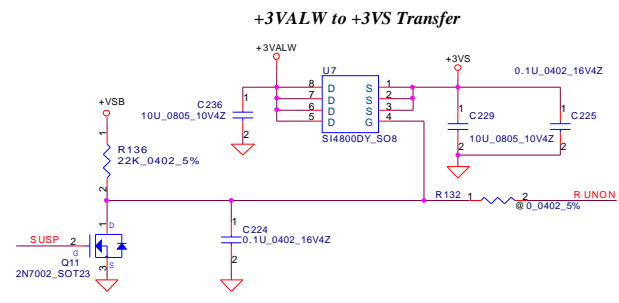
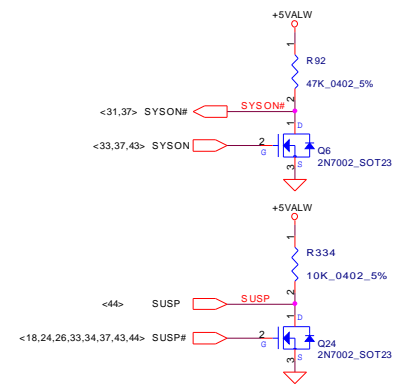
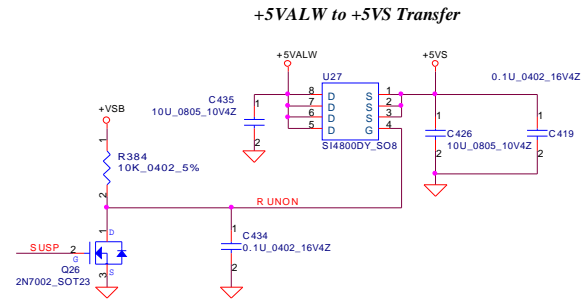
1MB Flash ROM



1MB ROM Socket



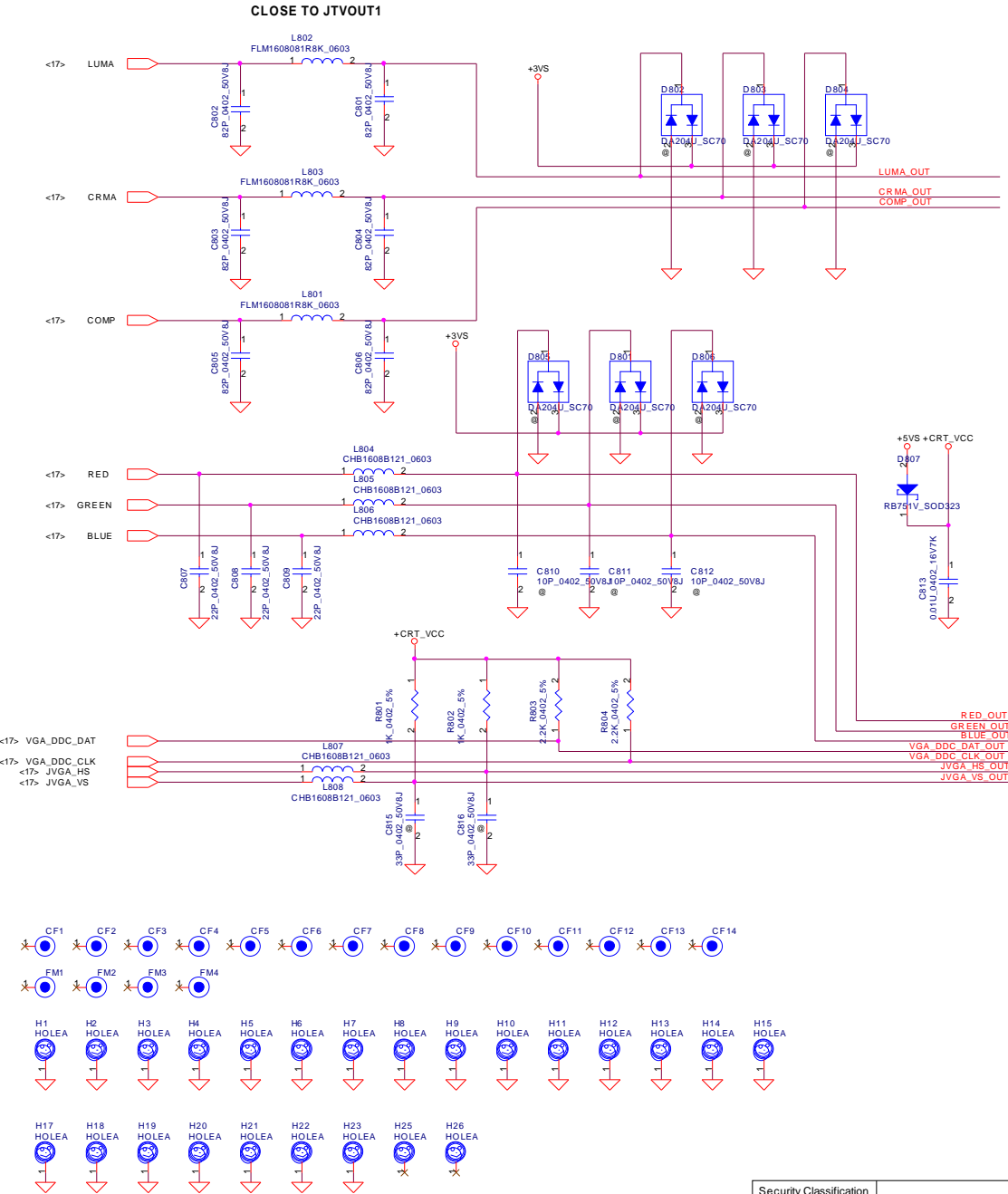
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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Compal Electronics, Inc.
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Date:	Monday, November 28, 2005	Sheet	34 of 45	



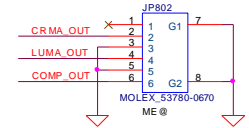
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Issued Date	2005/10/06	Deciphered Date
		2006/10/06
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Compal Electronics, Inc.		
Title	DC/DC Circuit	
Size	Document Number	Rev
Custody	HGT30/31 LA3061	0.1
Date:	Monday, November 28, 2005	Sheet 35 of 45

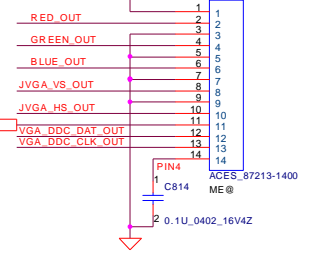
VGA I/O PORT Connector



S-VIDEO



DSUB



PIN ASSIGNMENT

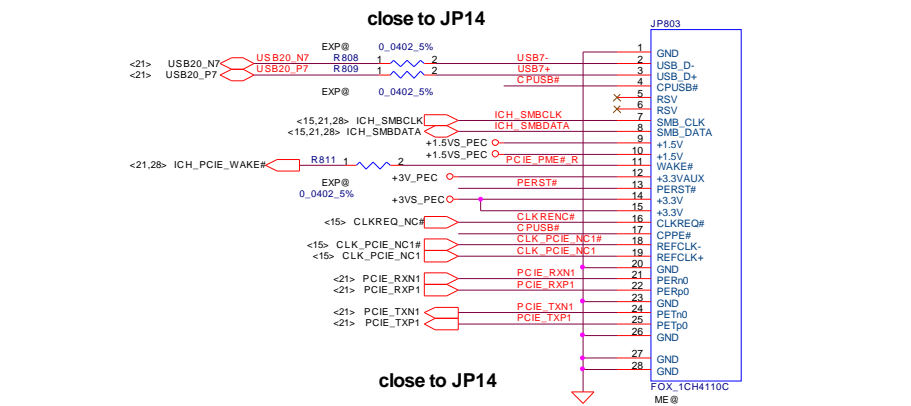
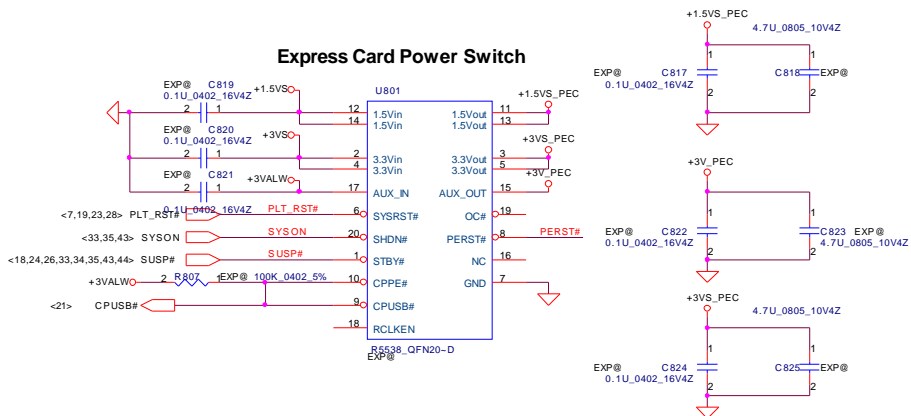
PIN	D-SUB	FUNCTION	PIN	SVIDEO	FUNCTION
1	9	+CRT_VCC	1	1	NC
2	1	RED	2	4	CRMA
3	6	GND	3	2	GND
4	2	GREEN	4	3	LUMA
5	7	GND	5	5	GND
6	3	BLUE	6	6	CVBS
7	8	GND			
8	14	VSYNC			
9	10	GND			
10	13	HSYNC			
11	11	SENSE			
12	12	SM_DAT			
13	15	SM_CLK			
14	4	PIN4			

Security Classification: Compal Secret Data
 Issued Date: 2005/03/10
 Deciphered Date: 2006/03/10

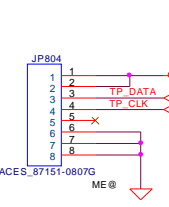
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Compal Electronics, Inc.
CRT & TVout Connector
 Size: Document Number
 Custom: HGT30/31 LA3061
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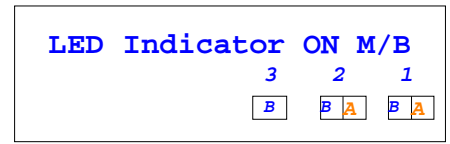
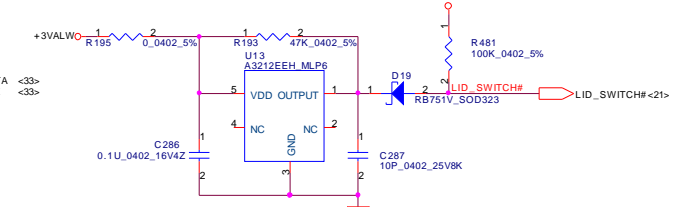
NEW CARD FOR C38



T/P Board



LID Switch

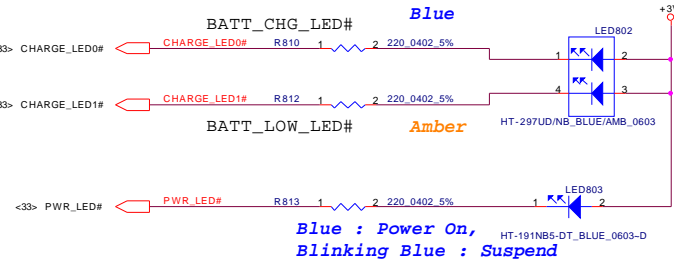


STATUS	
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

(1)

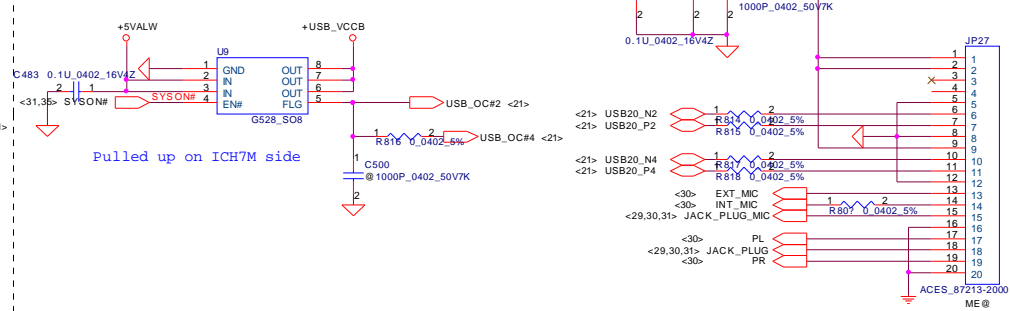
(2)

(3)



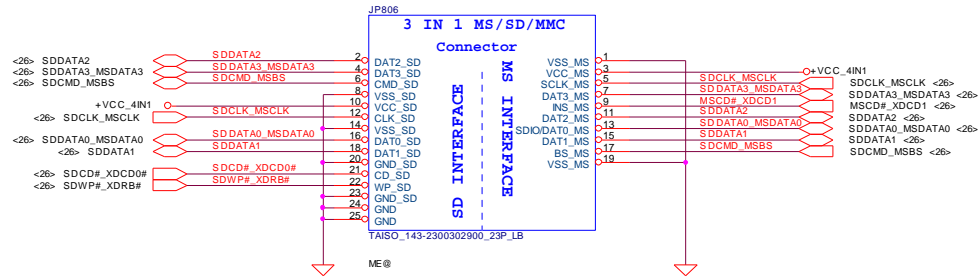
Blue : Power On,
Blinking Blue : Suspend

USB board

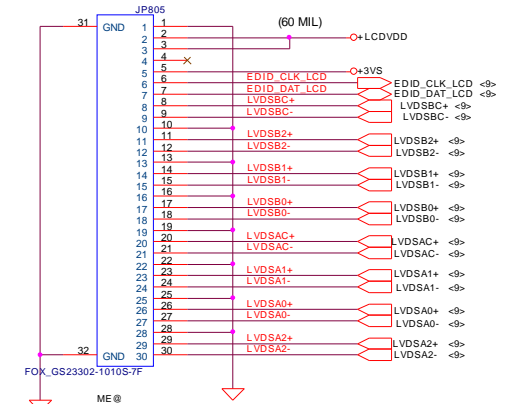


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Size	Document Number			Rev
Customer	HGT30/31 LA3061			0.1
Date	Monday, November 28, 2005	Sheet	37	of 45

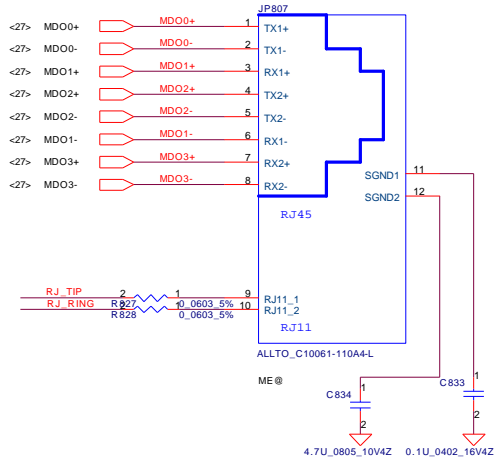
3 IN 1 Card Reader



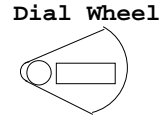
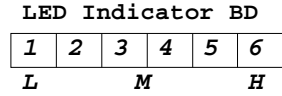
UMA LCD/PANEL Conn.



RJ11+RJ45 CONN

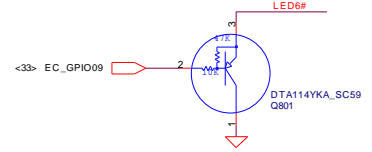


SWITCH BD

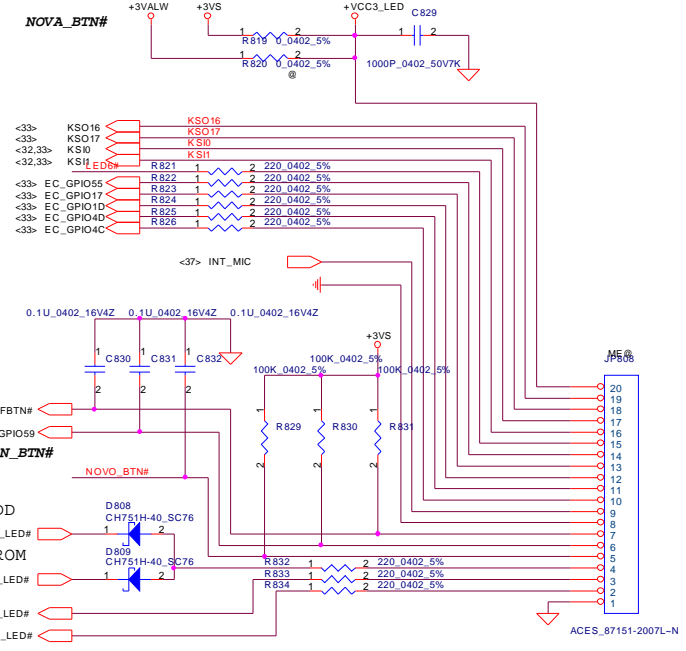
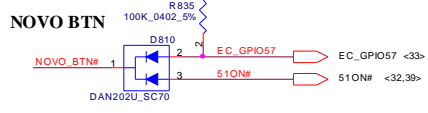
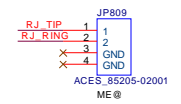


Function

KEY Matrix	K016	K017
KS10	DW-UP	DW-DOWN
KS11	DW-ENTER	MUTE

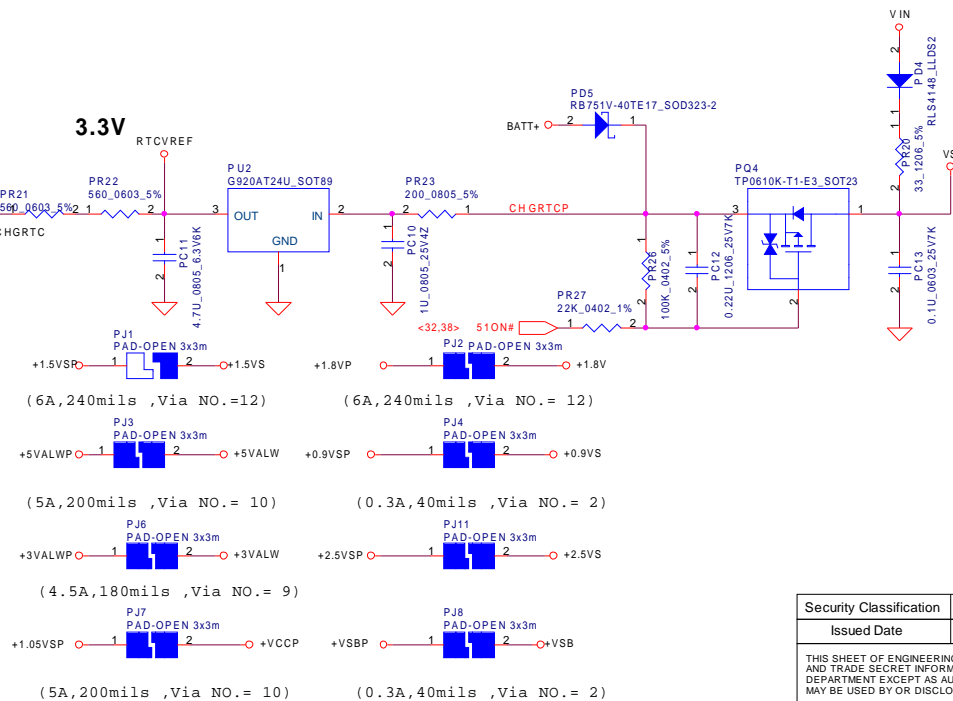
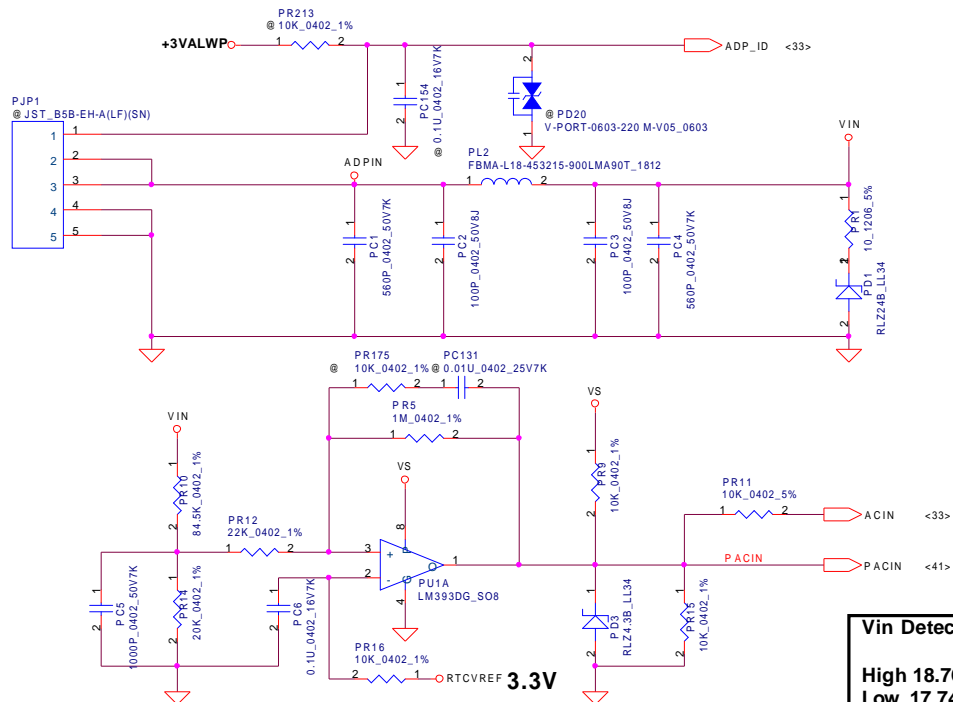


MDC CONN



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Compal Electronics, Inc.		
Title	INDICATE LED	
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ACIN

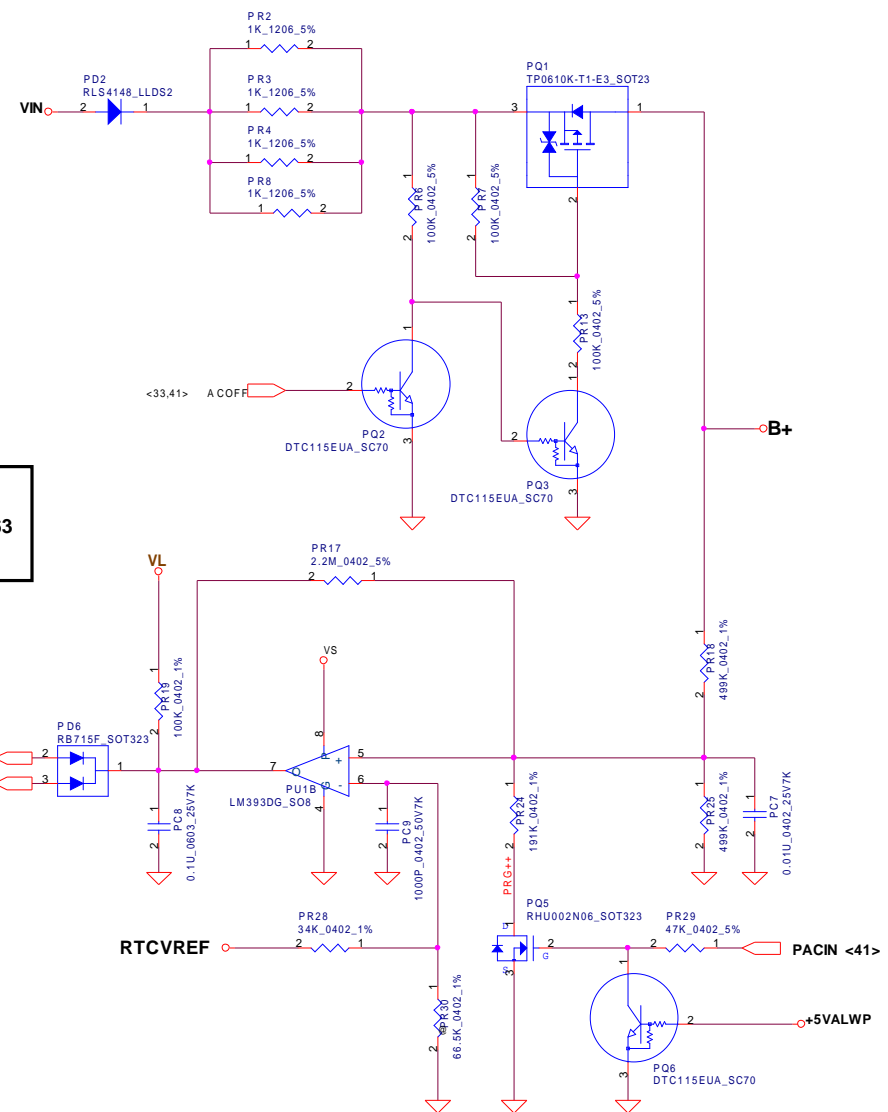
Precharge detector

	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

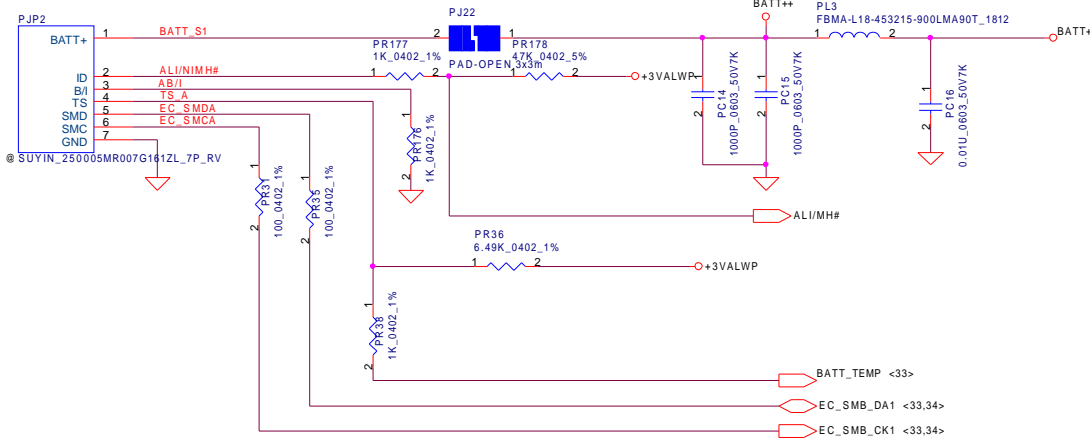
Precharge detector

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

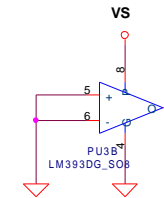
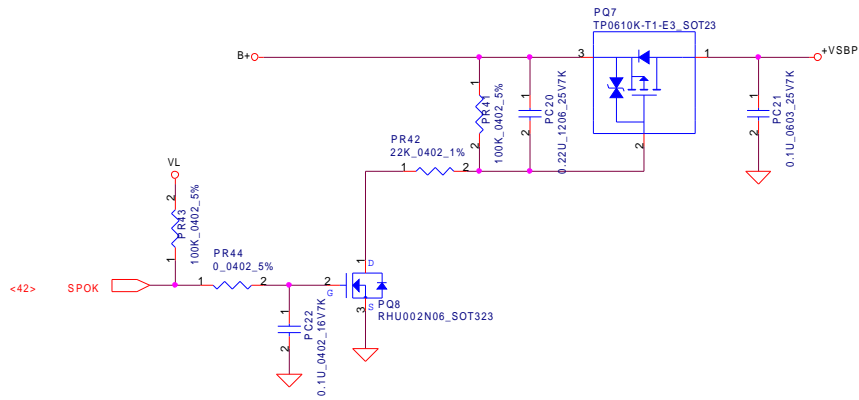
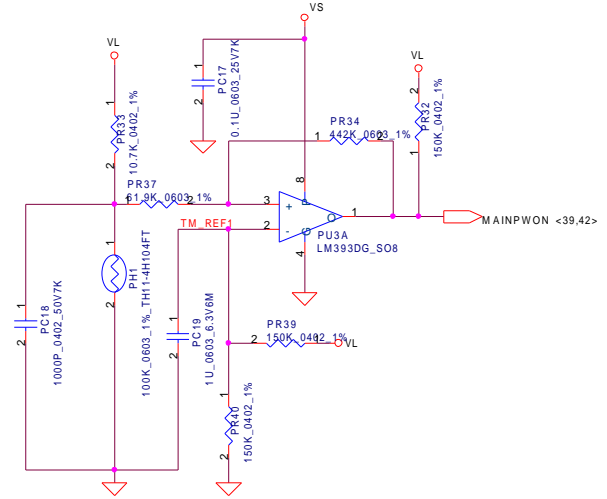


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		2006/08/01
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Compal Electronics, Inc.		
DCIN/DECTOR		
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PH1 under CPU bottom side :
 CPU thermal protection at 85 degree C
 Recovery at 70 degree C

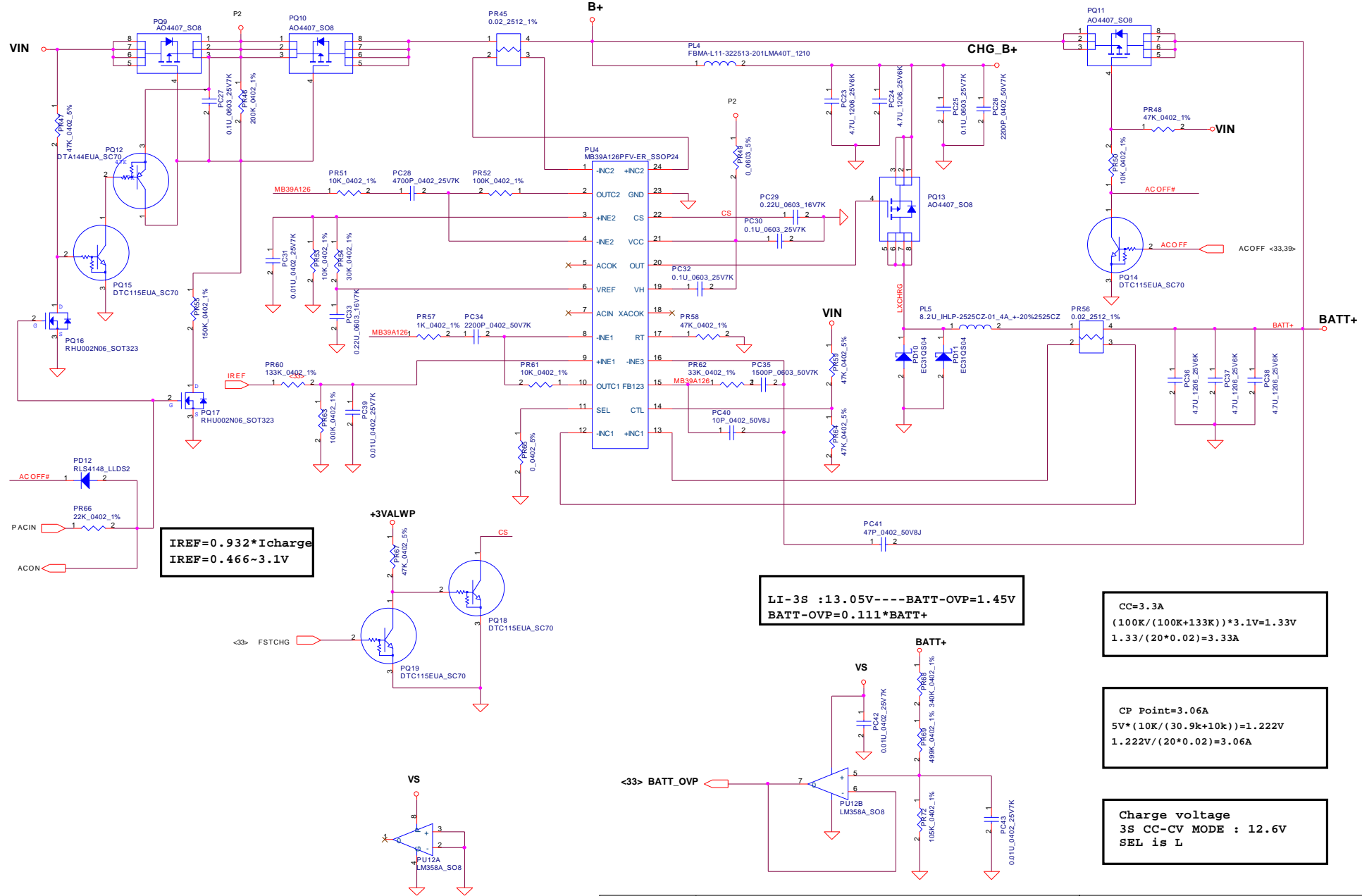


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65W PR45=0.02_2512_1% PR54=30K_0402_1% Iadp=0~3.125A
 90W PR45=0.15_2512_1% PR54=28.7K_0402_1% Iadp=0~4.3A

Fosc=14100/Rt=14100/47=300KHz

Charger



$I_{REF} = 0.932 * I_{charge}$
 $I_{REF} = 0.466 \sim 3.1V$

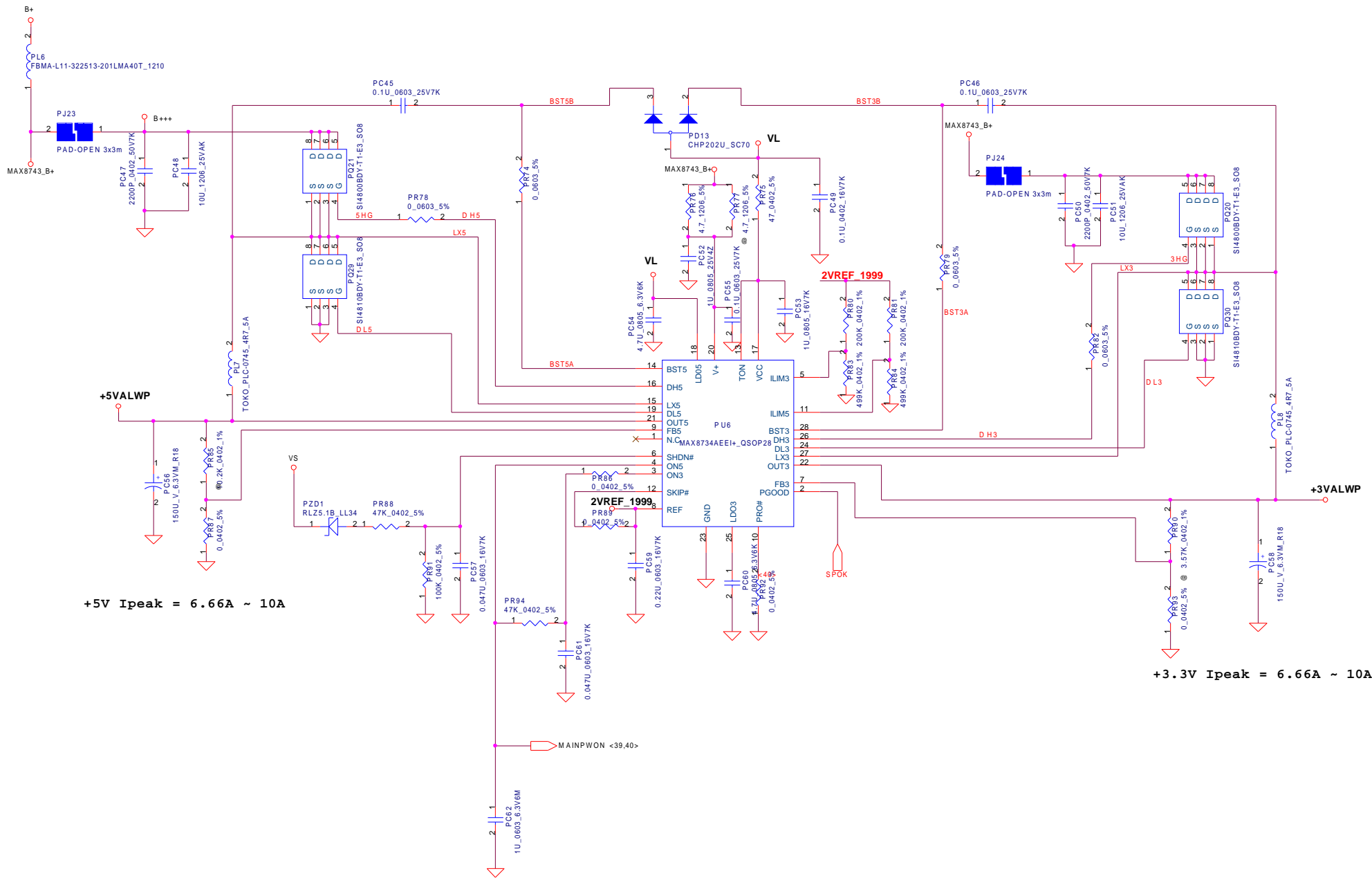
LI-3S : 13.05V --- BATT-OVP=1.45V
 BATT-OVP=0.111*BATT+

CC=3.3A
 $(100K / (100K + 133K)) * 3.1V = 1.33V$
 $1.33V / (20 * 0.02) = 3.33A$

CP Point=3.06A
 $5V * (10K / (30.9K + 10K)) = 1.222V$
 $1.222V / (20 * 0.02) = 3.06A$

Charge voltage
 3S CC-CV MODE : 12.6V
 SEL is L

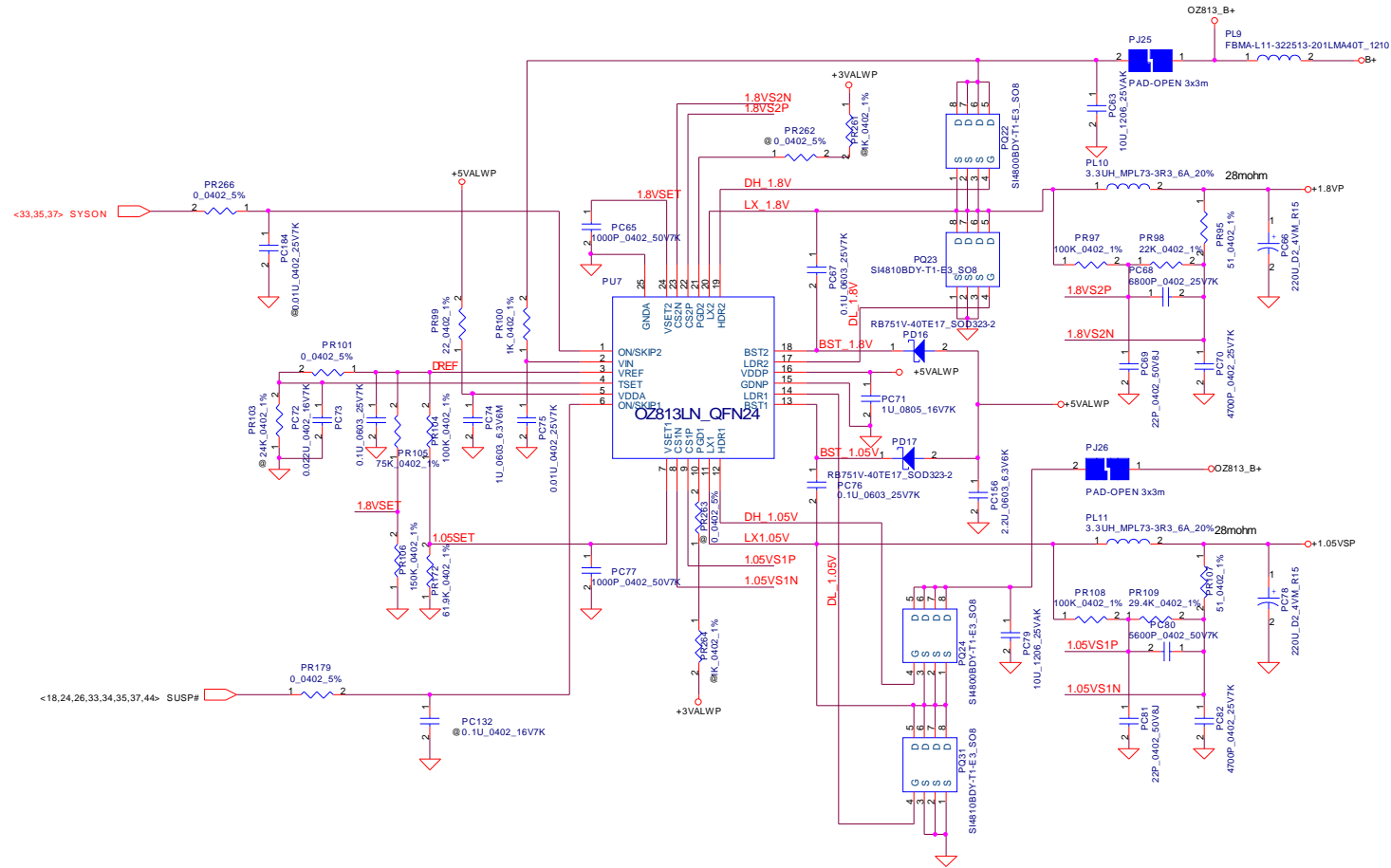
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	B	Document Number		Rev	0.1
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				Custom	Rev
				0.1	
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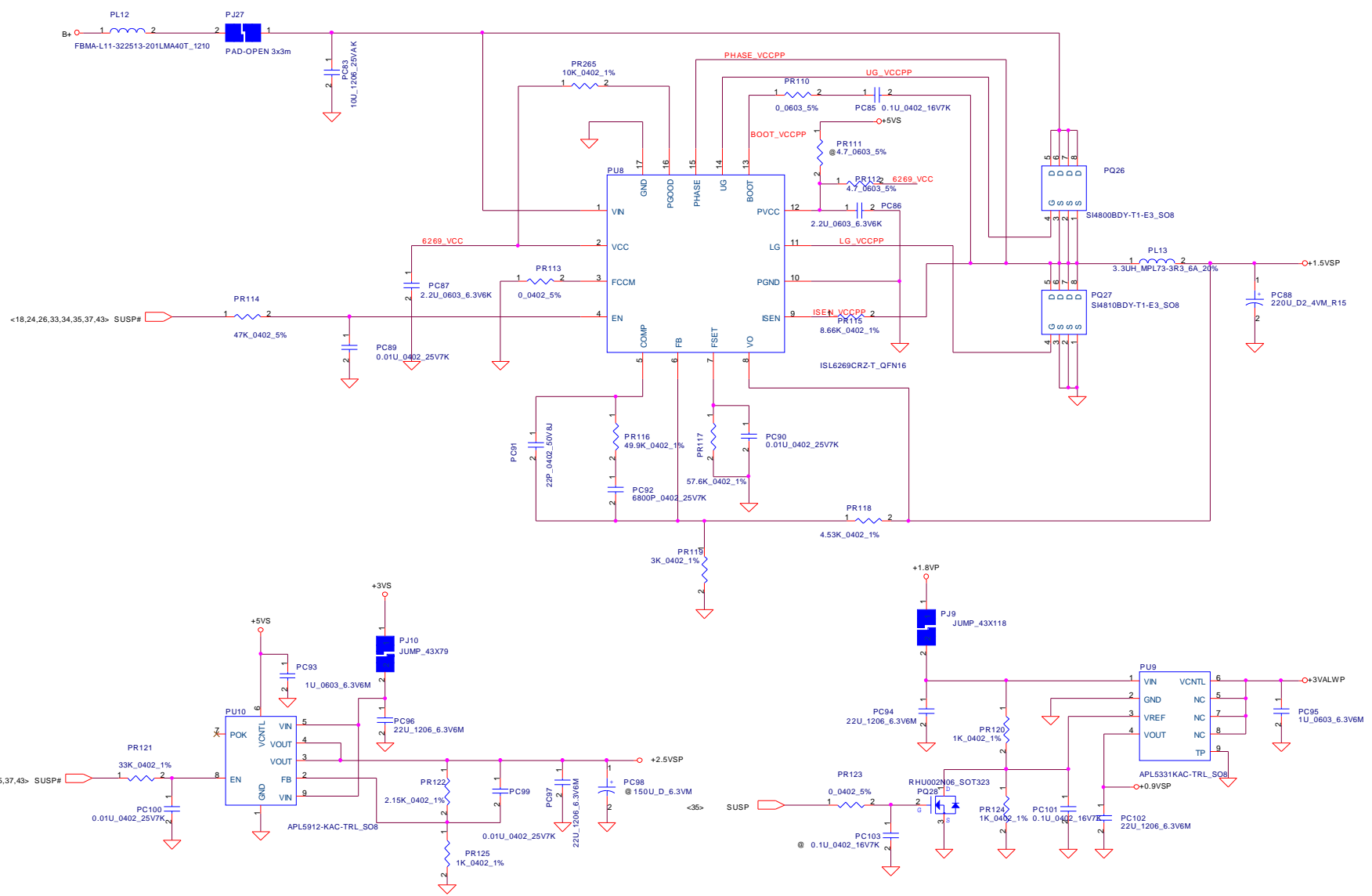
+1.8VP Ilimit = 10A

+1.05VSP Ilimit=8A

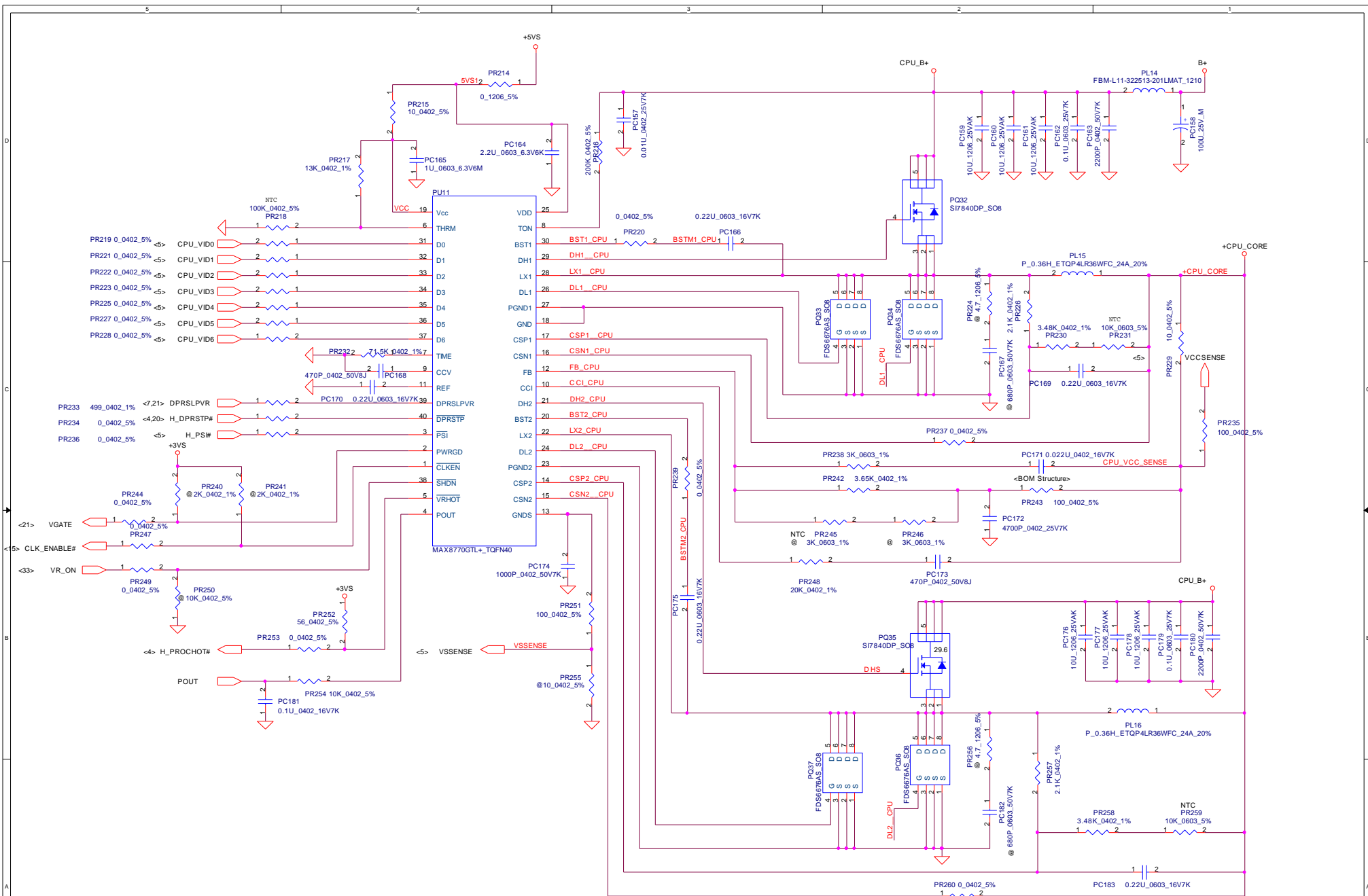


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Issued Date	2005/08/01	Deciphered Date	2006/08/01	Title	1.05VP/1.8VP
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+1.5VSP Ilimit = 9.38A-12.5A



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Custom				
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