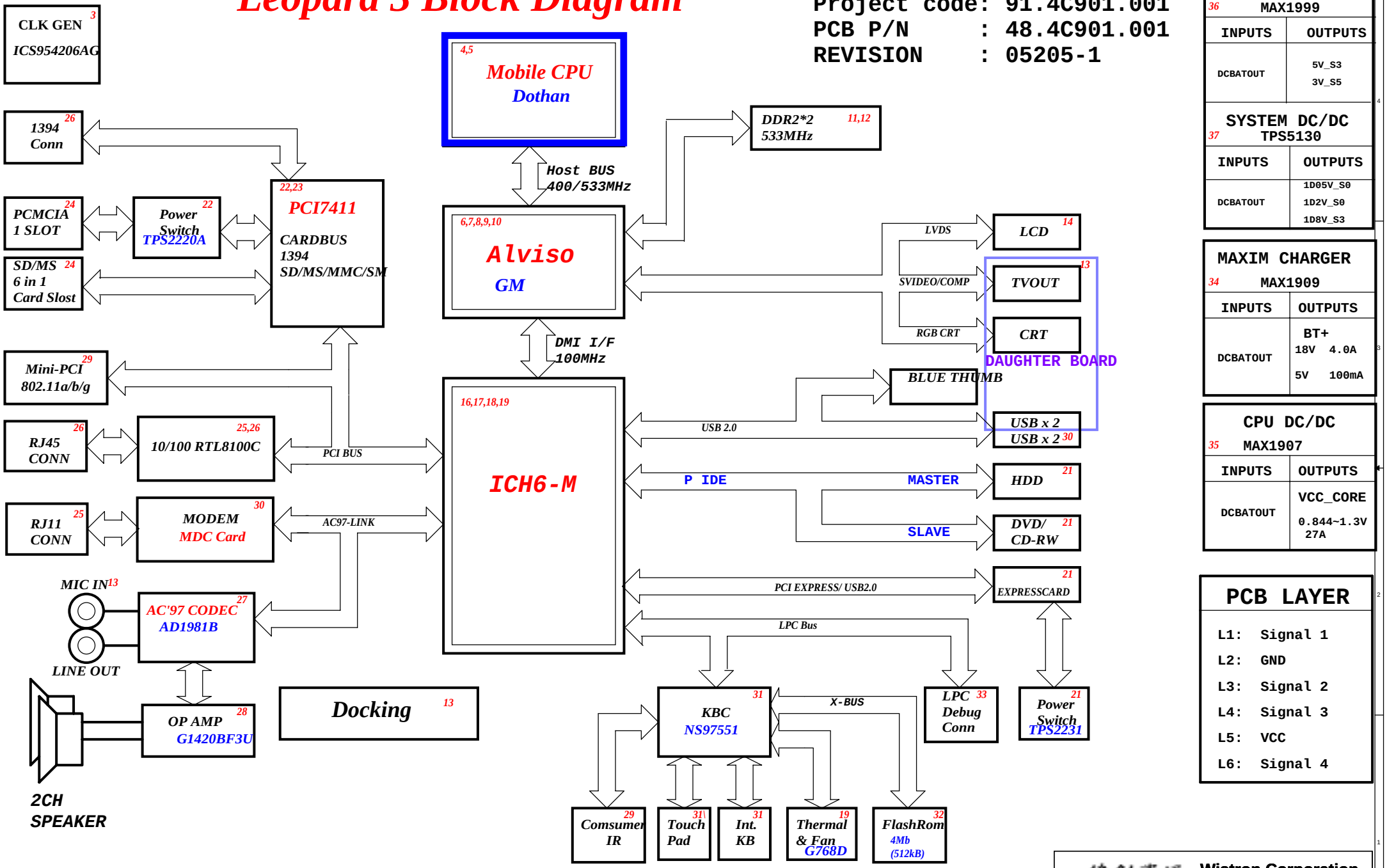
Leopard 3 Block Diagram

Project code: 91.4C901.001
PCB P/N : 48.4C901.001
REVISION : 05205-1



SYSTEM DC/DC MAX1999 (36)	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC TPS5130 (37)	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 1D8V_S3

MAXIM CHARGER MAX1909 (34)	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC MAX1907 (35)	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

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ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_1D8V= 1.8 Voltage power up on system work(S0 state)
1D8V_S3= 1.8Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 0.9 Voltage suspend to RAM(S3 state)
0D9V_S0= 1.25 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0#/GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1#/GNT1#
LAN	AD23	P_INTE#	REQ2#/GNT2#
Blue Thumb	AD24		

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Title: *ITP*

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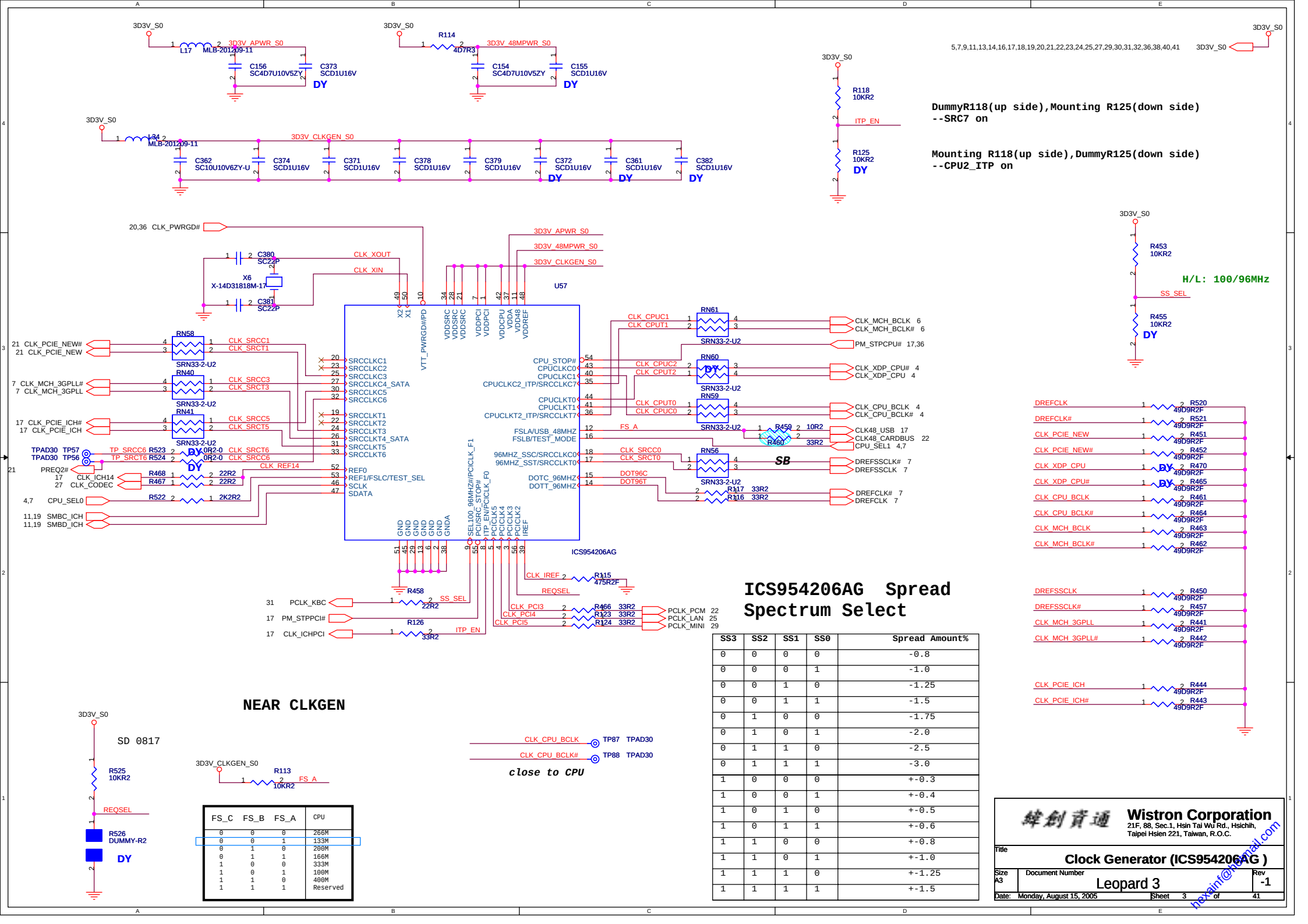
3D3V_S0
L17 MLB-201209-11
3D3V_APWR_S0
C156 SC4D7U10V5ZY
C373 SCD1U16V
DY
R114 4D7R3
3D3V_48MPWR_S0
C154 SC4D7U10V5ZY
C155 SCD1U16V
L34 MLB-201209-11
3D3V_CLKGEN_S0
C362 SC10U10V6ZY-U
C374 SCD1U16V
C371 SCD1U16V
C378 SCD1U16V
C379 SCD1U16V
C372 SCD1U16V
C361 SCD1U16V
C382 SCD1U16V
R118 10KR2
ITP_EN
R125 10KR2
DummyR118(up side),Mounting R125(down side)
--SRC7 on
Mounting R118(up side),DummyR125(down side)
--CPU2_ITP on
5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41
20,36 CLK_PWRGD#
C380 SC22P
C381 SC22P
X6 X-14D31818M-17
CLK_XOUT
CLK_XIN
U57
VTT_PWRGD#/PD
RN58
RN40
RN41
SRN33-2-U2
CLK_SRCC1
CLK_SRCT1
CLK_SRCC3
CLK_SRCT3
CLK_SRCC5
CLK_SRCT5
CLK_SRCC6
CLK_SRCT6
SRCCLKC1
SRCCLKC2
SRCCLKC3
SRCCLKC4_SATA
SRCCLKC5
SRCCLKC6
SRCCLKT1
SRCCLKT2
SRCCLKT3
SRCCLKT4_SATA
SRCCLKT5
SRCCLKT6
CLK_REF14
REF0
REF1/FSLC/TEST_SEL
SCLK
SDATA
TPAD30 TP57
TPAD30 TP56
TP_SRCC6 R523 0R2-0
TP_SRCT6 R524 0R2-0
PREQ2#
CLK_ICH14
CLK_CODEC
R468 22R2
R467 22R2
R522 2K2R2
CPU_SEL0
SMBC_ICH
SMBD_ICH
CPU_STOP#
CPUCLKC0
CPUCLKC1
CPUCLKC2_ITP/SRCCLKC7
CPUCLKT0
CPUCLKT1
CPUCLKT2_ITP/SRCCLKT7
FSLA/USB_48MHZ
FSLB/TEST_MODE
96MHZ_SSC/SRCCLKC0
96MHZ_SST/SRCCLKT0
DOTC_96MHZ
DOTT_96MHZ
FS_A
CLK_SRCC0
CLK_SRCT0
DOT96C
DOT96T
RN61
RN60
RN59
RN56
CLK_CPUC1
CLK_CPUT1
CLK_CPUC2
CLK_CPUT2
CLK_CPUT0
CLK_CPUC0
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
PM_STPCPU# 17,36
CLK_XDP_CPU# 4
CLK_XDP_CPU 4
CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
R459 10R2
R460 33R2
CLK48_USB 17
CLK48_CARDBUS 22
CPU_SEL1 4,7
SB
DREFSSCLK# 7
DREFSSCLK 7
R117 33R2
R116 33R2
DREFCLK# 7
DREFCLK 7
GND GND GND GND GND GND GNDA
SEL100_96MHZ#/PCICLK_F1
PCI/SRC_STOP#
ITP_EN/PCICLK_F0
PCICLK5
PCICLK4
PCICLK3
PCICLK2
IREF
ICS954206AG
R458
SS_SEL
R126 33R2
ITP_EN
CLK_IREF
R115 475R2F
REQSEL
CLK_PCI3
CLK_PCI4
CLK_PCI5
R466 33R2
R123 33R2
R124 33R2
PCLK_PCM 22
PCLK_LAN 25
PCLK_MINI 29
31 PCLK_KBC
17 PM_STPPCI#
17 CLK_ICHPCI
R453 10KR2
SS_SEL
R455 10KR2
H/L: 100/96MHz
DREFCLK R520 49D9R2F
DREFCLK# R521 49D9R2F
CLK_PCIE_NEW R451 49D9R2F
CLK_PCIE_NEW# R452 49D9R2F
CLK_XDP_CPU R470 49D9R2F
CLK_XDP_CPU# R465 49D9R2F
CLK_CPU_BCLK R461 49D9R2F
CLK_CPU_BCLK# R464 49D9R2F
CLK_MCH_BCLK R463 49D9R2F
CLK_MCH_BCLK# R462 49D9R2F
DREFSSCLK R450 49D9R2F
DREFSSCLK# R457 49D9R2F
CLK_MCH_3GPLL R441 49D9R2F
CLK_MCH_3GPLL# R442 49D9R2F
CLK_PCIE_ICH R444 49D9R2F
CLK_PCIE_ICH# R443 49D9R2F
21 CLK_PCIE_NEW#
21 CLK_PCIE_NEW
7 CLK_MCH_3GPLL#
7 CLK_MCH_3GPLL
17 CLK_PCIE_ICH#
17 CLK_PCIE_ICH
NEAR CLKGEN
SD 0817
R525 10KR2
REQSEL
R526 DUMMY-R2
R113 10KR2
FS_A
CLK_CPU_BCLK TP87 TPAD30
CLK_CPU_BCLK# TP88 TPAD30
close to CPU
ICS954206AG Spread Spectrum Select
SS3 SS2 SS1 SS0 Spread Amount%
0 0 0 0 -0.8
0 0 0 1 -1.0
0 0 1 0 -1.25
0 0 1 1 -1.5
0 1 0 0 -1.75
0 1 0 1 -2.0
0 1 1 0 -2.5
0 1 1 1 -3.0
1 0 0 0 +-0.3
1 0 0 1 +-0.4
1 0 1 0 +-0.5
1 0 1 1 +-0.6
1 1 0 0 +-0.8
1 1 0 1 +-1.0
1 1 1 0 +-1.25
1 1 1 1 +-1.5
FS_C FS_B FS_A CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator (ICS954206AG)
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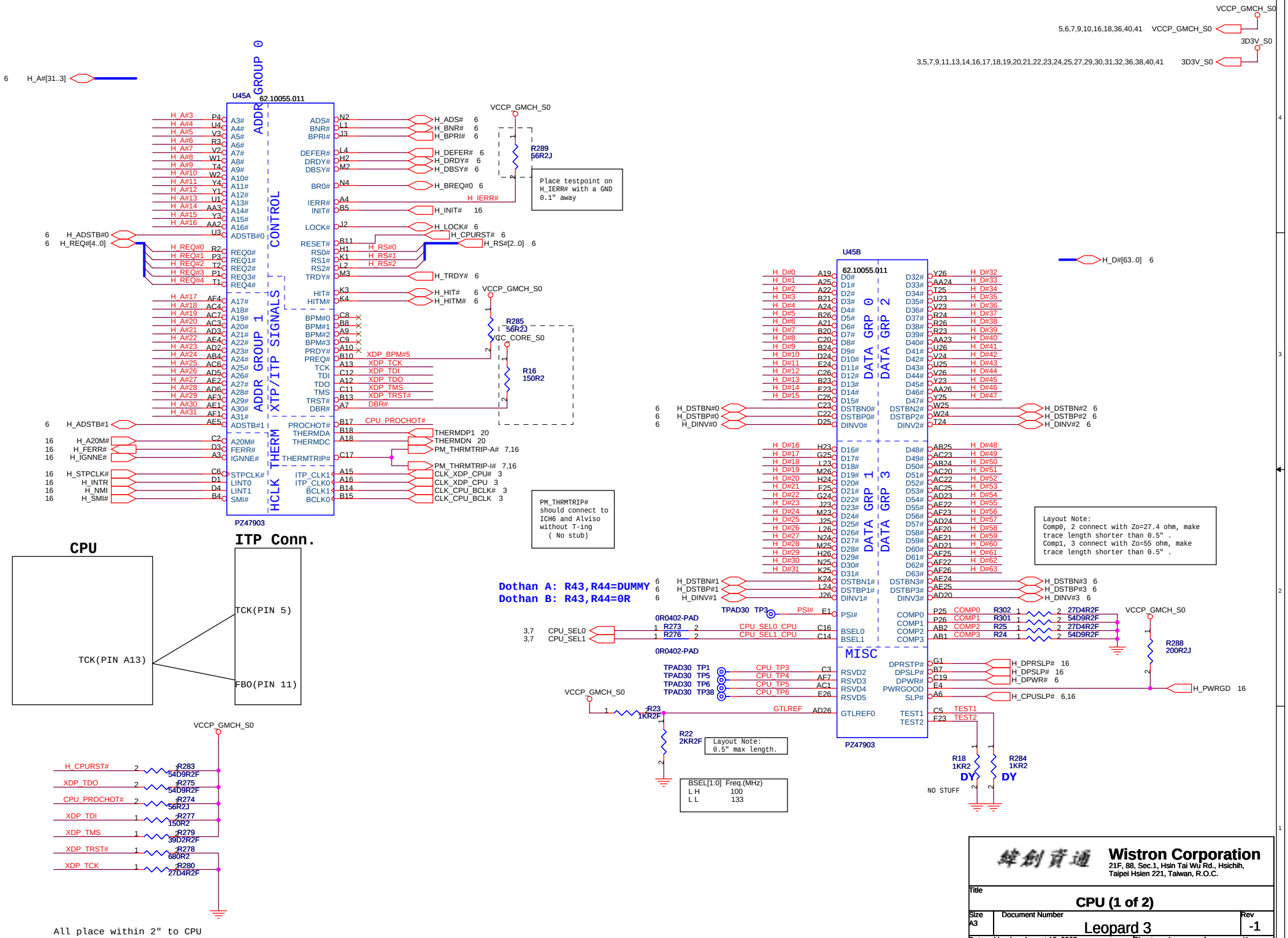

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Title: CPU (1 of 2)

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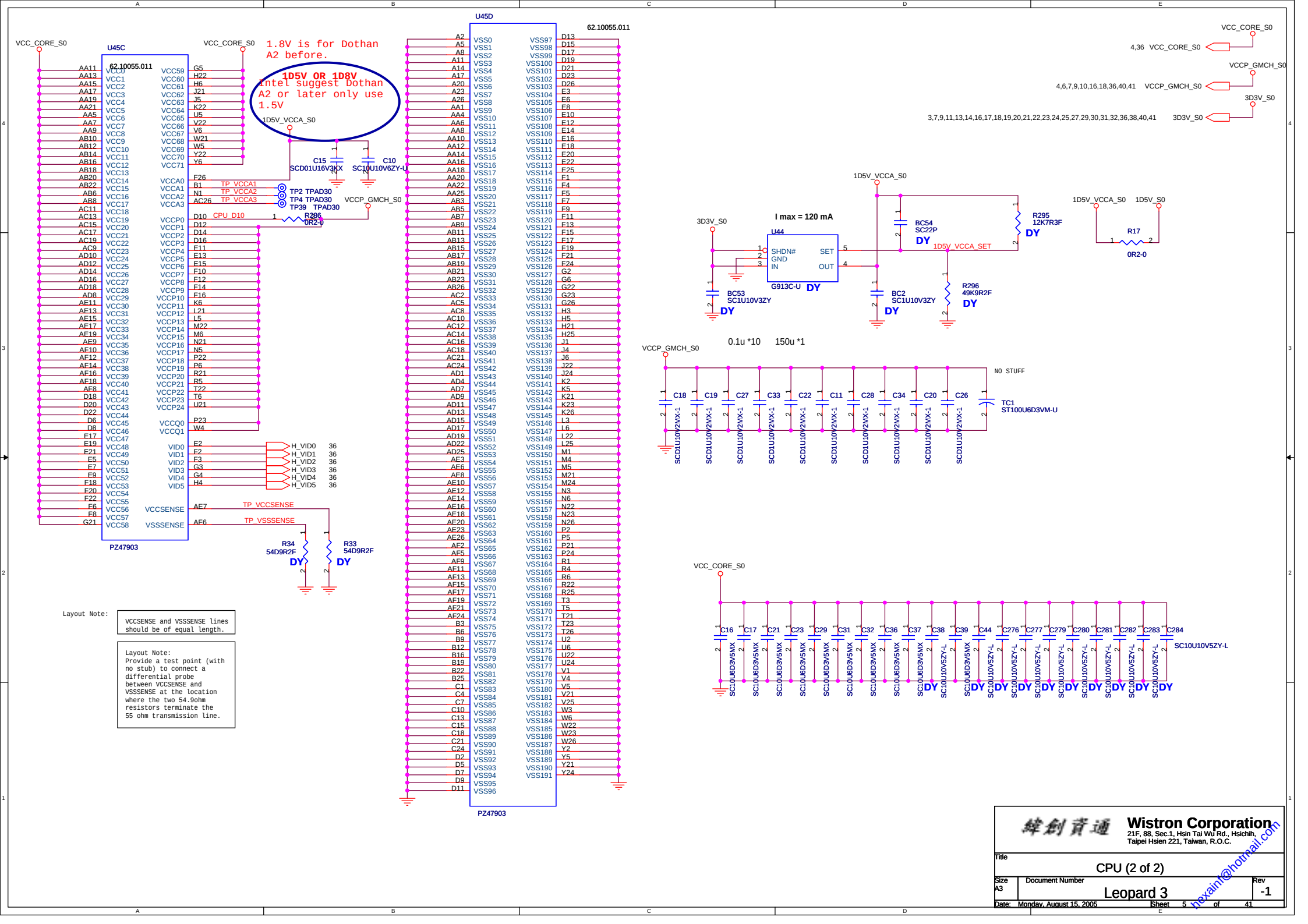
U45C
62.10055.011
PZ47903
U45D
62.10055.011
PZ47903
VCC_CORE_S0
1.8V is for Dothan A2 before.
1D5V OR 1D8V
Intel suggest Dothan A2 or later only use 1.5V
1D5V_VCCA_S0
C15 SCD01U16V3KX
C10 SC10U10V6ZY-U
TP_VCCA1
TP_VCCA2
TP_VCCA3
TP2 TPAD30
TP4 TPAD30
TP39 TPAD30
VCCP_GMCH_S0
CPU_D10
R286 0R2-0
H_VID0 36
H_VID1 36
H_VID2 36
H_VID3 36
H_VID4 36
H_VID5 36
TP_VCCSENSE
TP_VSSSENSE
R34 54D9R2F DY
R33 54D9R2F DY
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
4,36 VCC_CORE_S0
4,6,7,9,10,16,18,36,40,41 VCCP_GMCH_S0
3,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0
I max = 120 mA
U44
SHDN# GND IN SET OUT
G913C-U DY
BC53 SC1U10V3ZY DY
BC54 SC22P DY
BC2 SC1U10V3ZY DY
R295 12K7R3F DY
R296 49K9R2F DY
1D5V_VCCA_SET
R17 0R2-0
0.1u *10
150u *1
NO STUFF
TC1 ST100U6D3VM-U
SCD1U10V2MX-1
SC10U6D3V5MX
SC10U10V5ZY-L
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CPU (2 of 2)
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12/12 Trace 10 mil wide with 20 mil spacing

H_XRCOMP — R69 24D9R2F — 1 2

H_YRCOMP — R87 24D9R2F — 1 2

VCCP_GMCH_S0 — R70 54D9R2F — H_XSCOMP

VCCP_GMCH_S0 — R89 54D9R2F — H_YSCOMP

VCCP_GMCH_S0 — R67 221R3F — H_XSWING — R68 100R2F — C73 SCD1U16V

VCCP_GMCH_S0 — R86 221R3F — H_YSWING — R88 100R2F — C91 SCD1U16V

12/12 Trace 10 mil wide with 20 mil spacing

CORE_GMCH_S0

9,10,40,41 CORE_GMCH_S0

VCCP_GMCH_S0

4,5,7,9,10,16,18,36,40,41 VCCP_GMCH_S0

4 H_D#[63..0]

U17A

H_D#0	E4	HD0#	HA3#	G9	H_A#3
H_D#1	E1	HD1#	HA4#	C9	H_A#4
H_D#2	F4	HD2#	HA5#	E9	H_A#5
H_D#3	H7	HD3#	HA6#	B7	H_A#6
H_D#4	E2	HD4#	HA7#	A10	H_A#7
H_D#5	F1	HD5#	HA8#	F9	H_A#8
H_D#6	E3	HD6#	HA9#	D8	H_A#9
H_D#7	D3	HD7#	HA10#	B10	H_A#10
H_D#8	K7	HD8#	HA11#	E10	H_A#11
H_D#9	F2	HD9#	HA12#	G10	H_A#12
H_D#10	J7	HD10#	HA13#	D9	H_A#13
H_D#11	J8	HD11#	HA14#	E11	H_A#14
H_D#12	H6	HD12#	HA15#	F10	H_A#15
H_D#13	F3	HD13#	HA16#	G11	H_A#16
H_D#14	K8	HD14#	HA17#	G13	H_A#17
H_D#15	H5	HD15#	HA18#	C10	H_A#18
H_D#16	H1	HD16#	HA19#	C11	H_A#19
H_D#17	H2	HD17#	HA20#	D11	H_A#20
H_D#18	K5	HD18#	HA21#	C12	H_A#21
H_D#19	K6	HD19#	HA22#	B13	H_A#22
H_D#20	J4	HD20#	HA23#	A12	H_A#23
H_D#21	G3	HD21#	HA24#	E12	H_A#24
H_D#22	H3	HD22#	HA25#	G12	H_A#25
H_D#23	J1	HD23#	HA26#	E12	H_A#26
H_D#24	L5	HD24#	HA27#	C13	H_A#27
H_D#25	K4	HD25#	HA28#	B11	H_A#28
H_D#26	J5	HD26#	HA29#	D13	H_A#29
H_D#27	P7	HD27#	HA30#	A13	H_A#30
H_D#28	L7	HD28#	HA31#	F13	H_A#31
H_D#29	J3	HD29#			
H_D#30	P5	HD30#			
H_D#31	L3	HD31#			
H_D#32	U7	HD32#			
H_D#33	V6	HD33#			
H_D#34	R6	HD34#			
H_D#35	R5	HD35#			
H_D#36	P3	HD36#			
H_D#37	T8	HD37#			
H_D#38	R7	HD38#			
H_D#39	R8	HD39#			
H_D#40	U8	HD40#			
H_D#41	R4	HD41#			
H_D#42	T4	HD42#			
H_D#43	T5	HD43#			
H_D#44	R1	HD44#			
H_D#45	T3	HD45#			
H_D#46	V8	HD46#			
H_D#47	U6	HD47#			
H_D#48	W6	HD48#			
H_D#49	U3	HD49#			
H_D#50	V5	HD50#			
H_D#51	W8	HD51#			
H_D#52	W7	HD52#			
H_D#53	U2	HD53#			
H_D#54	U1	HD54#			
H_D#55	Y5	HD55#			
H_D#56	Y2	HD56#			
H_D#57	V4	HD57#			
H_D#58	Y7	HD58#			
H_D#59	W1	HD59#			
H_D#60	W3	HD60#			
H_D#61	Y3	HD61#			
H_D#62	Y6	HD62#			
H_D#63	W2	HD63#			

HOST

H_XRCOMP	C1	HXRCOMP	
H_XSCOMP	C2	HXSCOMP	
H_XSWING	D1	HXSWING	
H_YRCOMP	T1	HYRCOMP	
H_YSCOMP	L1	HYSCOMP	
H_YSWING	P1	HYSWING	

HADS#	F8	H_ADS#	4
HADSTB#0	B9	H_ADSTB#0	4
HADSTB#1	E13	H_ADSTB#1	4
HVREF	J11	H_VREF	
HBNR#	A5	H_BNR#	4
HBPRI#	D5	H_BPRI#	4
HBREQ0#	E7	H_BREQ#0	4
HCPURST#	H10	H_CPURST#	4
HCLKINN	AB1	CLK_MCH_BCLK#	3
HCLKINP	AB2	CLK_MCH_BCLK	3
HDBSY#	C6	H_DBSY#	4
HDEFER#	E6	H_DEFER#	4
HDINV#0	H8	H_DINV#0	
HDINV#1	K3	H_DINV#1	
HDINV#2	T7	H_DINV#2	
HDINV#3	U5	H_DINV#3	
HDPWR#	G6	H_DPWR#	4
HDRDY#	E7	H_DRDY#	4
HDSTBN#0	G4	H_DSTBN#0	
HDSTBN#1	K1	H_DSTBN#1	
HDSTBN#2	R3	H_DSTBN#2	
HDSTBN#3	V3	H_DSTBN#3	
HDSTBP#0	G5	H_DSTBP#0	
HDSTBP#1	K2	H_DSTBP#1	
HDSTBP#2	R2	H_DSTBP#2	
HDSTBP#3	W4	H_DSTBP#3	
HEDRDY#	F6	TP_H_EDRDY#	TP42 TPAD30
HHIT#	D4	H_HIT#	4
HHITM#	D6	H_HITM#	4
HLOCK#	B3	H_LOCK#	4
HPCREQ#	A11	TP_H_PCREQ#	TP9 TPAD30
HREQ#0	A7	H_REQ#0	
HREQ#1	D7	H_REQ#1	
HREQ#2	B8	H_REQ#2	
HREQ#3	C7	H_REQ#3	
HREQ#4	A8	H_REQ#4	
HRS0#	A4	H_RS#0	
HRS1#	C5	H_RS#1	
HRS2#	B4	H_RS#2	
HCPUSLP#	G8	H_CPUSLP#_GMCH	0R0402-PAD R311
HTRDY#	B5	H_TRDY#	4

H_A#[31..3] 4

H_DINV#[3..0] 4

H_DSTBN#[3..0] 4

H_DSTBP#[3..0] 4

H_REQ#[4..0] 4

H_RS#[2..0] 4

H_CPUSLP# 4,16

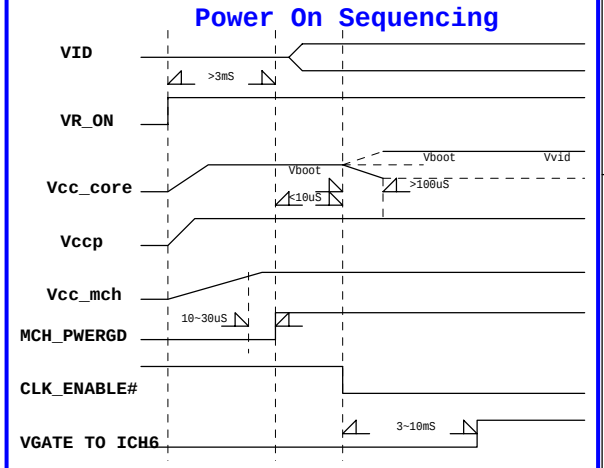
VCCP_GMCH_S0 — R336 100R2F — H_VREF — R337 200R2F — C308 SCD1U10V2KX

CORE_GMCH_S0 — R391 0R2-0 — DY — H_DPWR#

ALVISO-GM

For Banias/Celeron-M:R93=DUMMY
For Dothan A:R93=DUMMY
For Dothan B:R93=0R

Power On Sequencing



Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	0 = DDR2 **1 = DDR1 (Default)**
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present(Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

ALVISO-GM:71.0GMCH.08U
ALVISO-PM:71.0GMCH.0BU
ALVISO-GML:71.0GMCH.0JU

Wistron Corporation
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Title: GMCH (1 of 5)

Size: A3 | Document Number: Leopard 3 | Rev: -1

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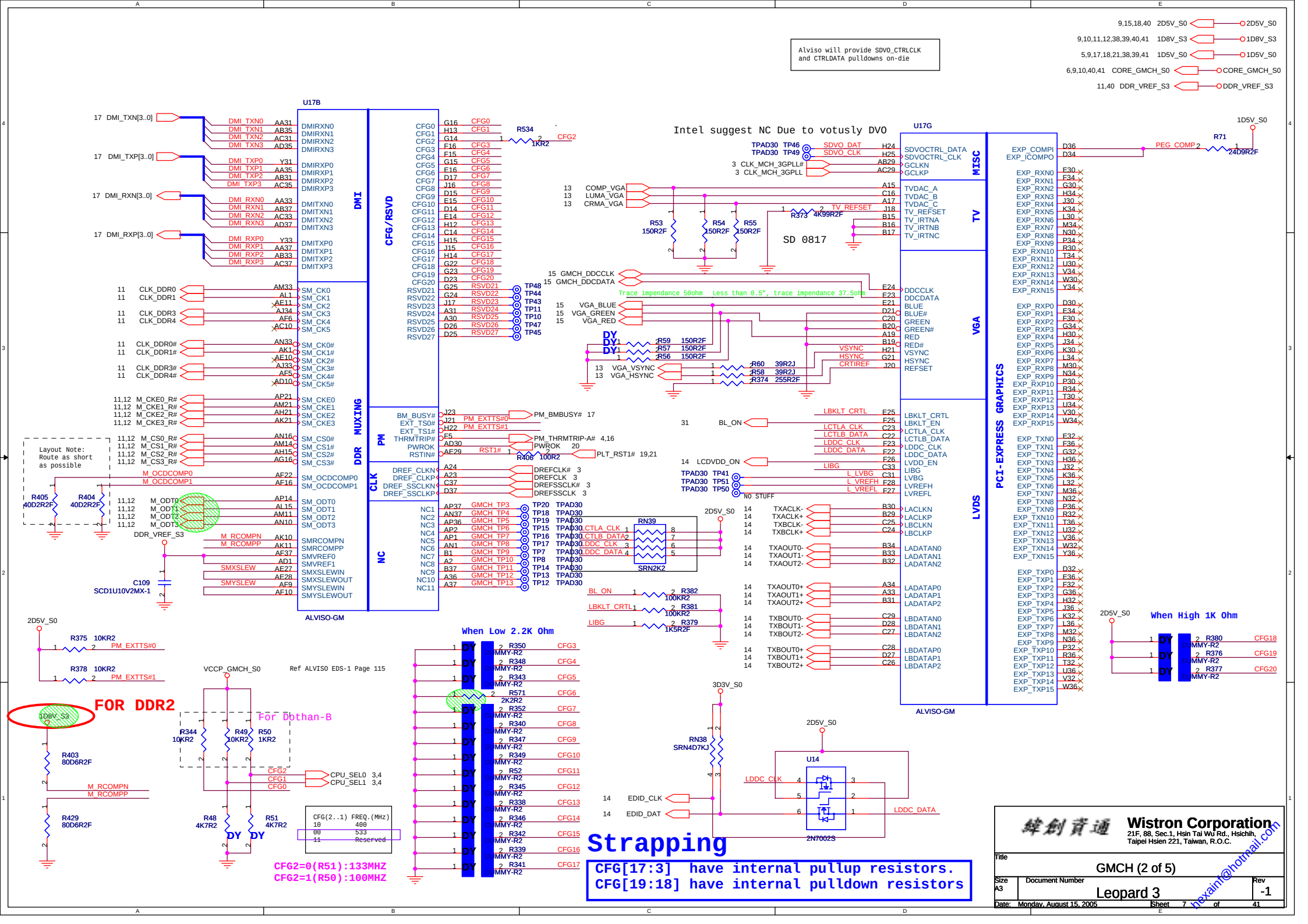
U17B
DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
ALVISO-GM
U17G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
Intel suggest NC Due to votusly DVO
SD 0817
Trace impendance 50ohm Less than 0.5", trace impendance 37.5ohm
Layout Note: Route as short as possible
FOR DDR2
For Dothan-B
Ref ALVISO EDS-1 Page 115
When Low 2.2K Ohm
When High 1K Ohm
Strapping
CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors
CFG2=0(R51):133MHZ
CFG2=1(R50):100MHZ
Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die
Wistron Corporation
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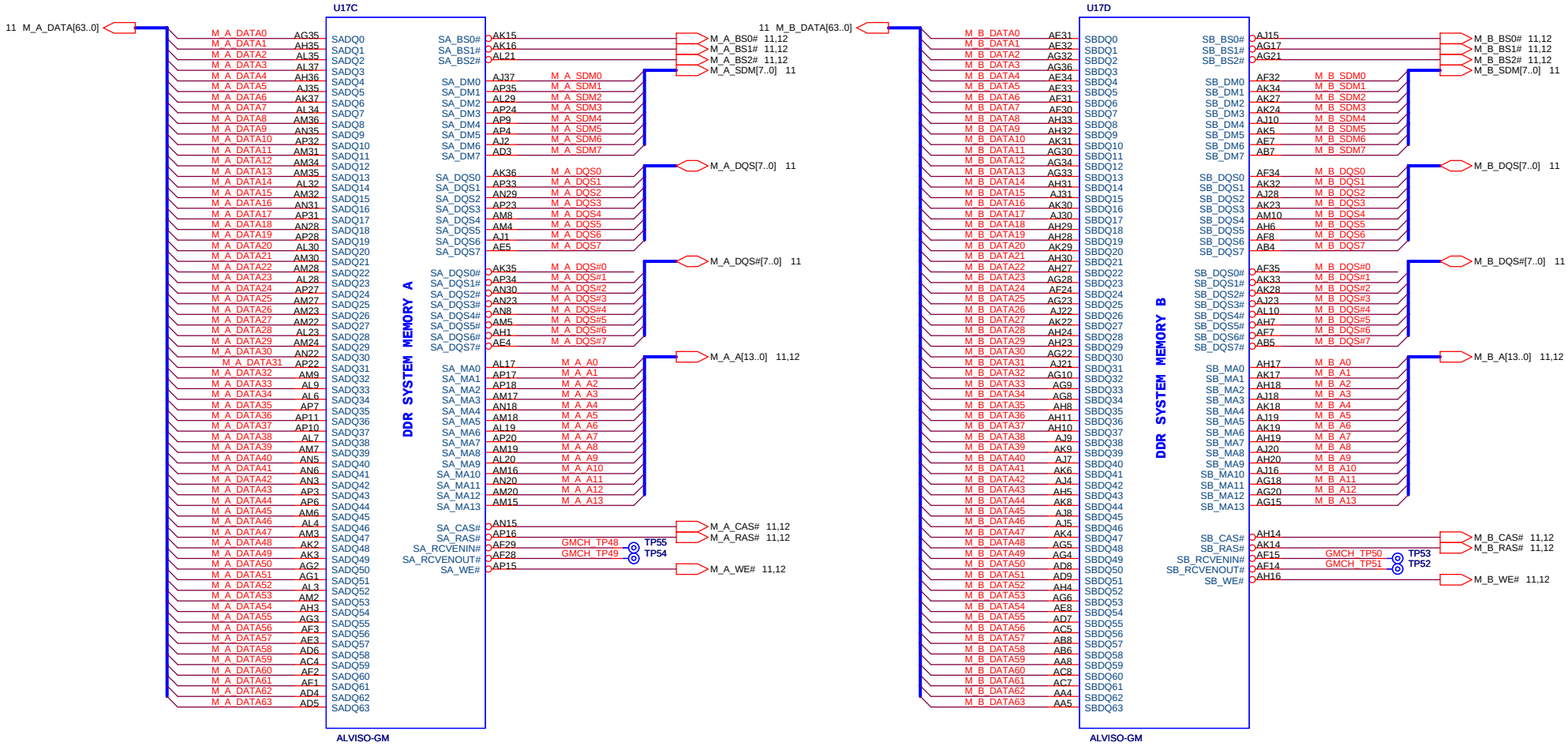
GMCH (2 of 5)
Leopard 3
Monday, August 15, 2005



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (3 of 5)

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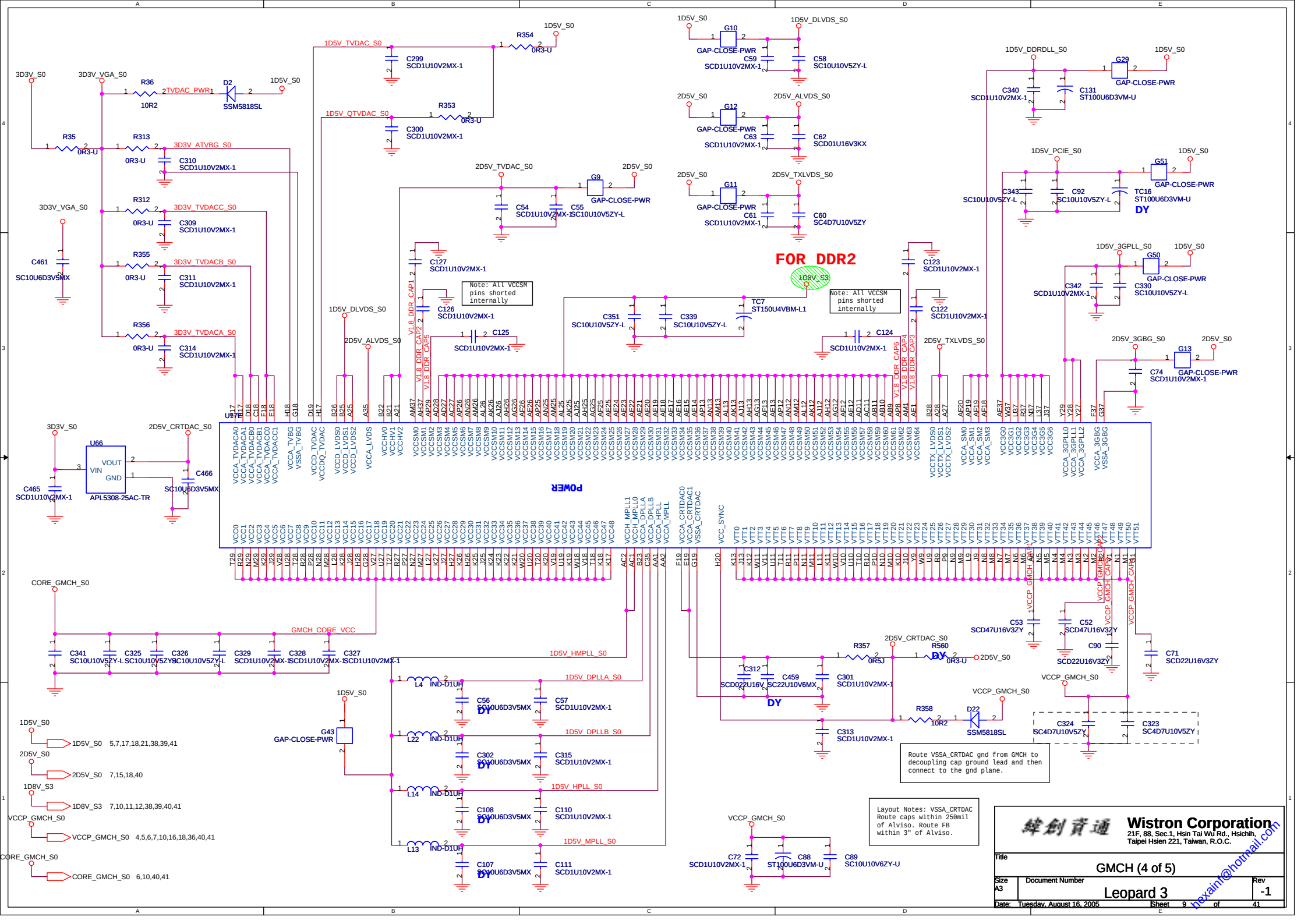
Date: Tuesday, July 12, 2005 | Sheet 8 of 41


FOR DDR2
POWER
Note: All VCCSM pins shorted internally
Note: All VCCSM pins shorted internally
Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
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Title
GMCH (4 of 5)
Size A3
Document Number
Leopard 3
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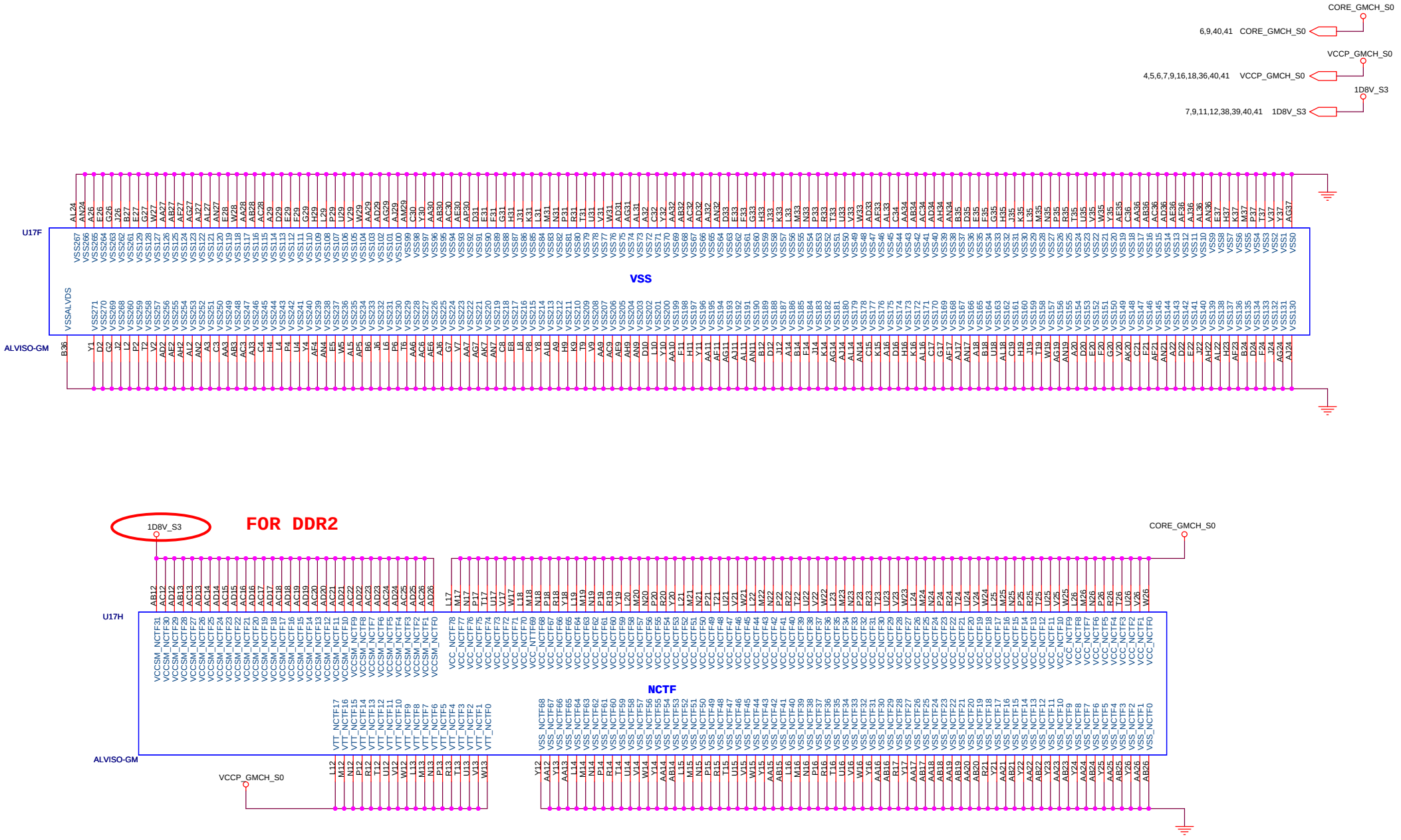
Date: Tuesday, August 16, 2005
Sheet 9 of 41
nexaint@hotmail.com



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GMCH (5 of 5)
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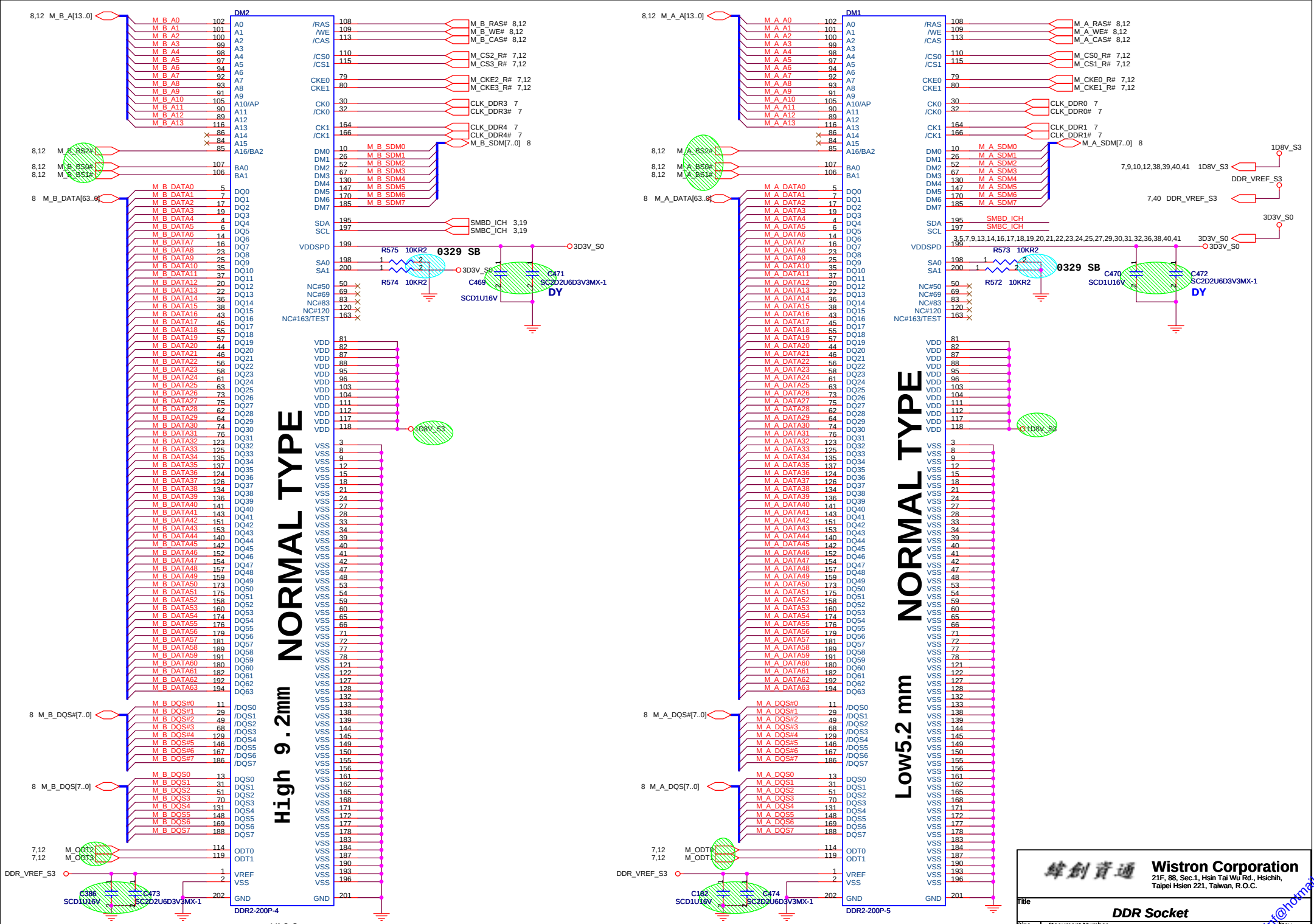

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR Socket

Size: Custom | Document Number: Leopard 3 | Rev: -1

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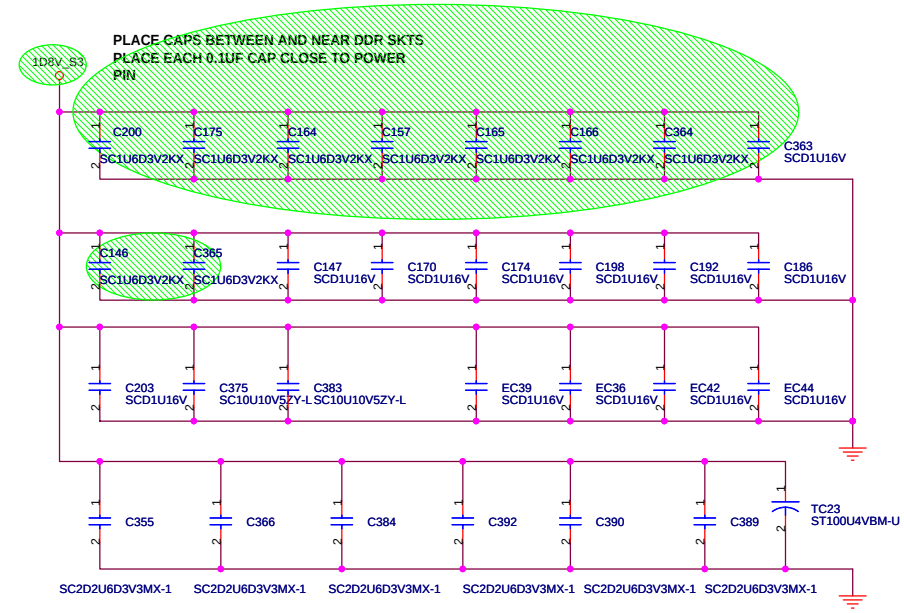
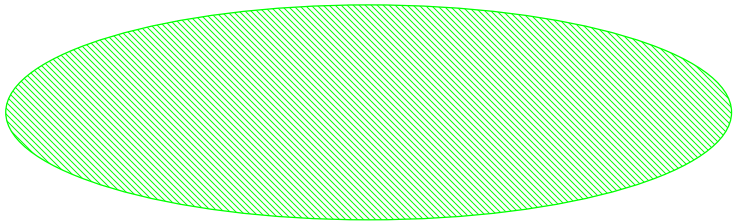
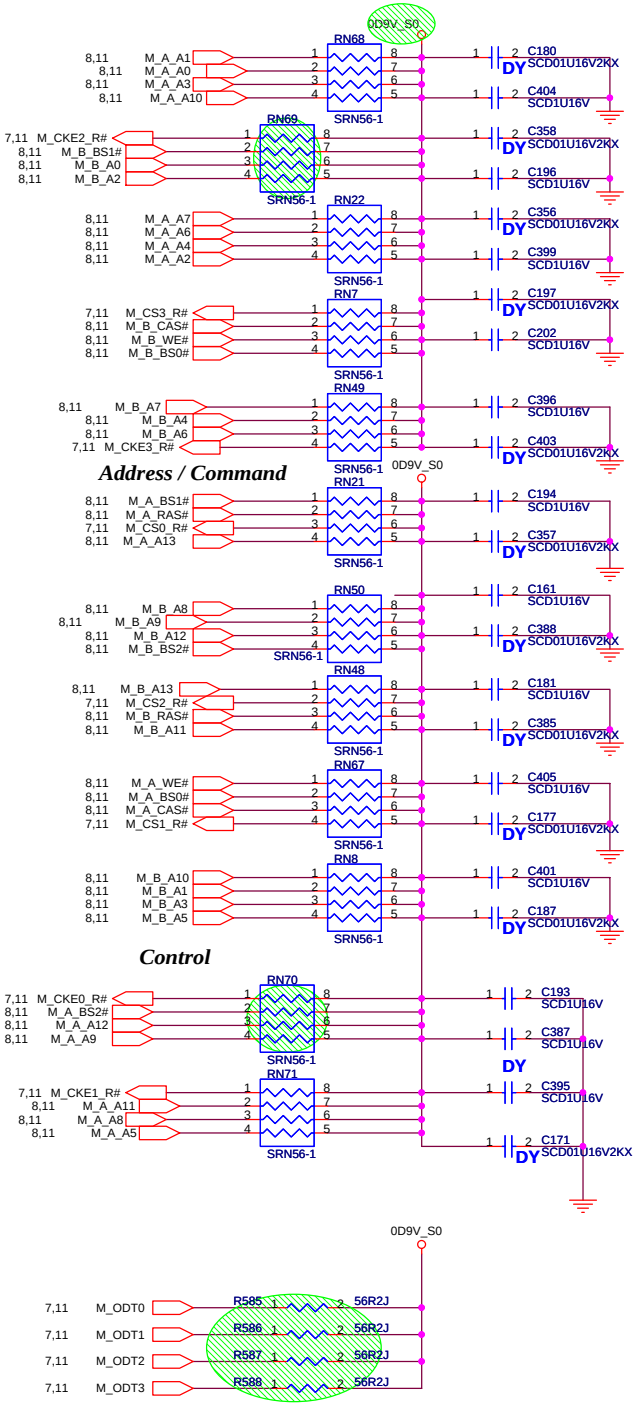
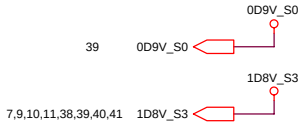


For 1GB Memory







緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR Serial/Terminator Resistor***	
Size A3	Document Number: Leopard 3	Rev: -1
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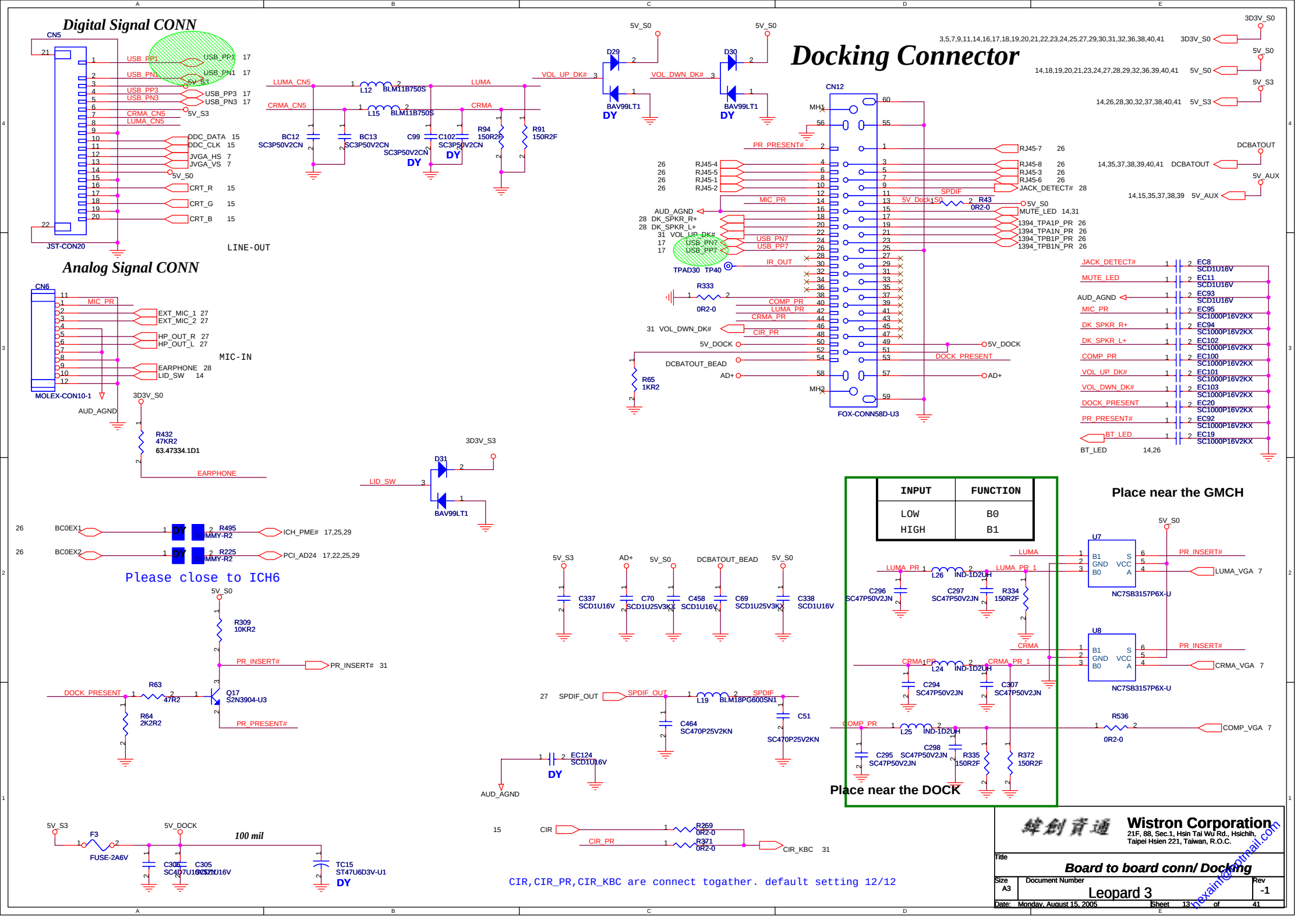
Digital Signal CONN
CN5
JST-CON20
LINE-OUT
Analog Signal CONN
CN6
MOLEX-CON10-1
MIC-IN
Docking Connector
CN12
FOX-CONN58D-U3
Please close to ICH6
Place near the GMCH
Place near the DOCK
INPUT
FUNCTION
LOW
B0
HIGH
B1
100 mil
CIR,CIR_PR,CIR_KBC are connect togather. default setting 12/12
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
Board to board conn/ Docking
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-1
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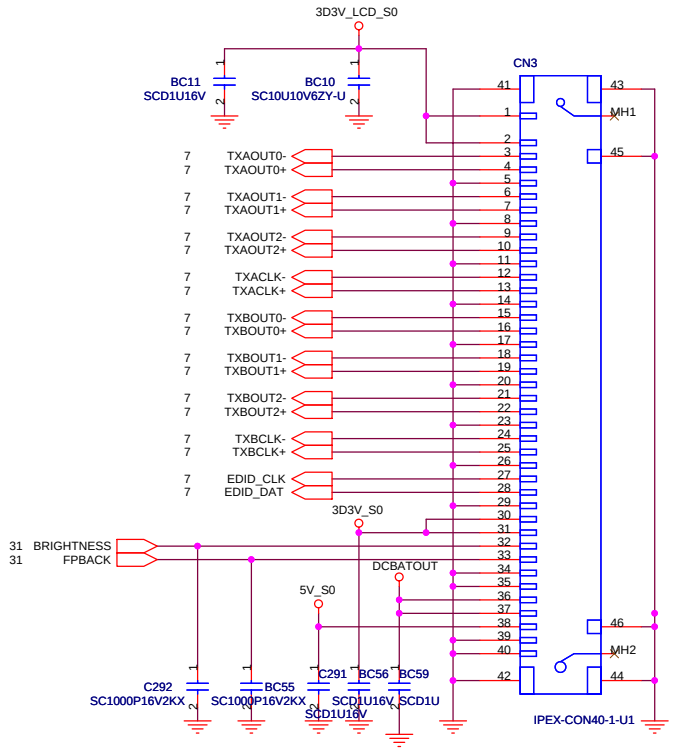
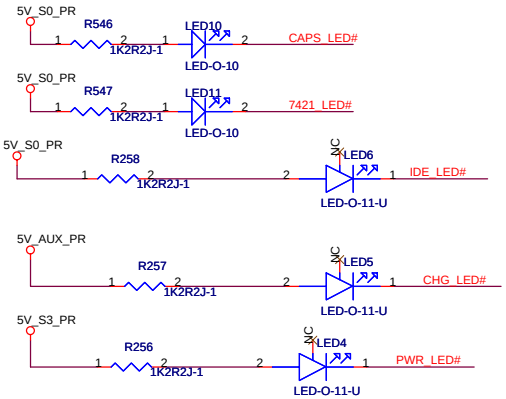
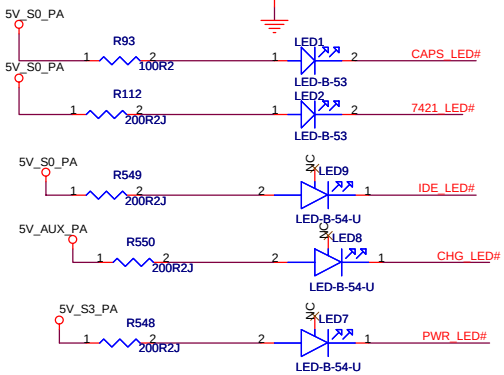
INVERTER/LCD

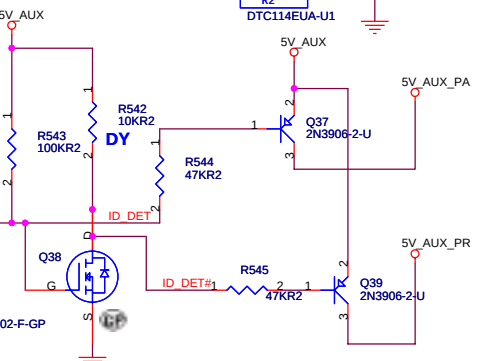


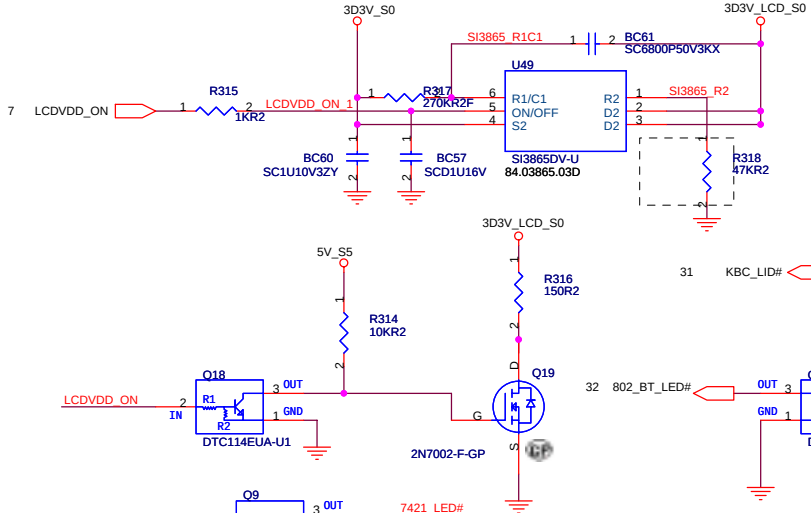
		PWR	CHR	HDD	IR	CAPS	7421
PR Botton		Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top		Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2

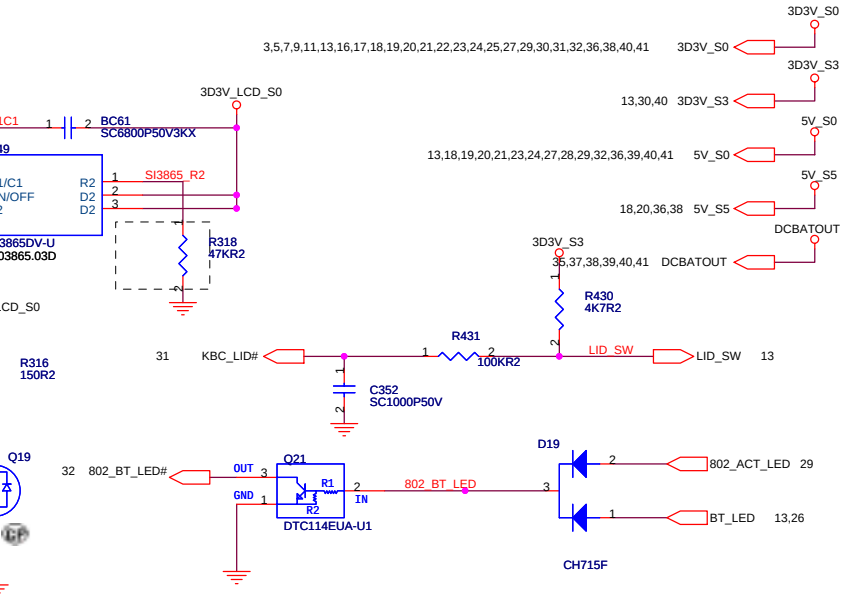
change R from 100 to 200 ohm











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Title	Inverter/LCD		
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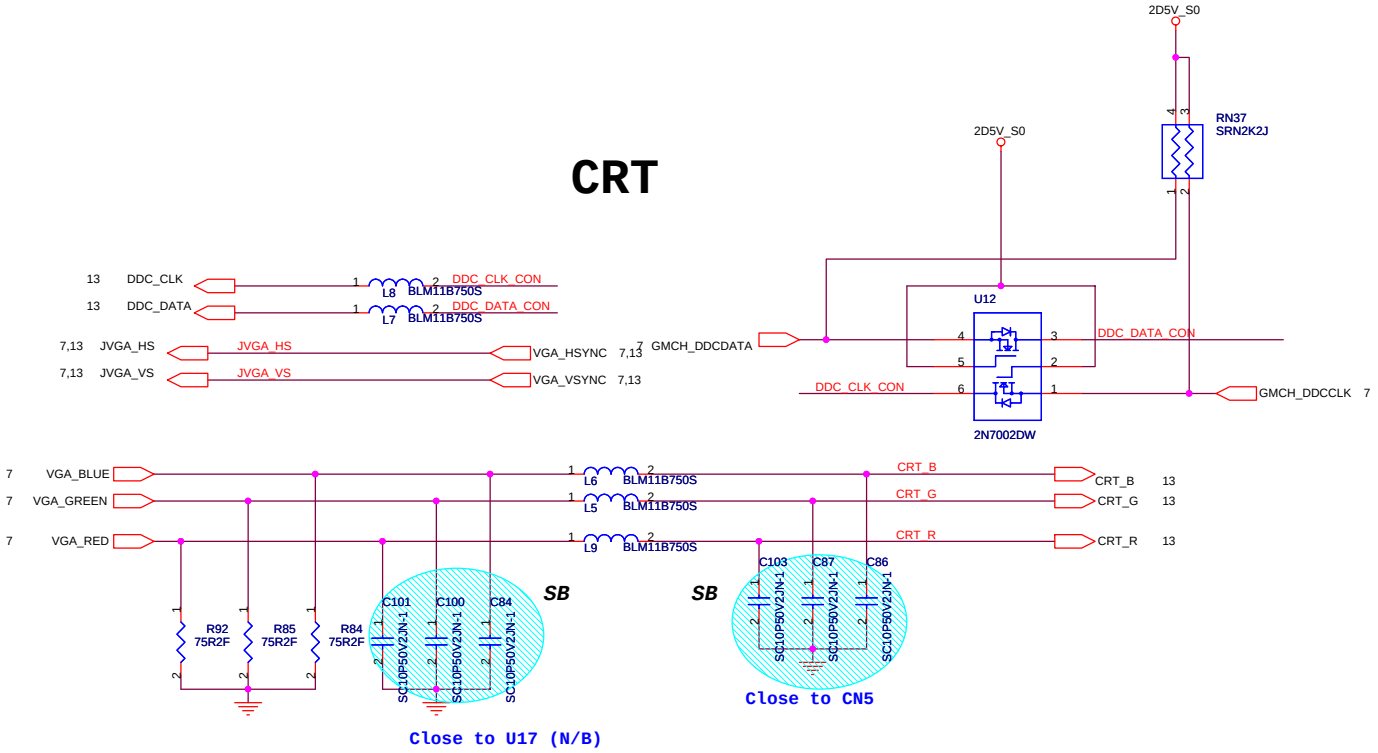
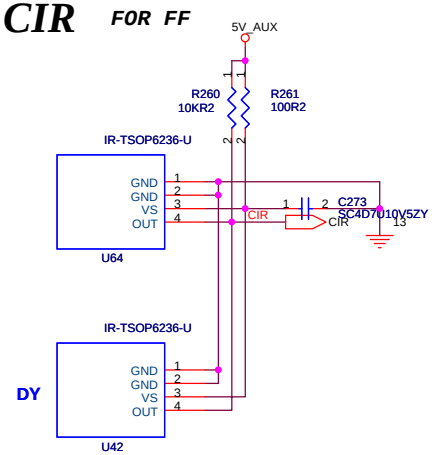
PA & PR diffent parts

	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED2	83.00190.Y70	83.00190.W70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	Dummy	83.00110.D70
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
LED9	83.00110.E70	Dummy
U64	56.15006.001	Dummy
U42	Dummy	56.15006.001
R256	63.20134.1D1	63.12234.1D1
R257	63.20134.1D1	63.12234.1D1
R258	63.20134.1D1	63.12234.1D1
R93	63.20134.1D1	63.12234.1D1
R112	63.20134.1D1	63.12234.1D1
CBUS1	21.H0088.001	21.H0088.001
R176	63.10334.1D1	Dummy
R177	Dummy	63.10334.1D1

CRT



CIR FOR FF



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Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/ CIR

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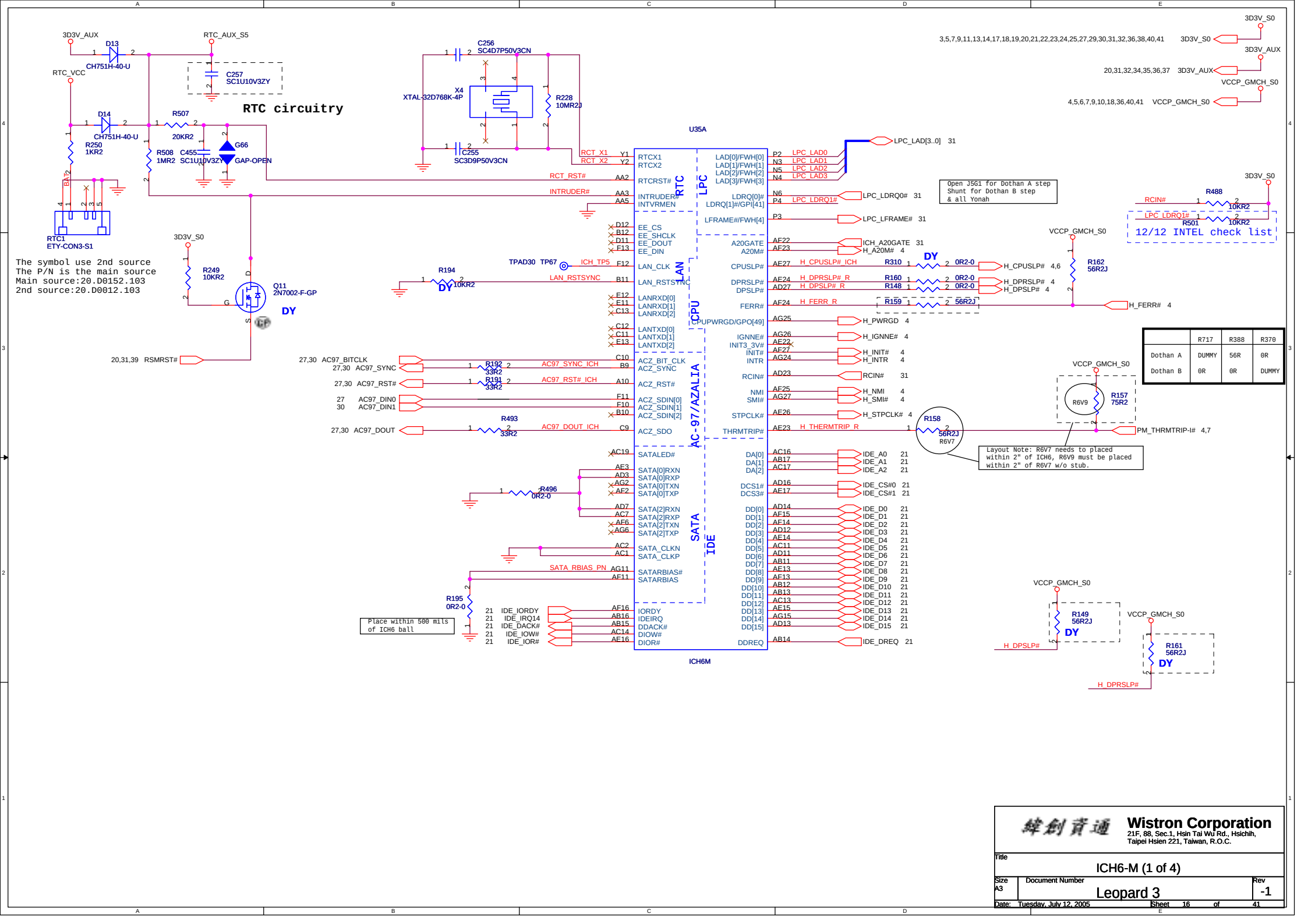
RTC circuitry
The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103
U35A
ICH6M
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
Open J561 for Dothan A step
Shunt for Dothan B step
& all Yonah
12/12 INTEL check list
Place within 500 mils of ICH6 ball
Layout Note: R6V7 needs to placed within 2" of ICH6, R6V9 must be placed within 2" of R6V7 w/o stub.
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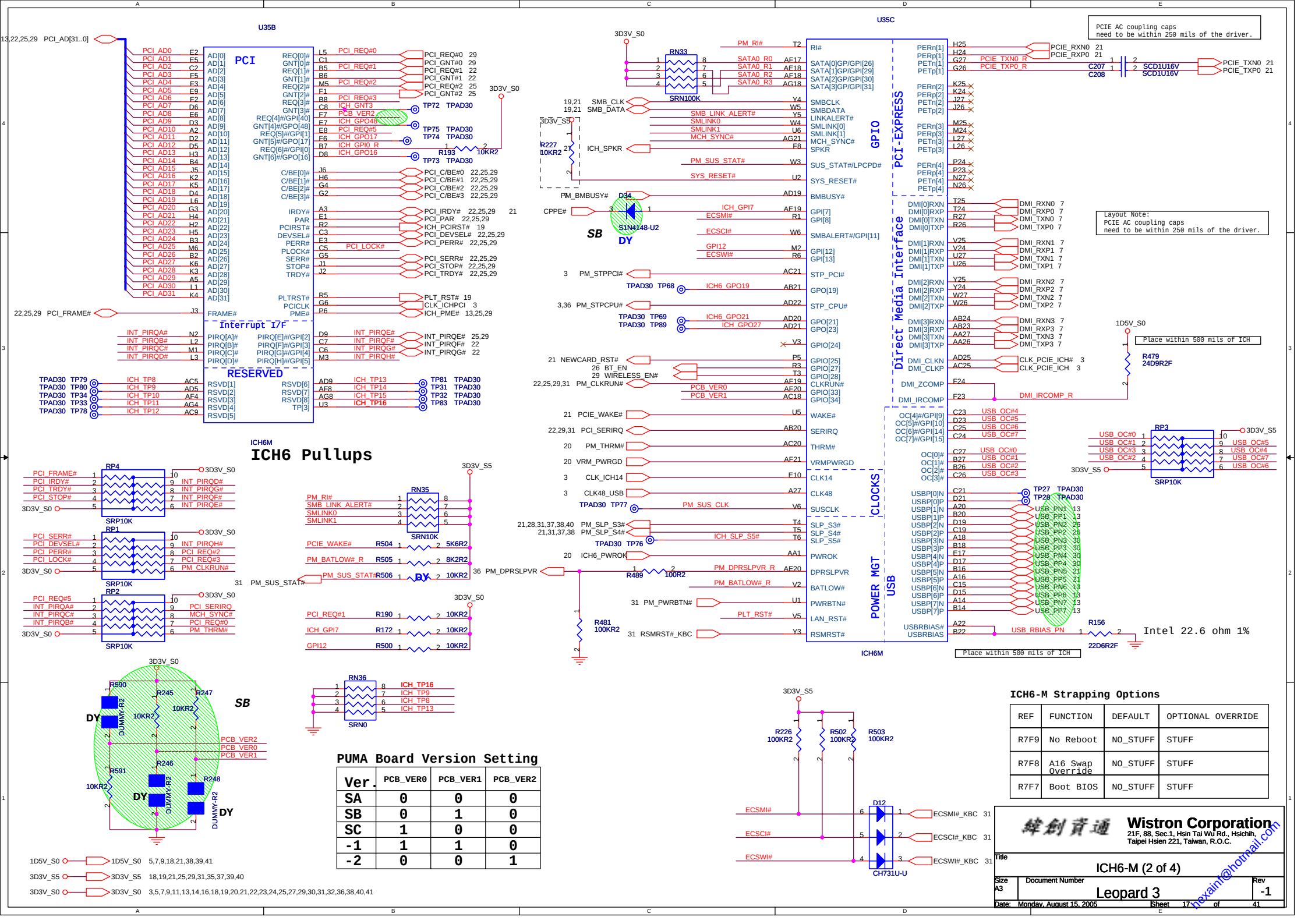
ICH6-M (1 of 4)
Leopard 3
Tuesday, July 12, 2005



PUMA Board Version Setting

Ver.	PCB_VER0	PCB_VER1	PCB_VER2
SA	0	0	0
SB	0	1	0
SC	1	0	0
-1	1	1	0
-2	0	0	1

ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

1D5V_S0 1D5V_S0 5,7,9,18,21,38,39,41
3D3V_S5 3D3V_S5 18,19,21,25,29,31,35,37,39,40
3D3V_S0 3D3V_S0 3,5,7,9,11,13,14,16,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41

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Title: ICH6-M (2 of 4)
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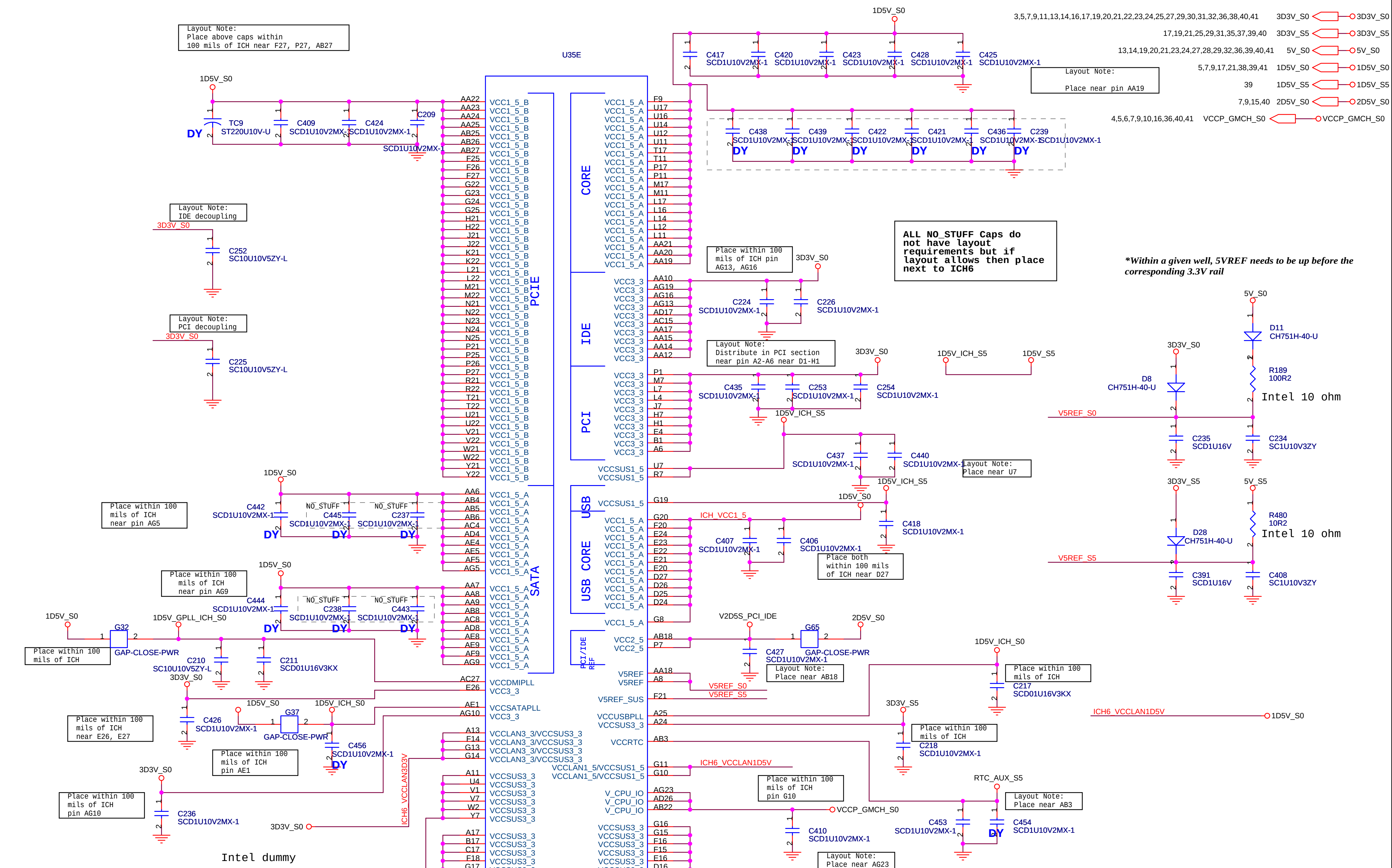
U35E
ICH6M
PCIE
CORE
IDE
PCI
USB
USB CORE
SATA
PCI/IDE REF
1D5V_S0
3D3V_S0
3D3V_S5
5V_S0
5V_S5
1D5V_S5
2D5V_S0
VCCP_GMCH_S0
1D5V_ICH_S5
1D5V_ICH_S0
1D5V_GPLL_ICH_S0
V2D5S_PCI_IDE
RTC_AUX_S5
V5REF_S0
V5REF_S5
ICH_VCC1_5
ICH6_VCCLAN1D5V
ICH6_VCCLAN3D3V
3,5,7,9,11,13,14,16,17,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41
17,19,21,25,29,31,35,37,39,40
13,14,19,20,21,23,24,27,28,29,32,36,39,40,41
5,7,9,17,21,38,39,41
39
7,9,15,40
4,5,6,7,9,10,16,36,40,41
Layout Note: Place above caps within 100 mils of ICH near F27, P27, AB27
Layout Note: Place near pin AA19
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Place within 100 mils of ICH pin AG13, AG16
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
Intel 10 ohm
Layout Note: Place near U7
Place within 100 mils of ICH near pin AG5
Place both within 100 mils of ICH near D27
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH
Layout Note: Place near AB18
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin G10
Layout Note: Place near AB3
Place within 100 mils of ICH pin AG10
Layout Note: Place near AG23
Intel dummy
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin A17
TC9 ST220U10V-U
C252 SC10U10V5ZY-L
C225 SC10U10V5ZY-L
C210 SC10U10V5ZY-L
C211 SCD01U16V3KX
C217 SCD01U16V3KX
C235 SCD1U16V
C391 SCD1U16V
C234 SC1U10V3ZY
C408 SC1U10V3ZY
D11 CH751H-40-U
D8 CH751H-40-U
D28 CH751H-40-U
R189 100R2
R480 10R2
G32 GAP-CLOSE-PWR
G37 GAP-CLOSE-PWR
G65 GAP-CLOSE-PWR
SCD1U10V2MX-1
NO_STUFF
DY

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Title	ICH6-M (3 of 4)	
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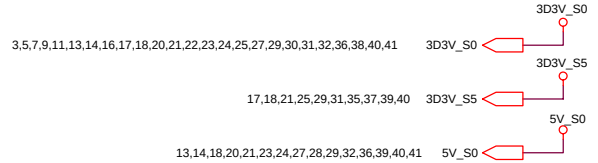
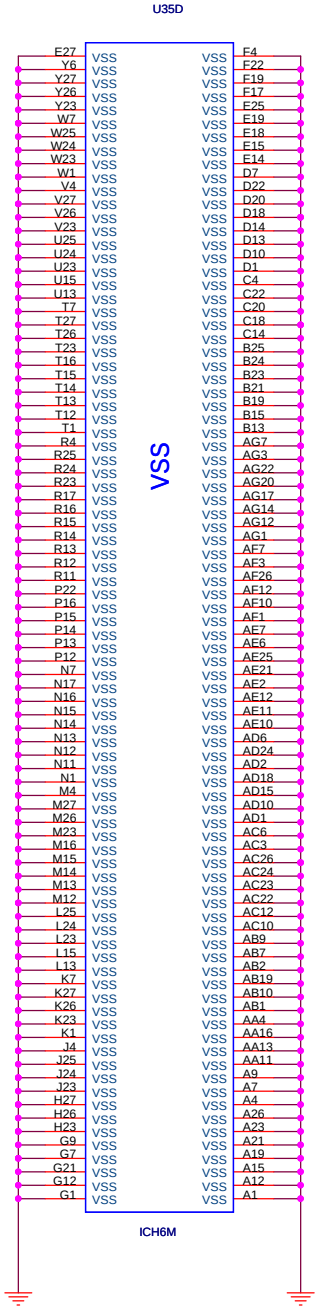
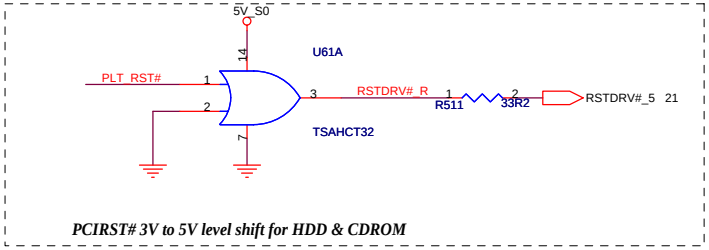
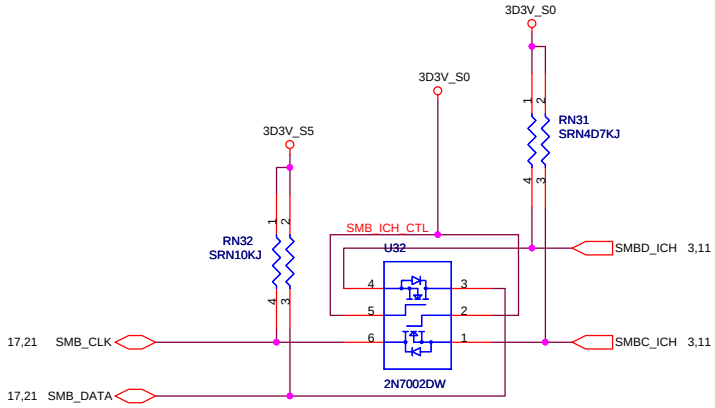
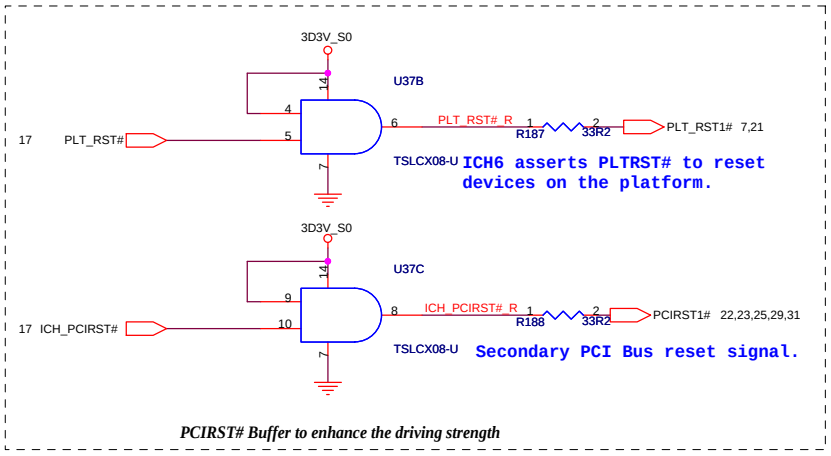






SMBUS(ICH6 ---> SODIMM,CLKGEN)





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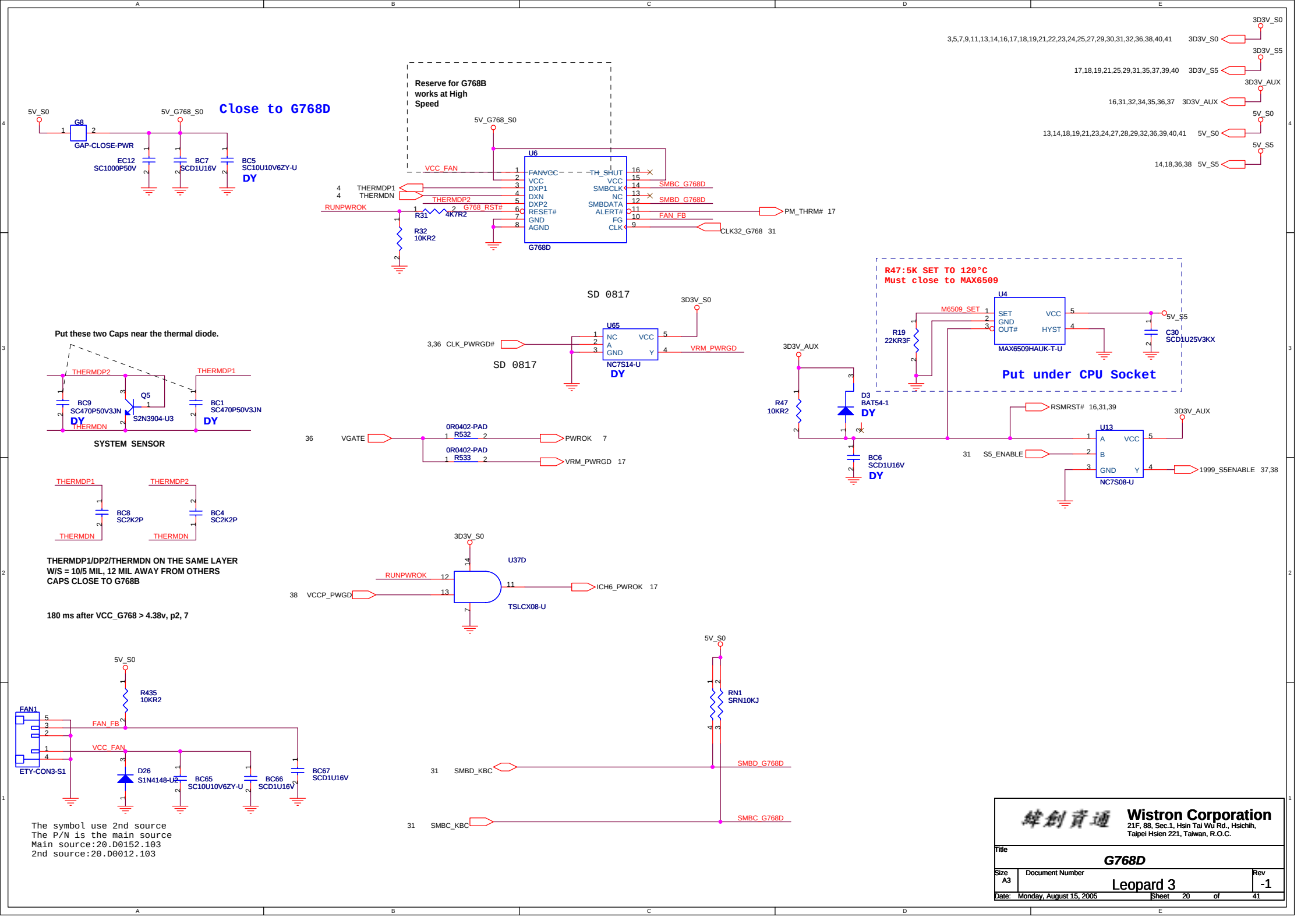
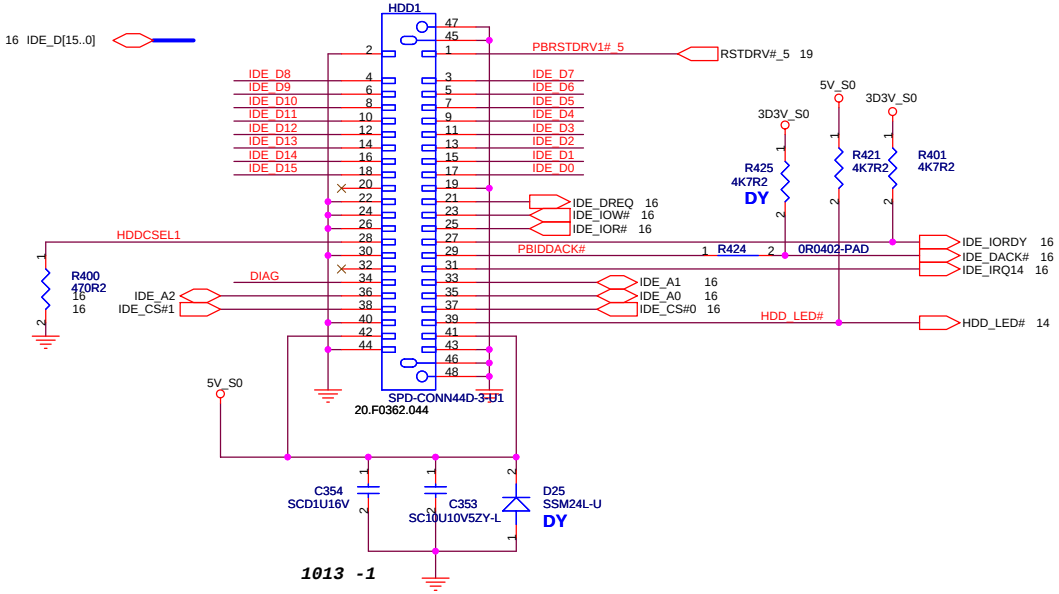
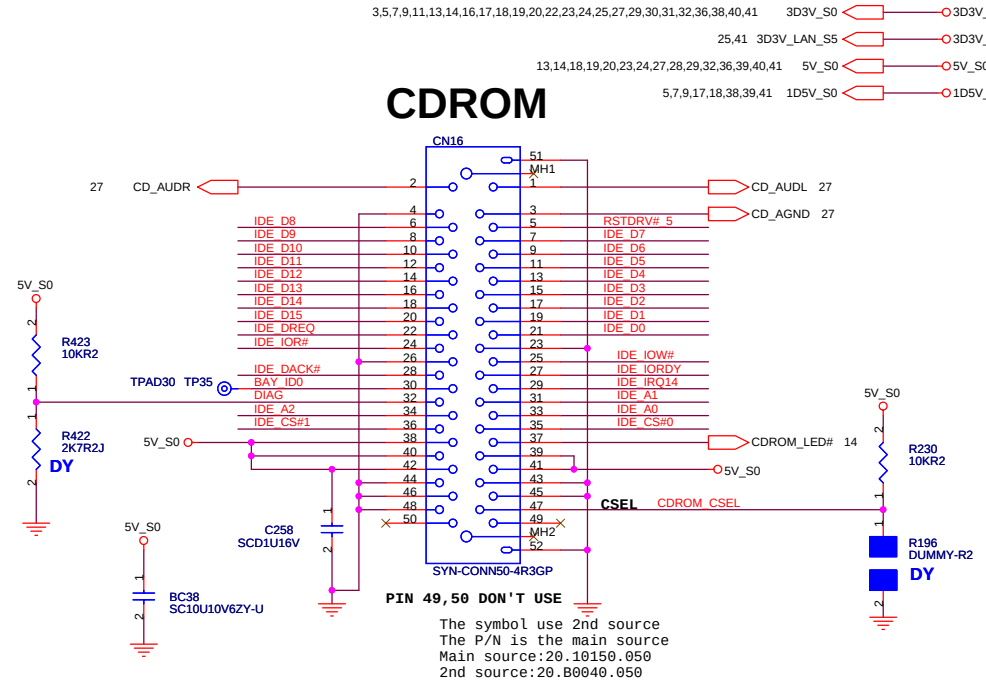

Close to G768D
5V_S0
5V_G768_S0
G8
GAP-CLOSE-PWR
EC12
SC1000P50V
BC7
SCD1U16V
BC5
SC10U10V6ZY-U
DY
Reserve for G768B
works at High
Speed
U6
VCC_FAN
THERMDP1
THERMDN
THERMDP2
RUNPWROK
R31
4K7R2
G768_RST#
R32
10KR2
FANVCC
VCC
DXP1
DXN
DXP2
RESET#
GND
AGND
TH_SHUT
SMBCLK
NC
SMBDATA
ALERT#
FG
CLK
SMBC_G768D
SMBD_G768D
FAN_FB
PM_THRM# 17
CLK32_G768 31
G768D
3D3V_S0
3,5,7,9,11,13,14,16,17,18,19,21,22,23,24,25,27,29,30,31,32,36,38,40,41
3D3V_S5
17,18,19,21,25,29,31,35,37,39,40
3D3V_AUX
16,31,32,34,35,36,37
5V_S0
13,14,18,19,21,23,24,27,28,29,32,36,39,40,41
5V_S5
14,18,36,38
SD 0817
U65
3,36 CLK_PWRGD#
NC
A
GND
VCC
Y
VRM_PWRGD
NC7S14-U
DY
SD 0817
R47:5K SET TO 120°C
Must close to MAX6509
U4
M6509_SET
SET
GND
OUT#
VCC
HYST
MAX6509HAUK-T-U
R19
22KR3F
C30
SCD1U25V3KX
Put under CPU Socket
3D3V_AUX
R47
10KR2
D3
BAT54-1
DY
BC6
SCD1U16V
DY
RSMRST# 16,31,39
31 S5_ENABLE
U13
A
B
GND
VCC
Y
NC7S08-U
1999_S5ENABLE 37,38
Put these two Caps near the thermal diode.
THERMDP2
THERMDP1
BC9
SC470P50V3JN
DY
Q5
S2N3904-U3
BC1
SC470P50V3JN
DY
THERMDN
SYSTEM SENSOR
36 VGATE
0R0402-PAD
R532
PWROK 7
0R0402-PAD
R533
VRM_PWRGD 17
THERMDP1
THERMDP2
BC8
SC2K2P
BC4
SC2K2P
THERMDN
THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B
180 ms after VCC_G768 > 4.38v, p2, 7
3D3V_S0
U37D
RUNPWROK
38 VCCP_PWGD
ICH6_PWROK 17
TSLCX08-U
5V_S0
R435
10KR2
FAN1
FAN_FB
VCC_FAN
ETY-CON3-S1
D26
S1N4148-U2
BC65
SC10U10V6ZY-U
BC66
SCD1U16V
BC67
SCD1U16V
5V_S0
RN1
SRN10KJ
31 SMBD_KBC
SMBD_G768D
31 SMBC_KBC
SMBC_G768D
The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G768D
Size
A3
Document Number
Leopard 3
Rev
-1
Date: Monday, August 15, 2005
Sheet 20 of 41

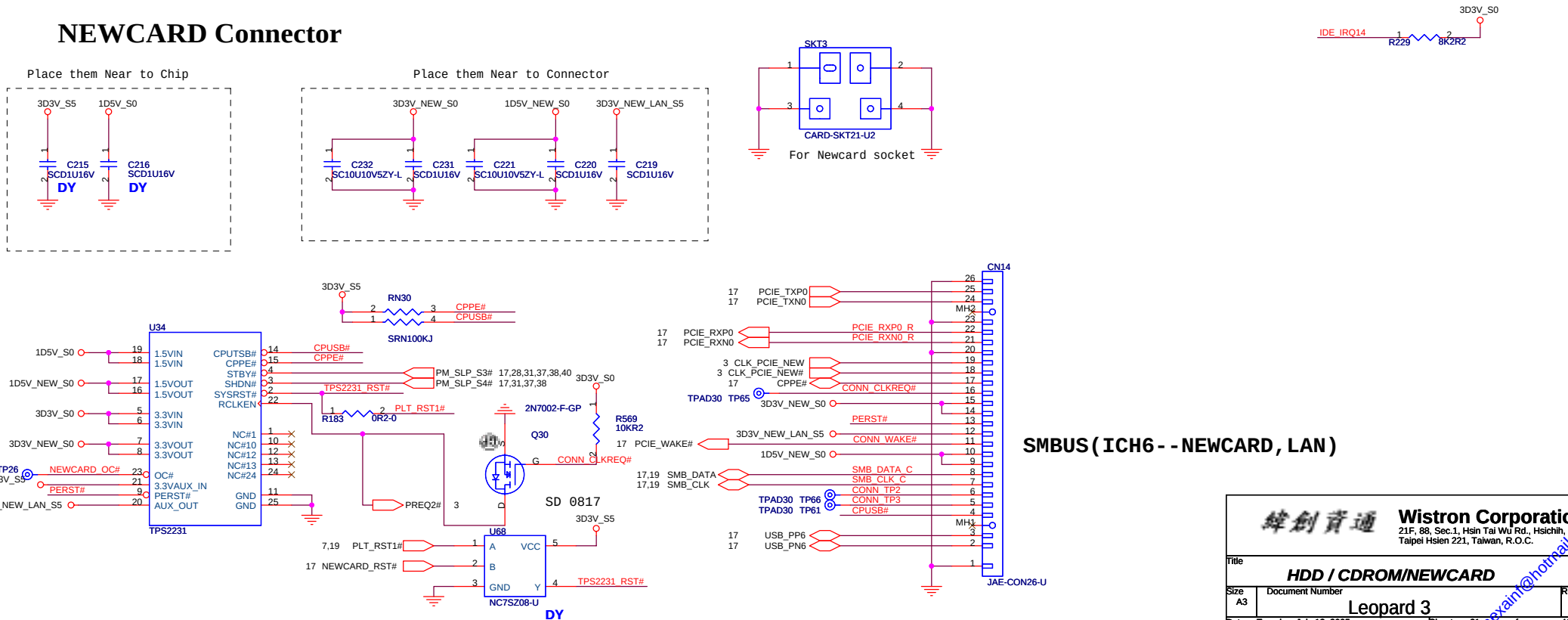
HDD Connector



CDROM



NEWCARD Connector



SMBUS(ICH6--NEWCARD,LAN)

華創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD / CDROM/NEWCARD***	
Size A3	Document Number: Leopard 3	Rev: -1
Date: Tuesday, July 12, 2005	Sheet 21 of 41	

INTA# CARBUS 1
INTB# NONE
INTC# 1394
INTD# CARD READER

1 of 4

U39A

PCI7411

CARD BUS

1394

SD/SDIO

UNUSED TERMINALS

Bypass/Decupoling Capacitors
Should be places as close to
PCI7421 as possible

* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible

SD
MS/MS_pro

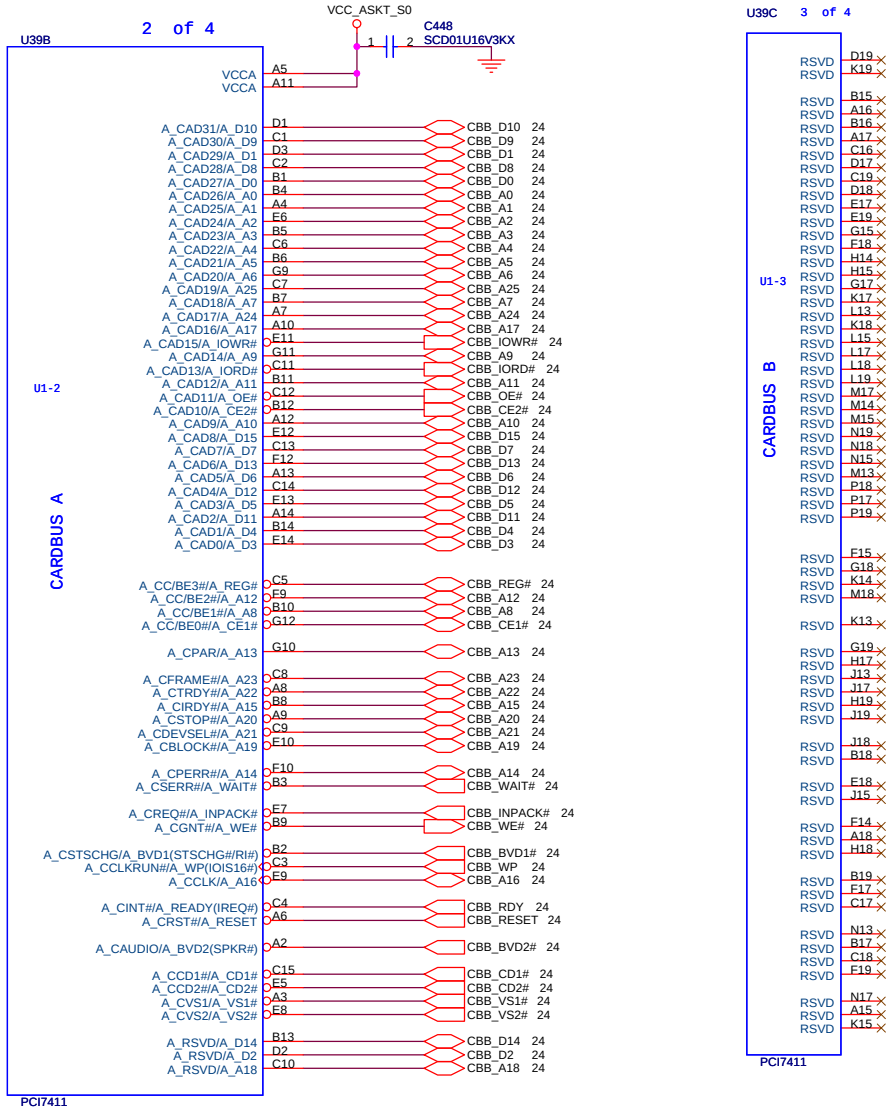
MS/MS_pro
XD

SM

7411:71.07411.00U
7421:71.07421.00U

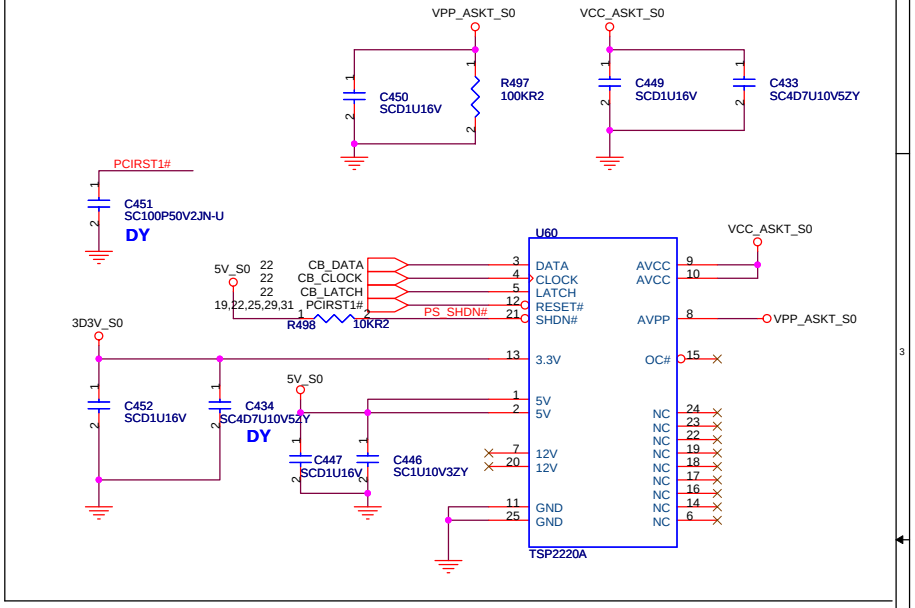
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

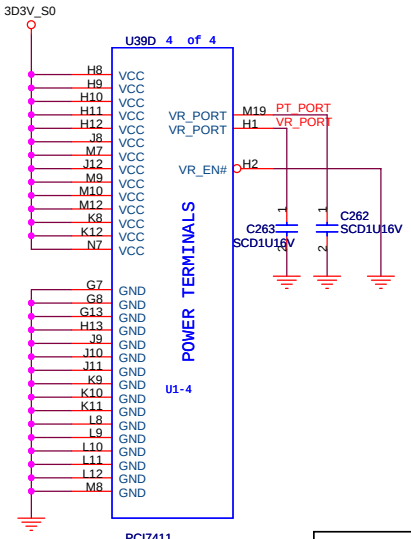
Title: TI SNC1Q21 (1 of 2)
Size: A3
Document Number: Leopard 3
Rev: -1
Date: Monday, August 15, 2005
Sheet 22 of 41



3D3V_S0
3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,25,27,29,30,31,32,36,38,40,41
3D3V_S0
5V_S0
13,14,18,19,20,21,24,27,28,29,32,36,39,40,41
5V_S0

Power switch





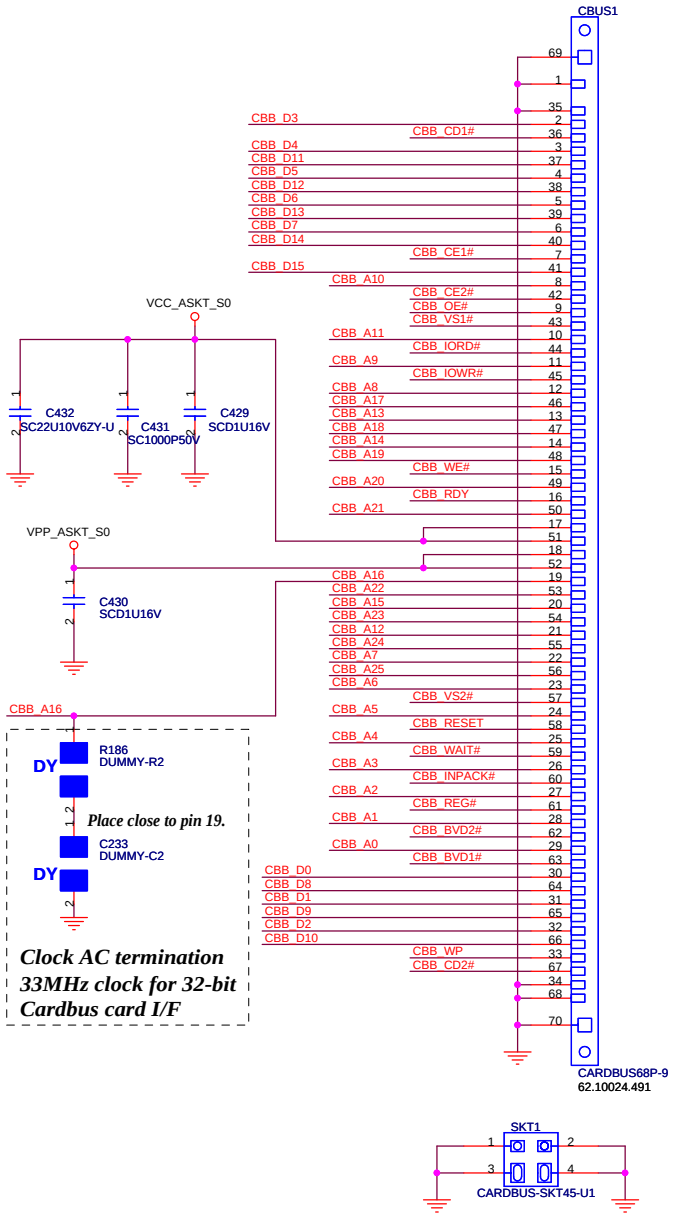
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TI PCI7411 GHK (2 of 2)

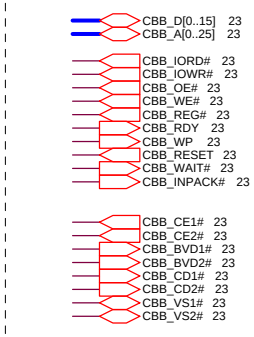
Size: A3 | Document Number: Leopard 3 | Rev: -1

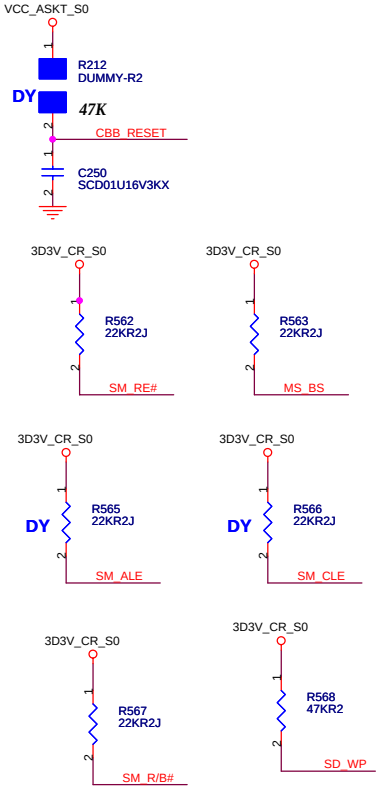
Date: Tuesday, July 12, 2005 | Sheet 23 of 41

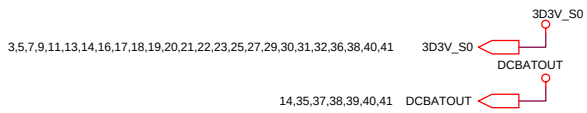
PCMCIA Socket



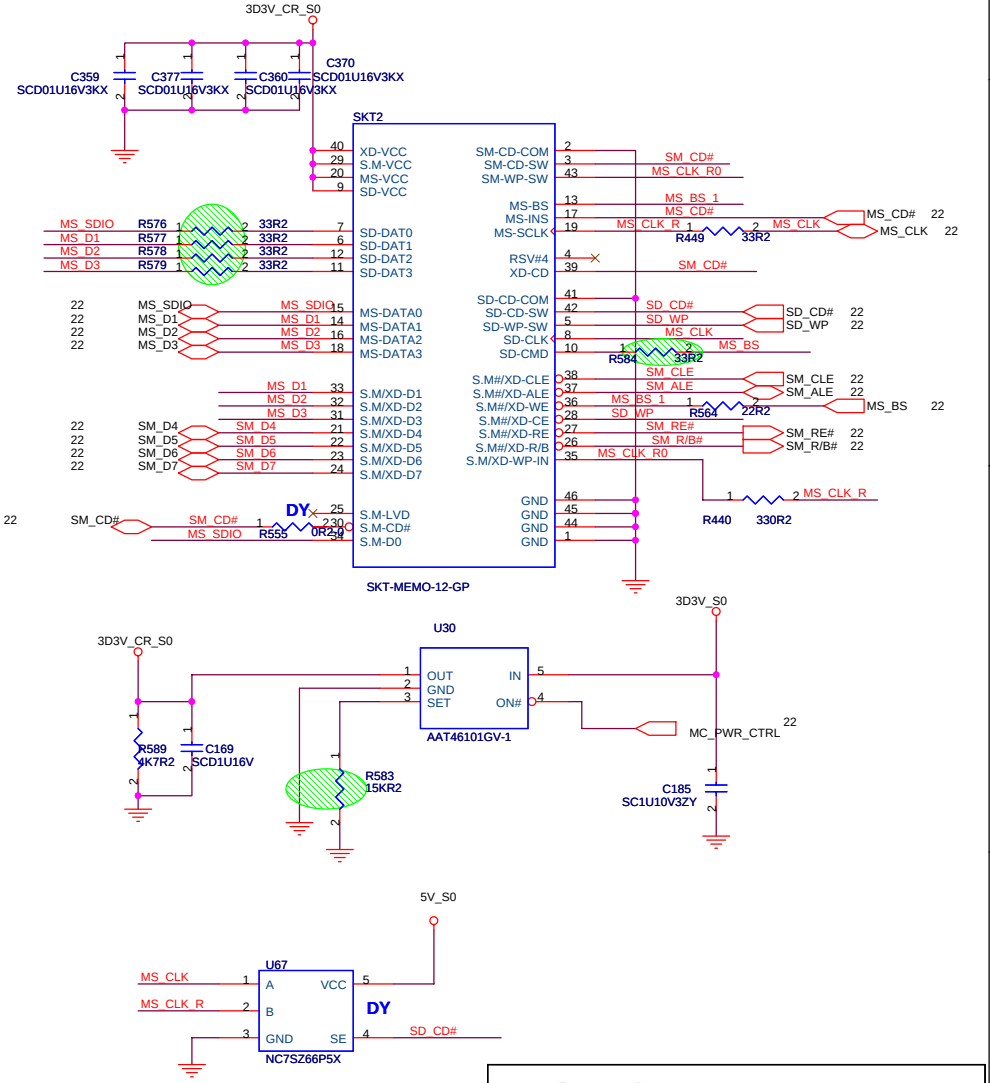
Cardbus I/F







6 in 1 Connector

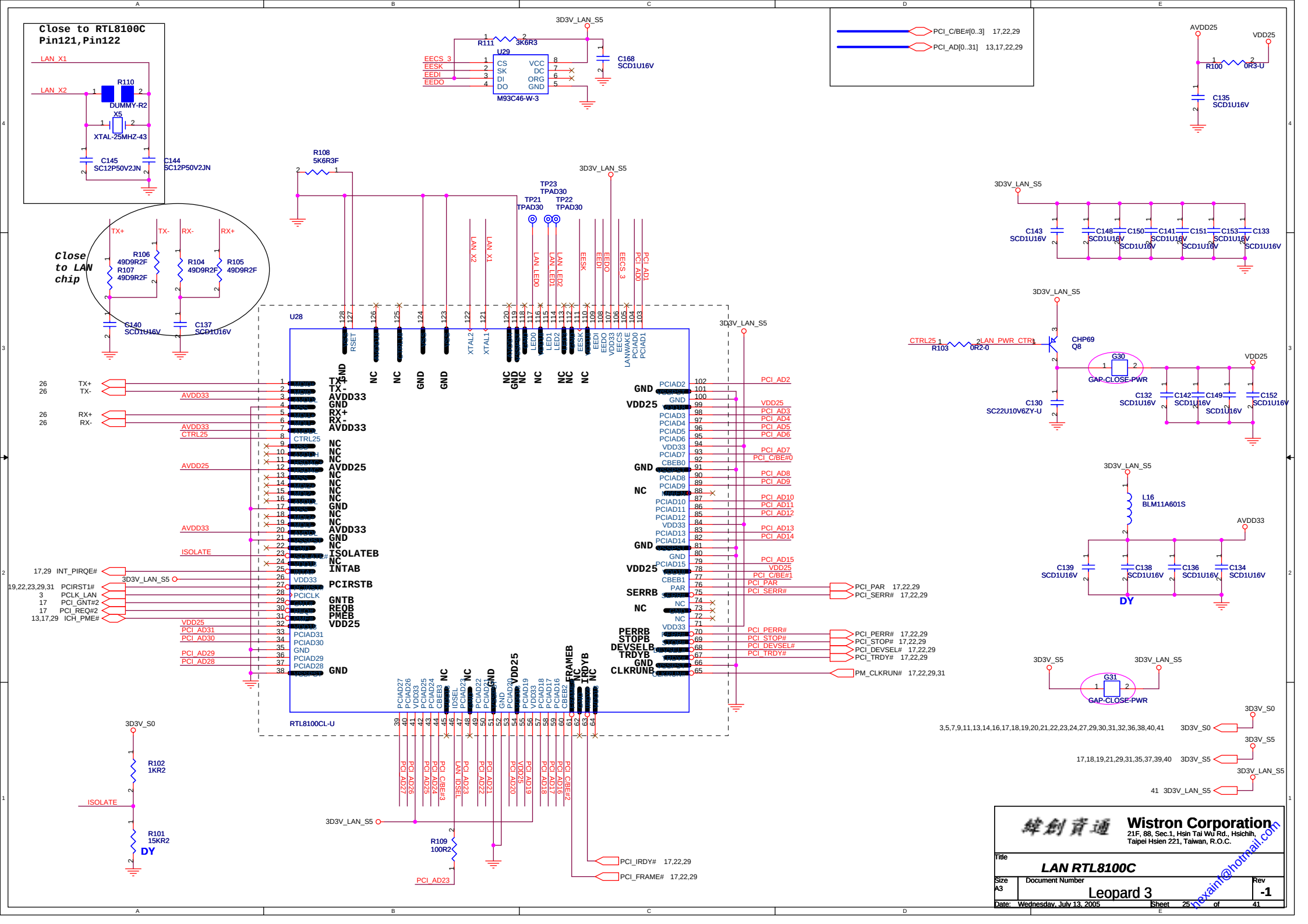


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA SLOT/ CARDBUS SKT

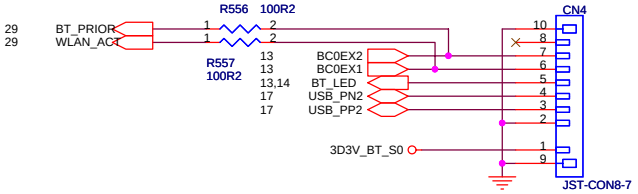
Size: A3 | Document Number: Leopard 3 | Rev: -1

Date: Tuesday, July 12, 2005 | Sheet 24 of 41


Close to RTL8100C Pin121,Pin122
LAN_X1
LAN_X2
R110
DUMMY-R2
X5
XTAL-25MHZ-43
C145 SC12P50V2JN
C144 SC12P50V2JN
Close to LAN chip
TX+
TX-
RX-
RX+
R106 49D9R2F
R107 49D9R2F
R104 49D9R2F
R105 49D9R2F
C140 SCD1U16V
C137 SCD1U16V
3D3V_LAN_S5
R111 3K6R3
U29
EECS_3
EESK
EEDI
EEDO
CS
SK
DI
DO
VCC
DC
ORG
GND
M93C46-W-3
C168 SCD1U16V
R108 5K6R3F
TP23 TPAD30
TP21 TPAD30
TP22 TPAD30
U28
RSET
XTAL2
XTAL1
LED0
LED1
LED2
EESK
EEDI
EEDO
VDD33
EECS
LANWAKE
PCIAD0
PCIAD1
TX+
TX-
AVDD33
GND
RX+
RX-
CTRL25
NC
AVDD25
ISOLATE
INTAB
PCIRSTB
GNTB
REQB
PMEB
PCIAD31
PCIAD30
PCIAD29
PCIAD28
PCICLK
PCIAD2
VDD25
PCIAD3
PCIAD4
PCIAD5
PCIAD6
PCIAD7
CBEB0
PCIAD8
PCIAD9
PCIAD10
PCIAD11
PCIAD12
PCIAD13
PCIAD14
PCIAD15
CBEB1
PAR
SERRB
PERRB
STOPB
DEVSELB
TRDYB
CLKRUNB
PCIAD27
PCIAD26
PCIAD25
PCIAD24
CBEB3
IDSEL
PCIAD23
PCIAD22
PCIAD21
PCIAD20
PCIAD19
PCIAD18
PCIAD17
PCIAD16
CBEB2
FRAMEB
IRDYB
RTL8100CL-U
PCI_C/BE#[0..3] 17,22,29
PCI_AD[0..31] 13,17,22,29
AVDD25
VDD25
R100 0R3-U
C135 SCD1U16V
C143 SCD1U16V
C148 SCD1U16V
C150 SCD1U16V
C141 SCD1U16V
C151 SCD1U16V
C153 SCD1U16V
C133 SCD1U16V
CTRL25
R103 0R2-0
LAN_PWR_CTRL
CHP69 Q8
G30 GAP-CLOSE-PWR
C130 SC22U10V6ZY-U
C132 SCD1U16V
C142 SCD1U16V
C149 SCD1U16V
C152 SCD1U16V
L16 BLM11A601S
C139 SCD1U16V
C138 SCD1U16V
C136 SCD1U16V
C134 SCD1U16V
DY
3D3V_S5
G31 GAP-CLOSE-PWR
3D3V_S0
R102 1KR2
R101 15KR2
R109 100R2
PCI_PAR 17,22,29
PCI_SERR# 17,22,29
PCI_PERR# 17,22,29
PCI_STOP# 17,22,29
PCI_DEVSEL# 17,22,29
PCI_TRDY# 17,22,29
PM_CLKRUN# 17,22,29,31
PCI_IRDY# 17,22,29
PCI_FRAME# 17,22,29
3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,27,29,30,31,32,36,38,40,41
17,18,19,21,29,31,35,37,39,40
41
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN RTL8100C
Size A3
Document Number
Leopard 3
Rev -1
Date: Wednesday, July 13, 2005
Sheet 25 of 41
nexaint@hotmail.com

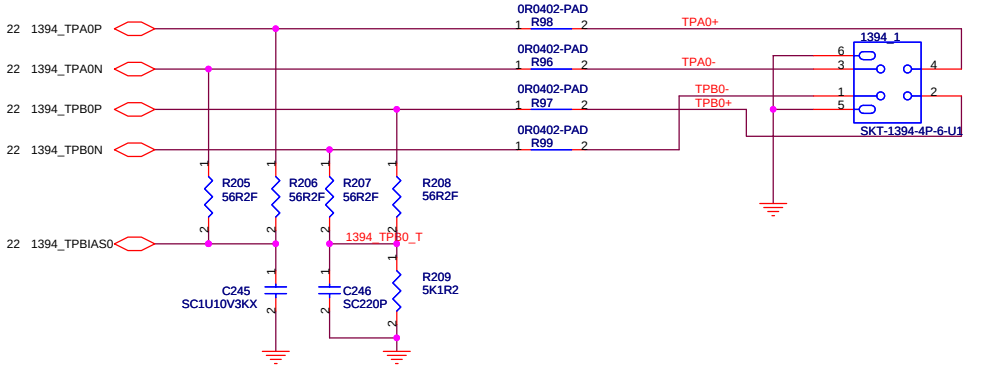
Blue thumb

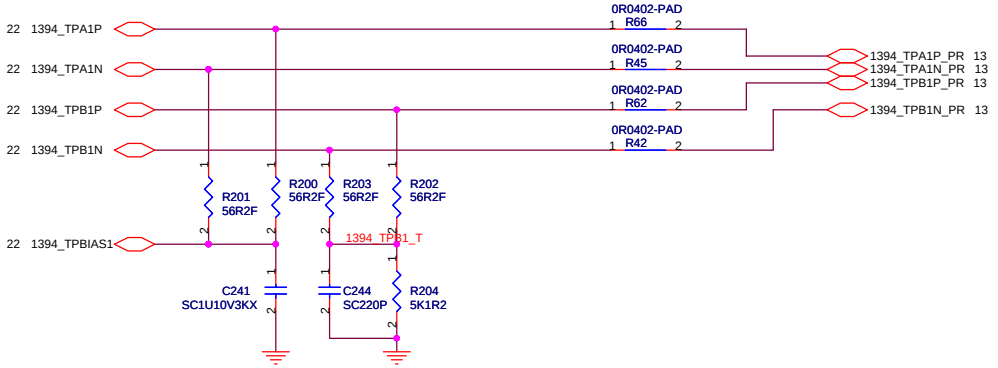
Place on bottom side



BC0EX2 connect to PCI_AD22 on main board.
BC0EX1 connect to ICH_PME# on main board.

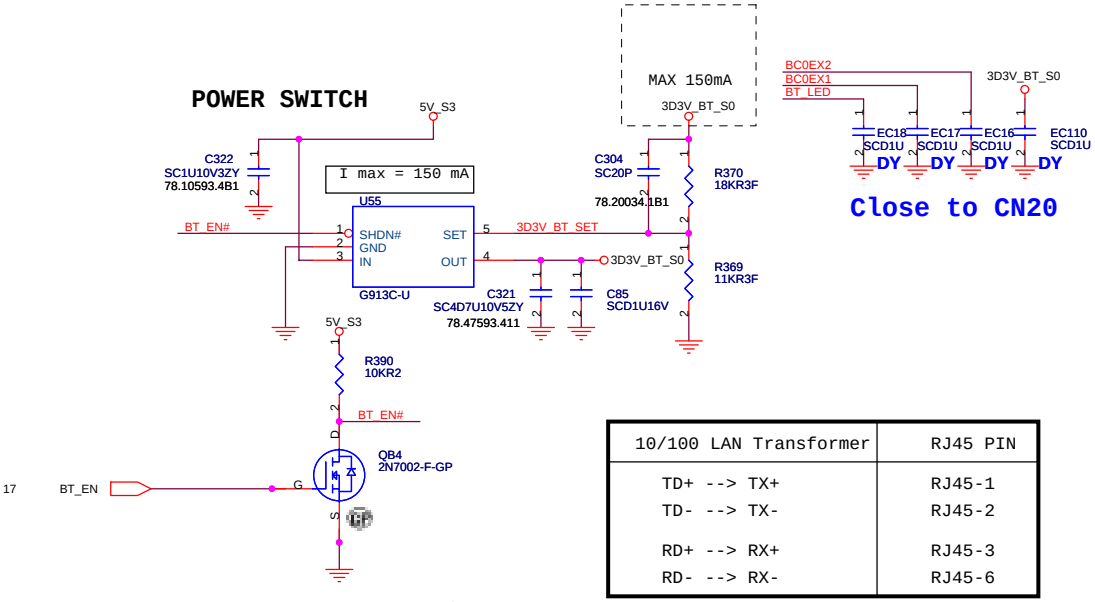
1394 Connector





These components near to chip side.

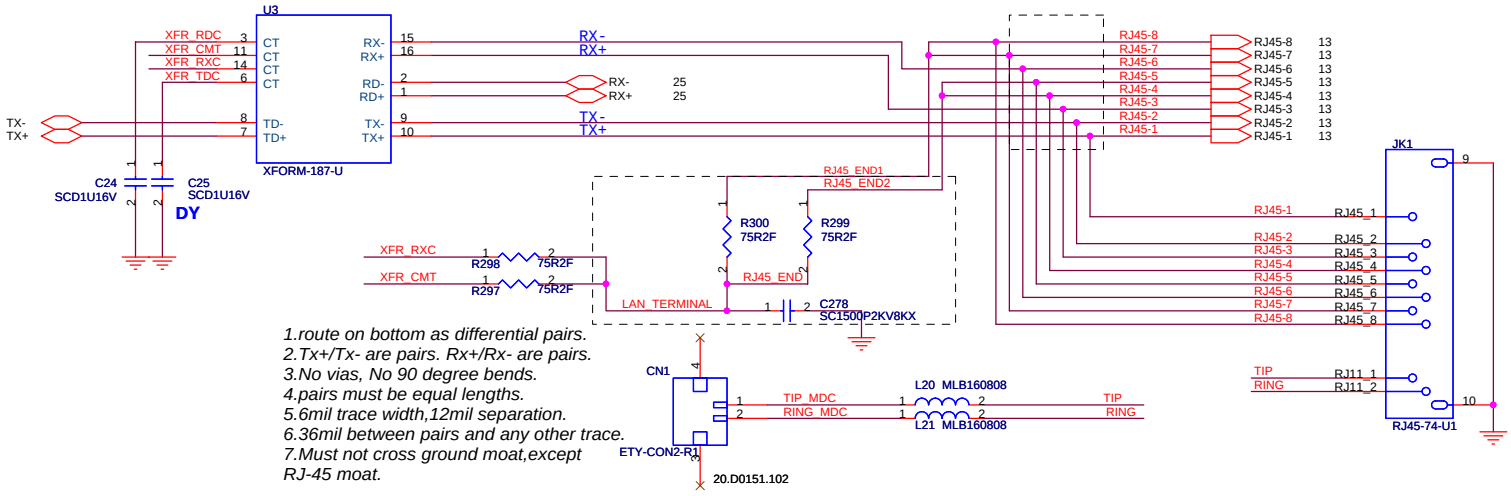
POWER SWITCH



Close to CN20

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN / 1394 Connector***

Size: A3 | Document Number: Leopard 3 | Rev: -1

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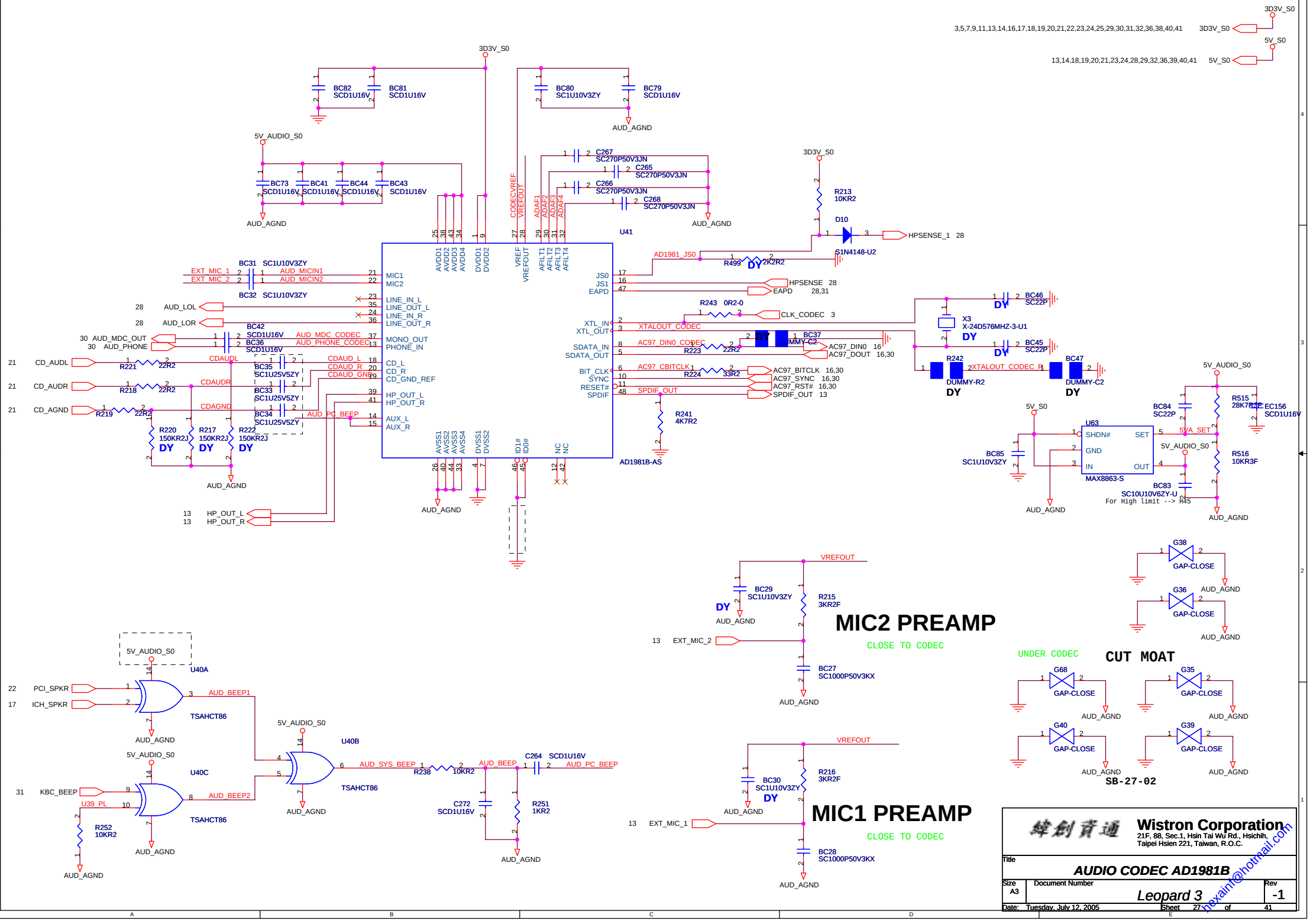
3D3V_S0
5V_S0
5V_AUDIO_S0
AUD_AGND
U41
AD1981B-AS
MIC2 PREAMP
CLOSE TO CODEC
MIC1 PREAMP
CLOSE TO CODEC
CUT MOAT
UNDER CODEC
SB-27-02
MAX8863-S
TSAHCT86
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC AD1981B
Leopard 3
Size A3
Rev -1
Date: Tuesday, July 12, 2005
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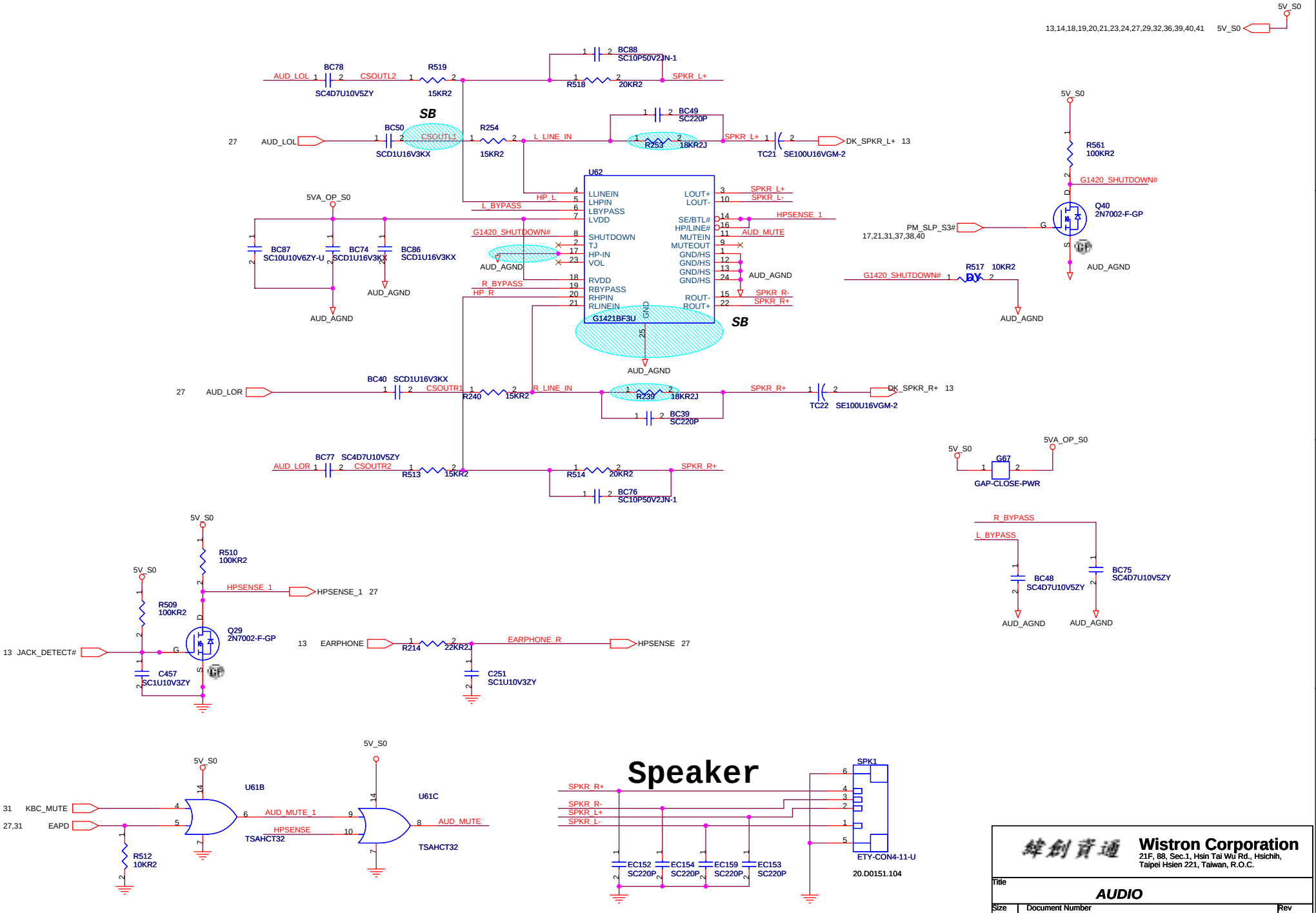
5V_S0
13,14,18,19,20,21,23,24,27,29,32,36,39,40,41
AUD_LOL
CSOUTL2
CSOUTL1
L_LINE_IN
SPKR_L+
SPKR_L-
DK_SPKR_L+
HP_L
L_BYPASS
R_BYPASS
HP_R
HPSENSE_1
AUD_MUTE
G1420_SHUTDOWN#
PM_SLP_S3#
17,21,31,37,38,40
R517 10KR2
AUD_LOR
CSOUTR1
CSOUTR2
R_LINE_IN
SPKR_R+
SPKR_R-
DK_SPKR_R+
5VA_OP_S0
AUD_AGND
U62
G1421BF3U
LLINEIN
LHPIN
LBYPASS
LVDD
SHUTDOWN
TJ
HP-IN
VOL
RVDD
RBYPASS
RHPIN
RLINEIN
LOUT+
LOUT-
SE/BTL#
HP/LINE#
MUTEIN
MUTEOUT
GND/HS
ROUT-
ROUT+
GND
SB
R561 100KR2
Q40 2N7002-F-GP
R510 100KR2
R509 100KR2
Q29 2N7002-F-GP
HPSENSE
JACK_DETECT#
EARPHONE
EARPHONE_R
R214 22KR2
C457 SC1U10V3ZY
C251 SC1U10V3ZY
G67
GAP-CLOSE-PWR
BC48 SC4D7U10V5ZY
BC75 SC4D7U10V5ZY
U61B
U61C
TSAHCT32
KBC_MUTE
EAPD
AUD_MUTE_1
R512 10KR2
Speaker
SPK1
ETY-CON4-11-U
EC152 SC220P
EC154 SC220P
EC159 SC220P
EC153 SC220P
20.D0151.104
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO
Size A3
Document Number
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Rev -1
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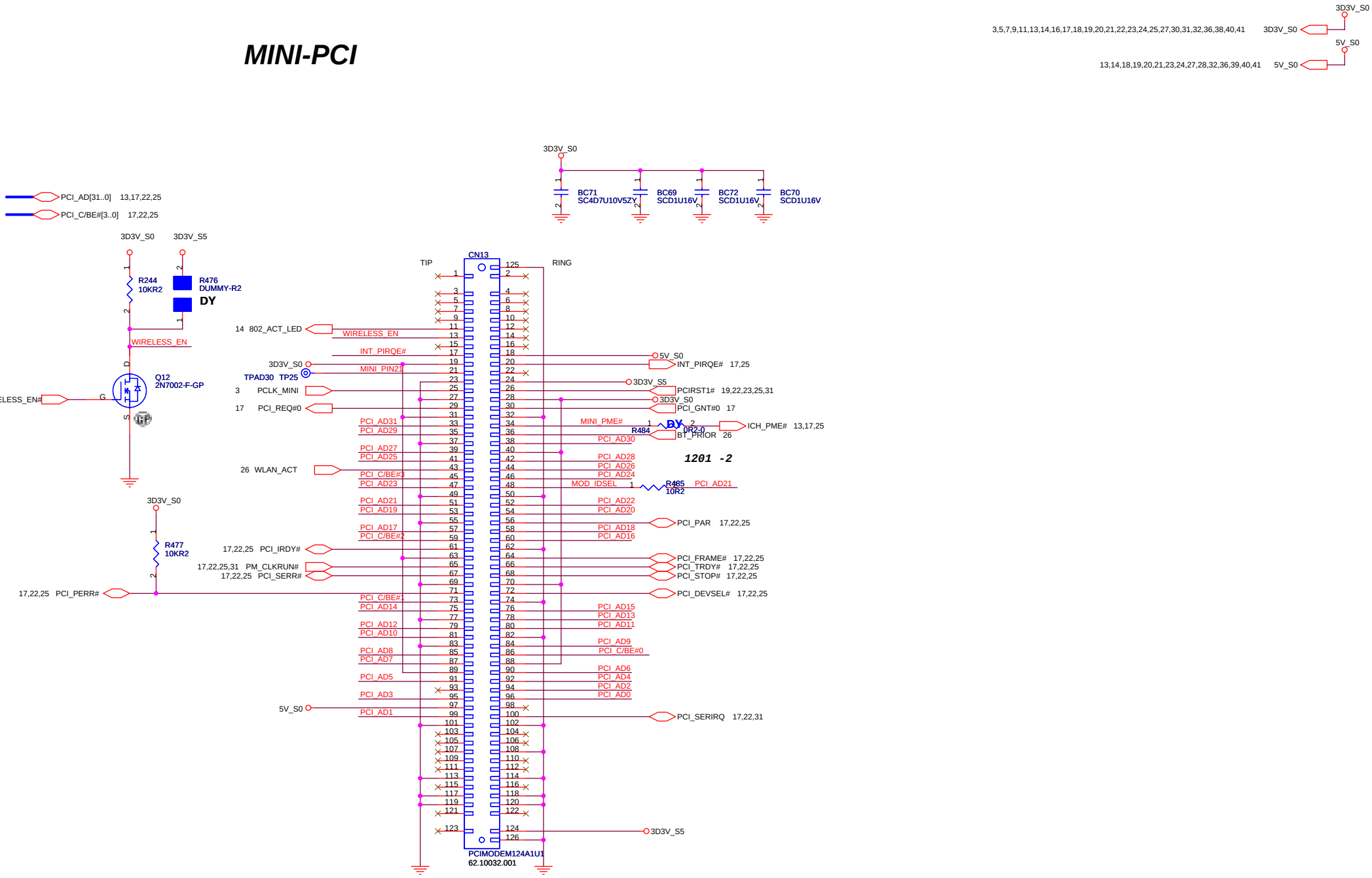
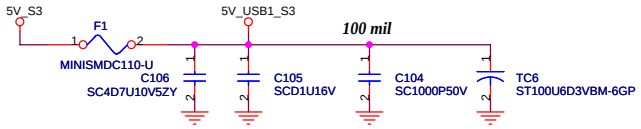
MINI-PCI

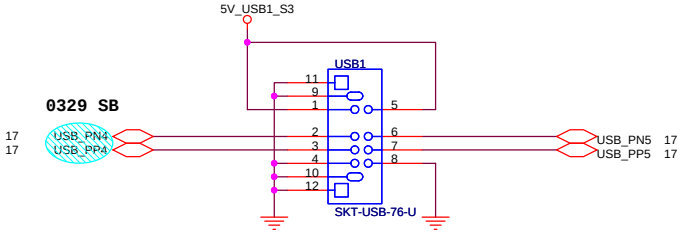


The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

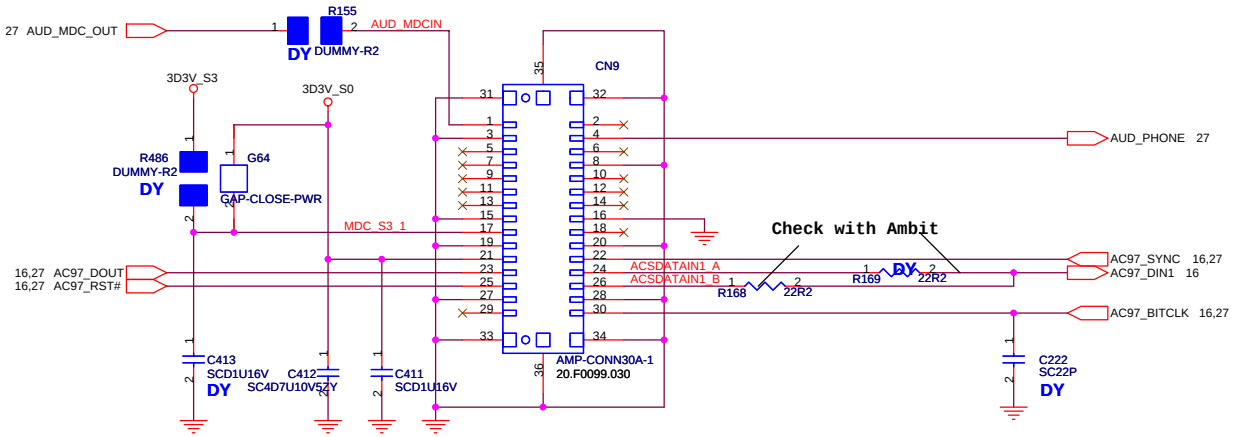
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI-PCI		
Size: A3	Document Number: Leopard 3	Rev: -1
Date: Tuesday, July 12, 2005	Sheet 29 of 41	

USB POWER

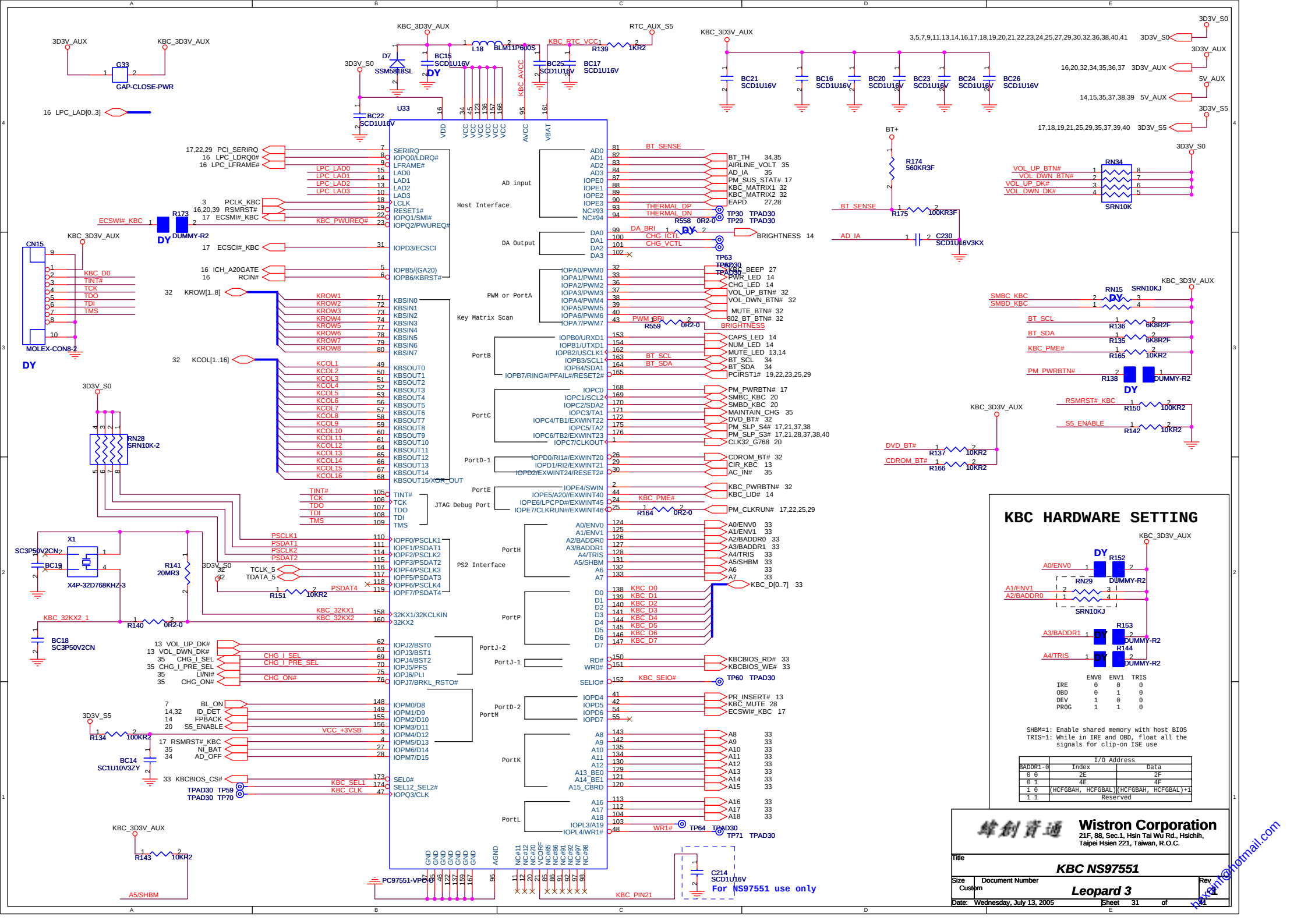




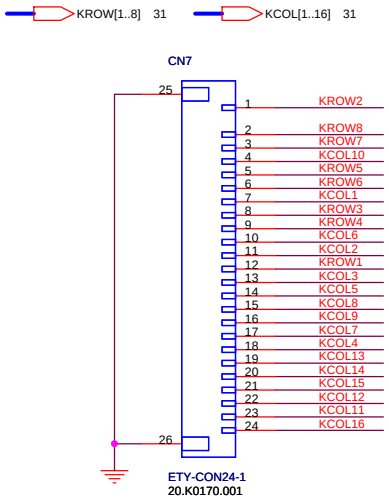
MDC Connector

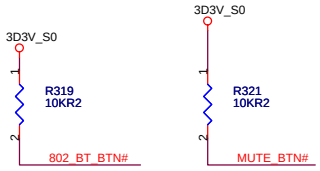


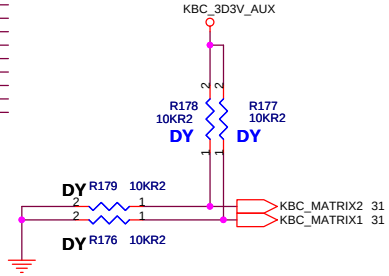
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *USB / MDC CONN.*		
Size: A3	Document Number: Leopard 3	Rev: -1
Date: Tuesday, July 12, 2005	Sheet 30 of 41	


KBC HARDWARE SETTING
KBC_3D3V_AUX
DY
A0/ENV0
A1/ENV1
A2/BADDR0
A3/BADDR1
A4/TRIS
RN29
SRN10KJ
R152
R153
R144
DUMMY-R2
ENV0 ENV1 TRIS
IRE 0 0 0
OBD 0 1 0
DEV 1 0 0
PROG 1 1 0
SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use
I/O Address
BADDR1-0 Index Data
0 0 2E 2F
0 1 4E 4F
1 0 (HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1
1 1 Reserved
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC NS97551
Size Custom
Document Number
Leopard 3
Rev 1
Date: Wednesday, July 13, 2005
Sheet 31 of 31
For NS97551 use only
U33
KBC_3D3V_AUX
3D3V_AUX
3D3V_S0
RTC_AUX_S5
BT_SENSE
BRIGHTNESS
PM_PWRBTN#
SMBC_KBC
SMBD_KBC
BT_SCL
BT_SDA
KBC_PME#
PM_CLKRUN#
KBC_D[0..7]
KBC_SEIO#
KBC_PWUREQ#
KBC_PIN21
MOLEX-CON8-2
SC3P50V2CN
X4P-32D768KHZ-3
PC97551-VPC0
SSM5818SL
SRN10K
SRN10KJ
DUMMY-R2

INTERNAL KEYBOARD CONNECTOR





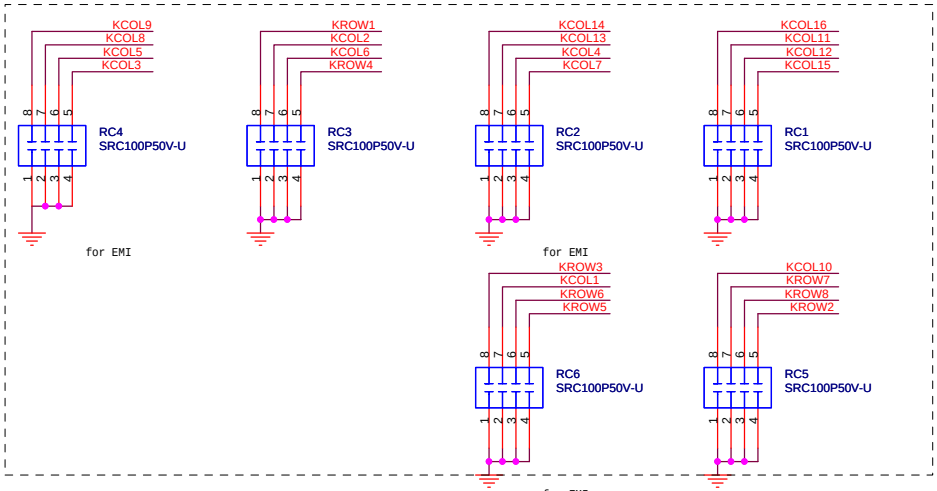


the matrix table for PCB

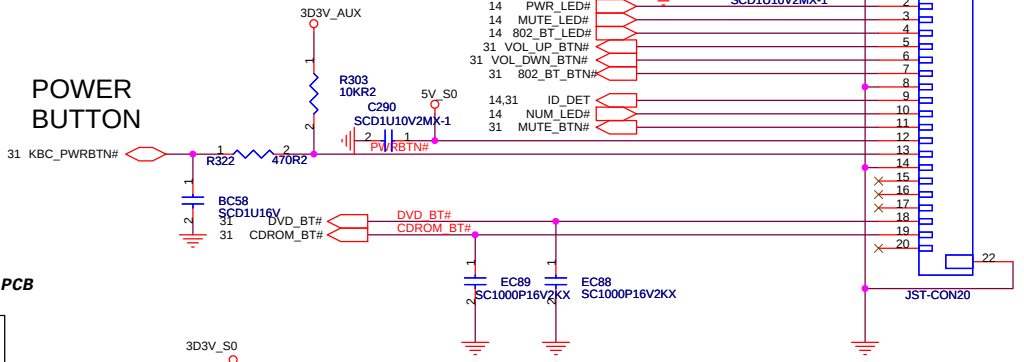
KBC_MATRIX2,KBC_MATRIX1

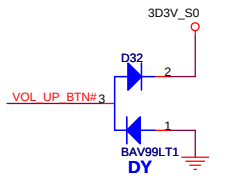
	PA	PR
FF	00	01
DF	10	11

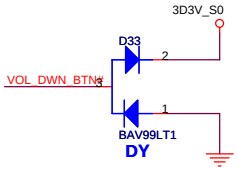
	NONE Quick Play	Quick Play
MATRIXID1#	0	1

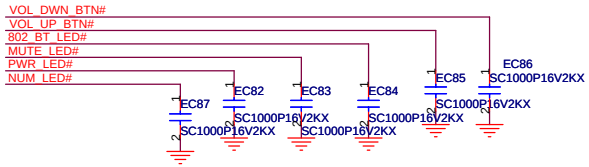


LAUNCH Board

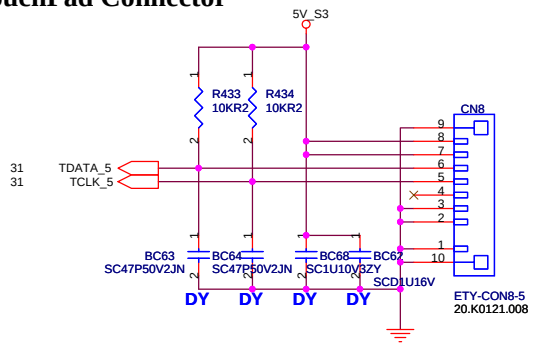








TouchPad Connector



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TOUCH PAD/Launch key

Size: A3 | Document Number: Leopard 3 | Rev: -1

Date: Tuesday, July 12, 2005 | Sheet 32 of 41

3D3V_S0

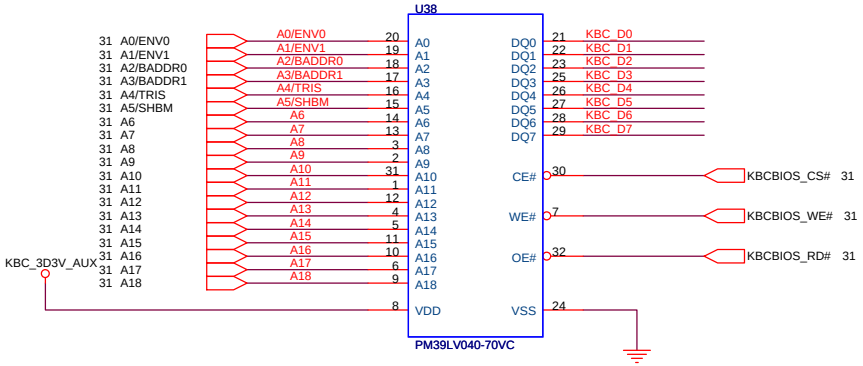
3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0

5V_S0

13,14,18,19,20,21,23,24,27,28,29,32,36,39,40,41 5V_S0

KBC_D[0..7] 31

512KB Flash



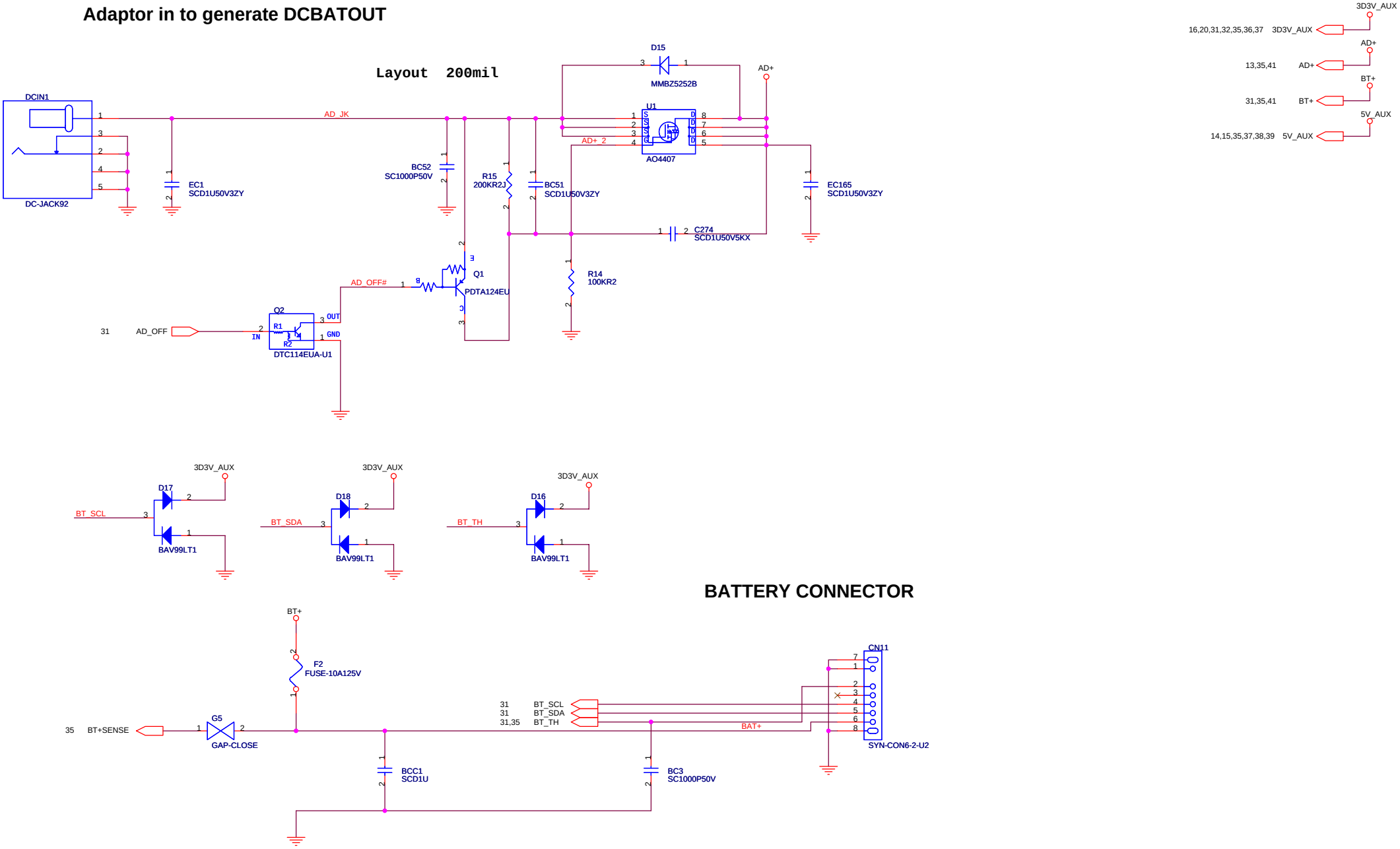
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS/GF

Size: A3 | Document Number: Leopard 3 | Rev: -1

Date: Tuesday, July 12, 2005 | Sheet 33 of 41

Adaptor in to generate DCBATOUT



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Adaptor/ Bettery conn.***

Size	Document Number	Rev
A3	Leopard 3	-1

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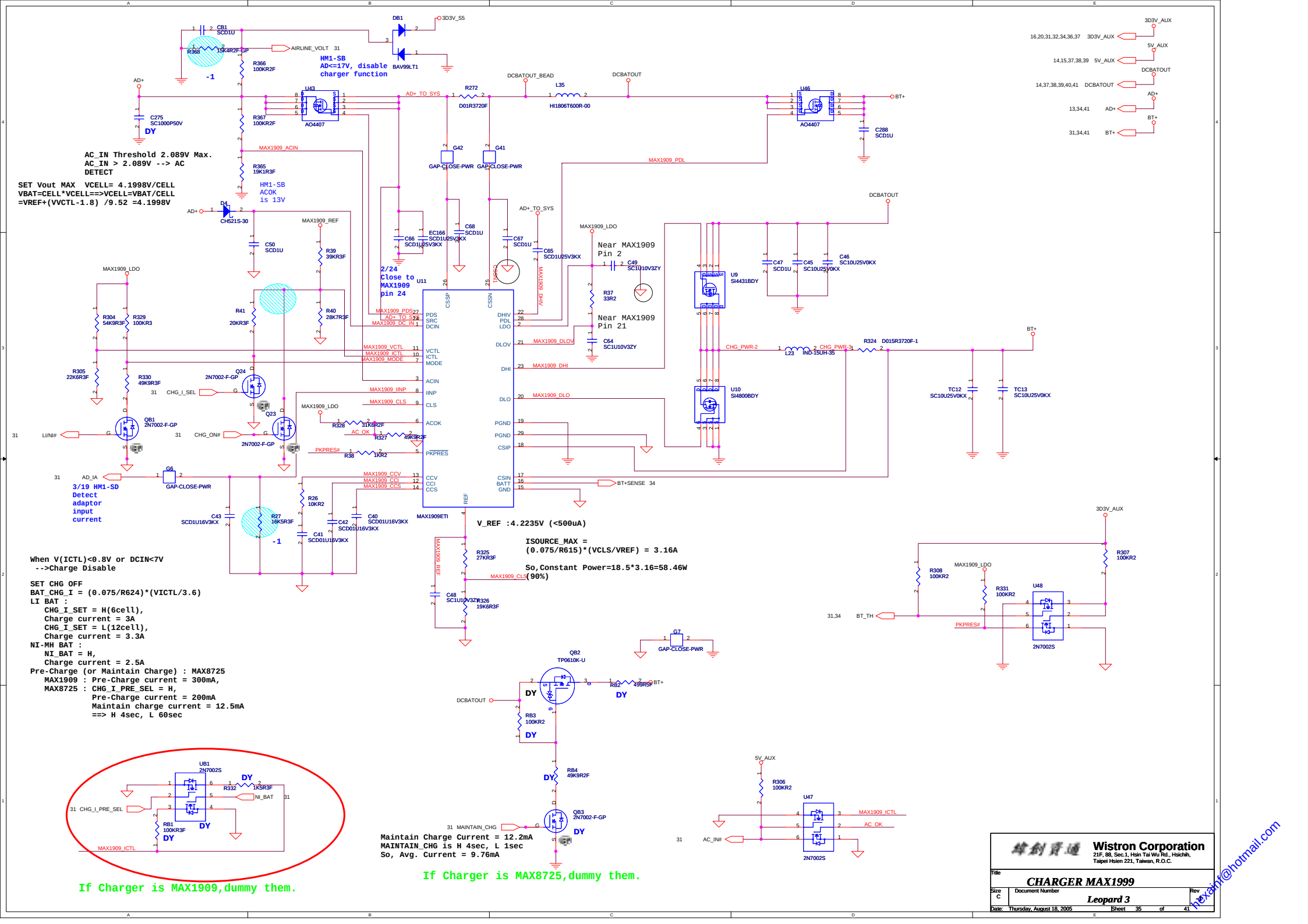
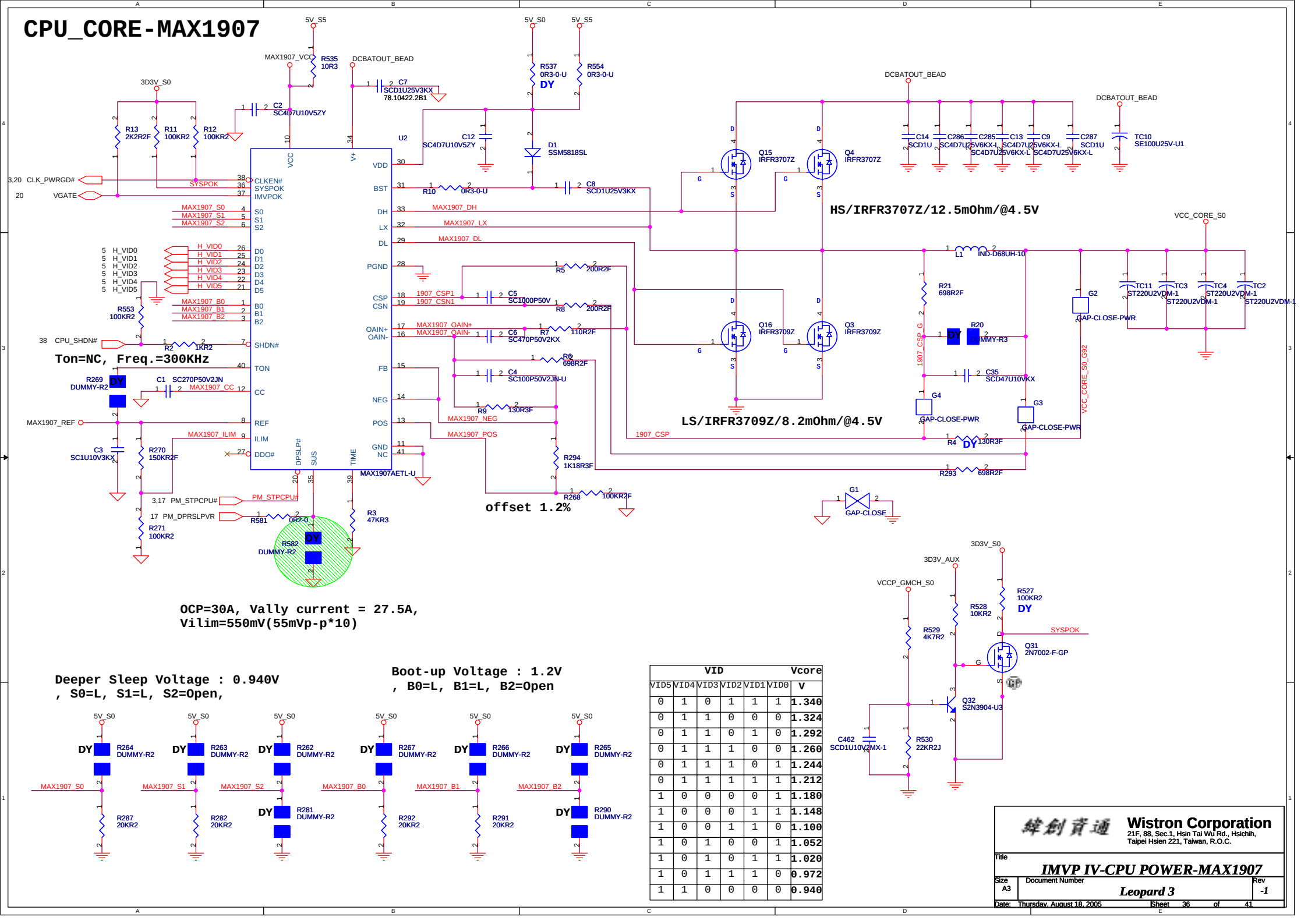

AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
HM1-SB AD<=17V, disable charger function
HM1-SB ACOK is 13V
2/24 Close to MAX1909 pin 24
Near MAX1909 Pin 2
Near MAX1909 Pin 21
3/19 HM1-SD Detect adaptor input current
V_REF :4.2235V (<500uA)
ISOURCE_MAX = (0.075/R615)*(VCLS/VREF) = 3.16A
So,Constant Power=18.5*3.16=58.46W (90%)
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
SET CHG OFF
BAT_CHG_I = (0.075/R624)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3A
CHG_I_SET = L(12cell),
Charge current = 3.3A
NI-MH BAT :
NI_BAT = H,
Charge current = 2.5A
Pre-Charge (or Maintain Charge) : MAX8725
MAX1909 : Pre-Charge current = 300mA,
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 200mA
Maintain charge current = 12.5mA
==> H 4sec, L 60sec
Maintain Charge Current = 12.2mA
MAINTAIN_CHG is H 4sec, L 1sec
So, Avg. Current = 9.76mA
If Charger is MAX1909,dummy them.
If Charger is MAX8725,dummy them.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX1999
Leopard 3
Thursday, August 18, 2005
Sheet 35 of 41
hexainf@hotmail.com

CPU_CORE-MAX1907



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

SYSTEM DC/DC 3D3V_S5 / 5V_S5

3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0 → 3D3V_S0
17,18,19,21,25,29,31,35,39,40 3D3V_S5 → 3D3V_S5
16,20,31,32,34,35,36 3D3V_AUX → 3D3V_AUX
14,18,20,36,38 5V_S5 → 5V_S5
14,15,35,38,39 5V_AUX → 5V_AUX
14,35,38,39,40,41 DCBATOUT → DCBATOUT

Sanyo / 6*7.7 / CV-AX

3V = 4Arms, OCP>6A

5V = 5Arms, OCP>6.8A

DCBATOUT
5V_AUX
MAX1999_VCC
3D3V_DC_S5
5V_DC_S3
MAX1999_V+
MAX1999_BST3
MAX1999_BST3R
MAX1999_BST5
MAX1999_BST5R
MAX1999_DH3
MAX1999_LX3
MAX1999_DL3
MAX1999_FB3
MAX1999_ON3
MAX1999_ON5
MAX1999_SHDN#
MAX1999_PRO#
MAX1999_ILIM
MAX1999_REF
MAX1999_LDO3
MAX1999_LDO5
MAX1999_SKIP#
MAX1999_DH5
MAX1999_LX5
MAX1999_DL5
MAX1999_FB5

R83 4D7R5
C80 SC1U25V5ZY
C81 SCD1U
R387 47R2
C319 SC1U10V3ZY
D21 BAW56-1
C121 SCD1U
C120 SC4D7U25V-U
U24 AO4422
C336 SCD1U50V5KX
R399 0R3-U
U54
R362 0R3-U
C303 SCD1U50V5KX
CLOSE TO CMOS
U16
C82 SC4D7U25V-U
C83 SC4D7U25V-U
C98 SCD1U
L30 IND-8UH-2
U25 AO4422
C96 SC47P50V2JN
R90 2MR3
Rds(on) = 24 mohm
TC19 ST220U4VDM-L3
C78 SC100P50V2JN-U
R80 6K98R3F
R82 10KR3F
U19
L28 IND-8UH-2
C79 SC47P50V2JN
R81 2MR3
R79 15K4R3
TC14 ST150U6D3VDM-9
C77 SC100P50V2JN-U
R78 10KR3F
R385 100KR2
R77 300KR3
R75 200KR3
These components should be located near by MAX1977
These components should be located near by MAX1977

20,38 1999_S5ENABLE → R393 1KR2
17,21,31,38 PM_SLP_S4# → R386 1KR2
D6 1SS400
D5 1SS400
DY
39 BL3#

Vref = 2V
C316 SCD22U10V3KX
3V_LDO=100mA
5V_LDO=100mA
MAX1999EEI
C320 SC1U10V3KX
C318 SC2D2U6D3V3MX-1
G44 GAP-CLOSE-PWR
G45 GAP-CLOSE-PWR
EC167 SCD1U25V3KX
5V_S3
R384 300KR2J
R76 300KR3
R74 150KR3
Q26 DTC115EE-U
17,21,28,31,38,40 PM_SLP_S3#
PM_SLP_S3# high = PWM
PM_SLP_S3# low = Ultrasonic
5V_S5 spec. = 10mA

ILIM5: 5V * 200K / (200K+300K) = 2.0V
200mV / 24 = 8.3A
OCP point = 8.3A +1/2Iripple

ILIM3: 5V * 200K / (200K+300K) = 2.0V
200mV / 24 = 8.3A
OCP point = 8.3A +1/2Iripple
OCP point = 20A +1/2Iripple

ILIM=Vcc 100mV*
ILIM=Vref 200mV*
OCP= 0.1Vth/Rds(on) + 0.5Iripple

SKIP# > 2.4V : PWM mode
SKIP# = GND(,0.8V) : SKIP MODE
SKIP# = REF (1.7V~2.3V)/FloatING
Ultrasonic MODE(25KHz min)

C317 DUMMY-C2
C331 DUMMY-C2
G21 GAP-CLOSE

華創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DC/DC 3V_S5/5V_S5		
Size A3	Document Number Leopard 3		Rev -1
Date: Monday, August 15, 2005	Sheet 37 of 41		

TI TPS5130 for 1D8V, 1.5V, 1.05V.

(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)

For 1.5V
SETTING=1.517V

PWM_1D5V
R413 680R2
C348 SC4700P50V3KX
R416 10KR3F
R410 7K87R2F
R409 3K9R2F
C349 SC4700P50V3KX
5130_INV1
5130_FB1

For 1.8V
SETTING=1.8V

PWM_1D8V
R411 680R2
C347 SC5600P25V2KX
R415 10K2R3F
R412 11K5R2F
R414 2KR2F
C350 SC3300P50V2KX
5130_INV2
5130_FB2

SB

For 1.05V
SETTING=1.061V

PWM_1D05V
R396 680R2
C333 SC5600P25V2KX
R398 80K6R3F
R395 20KR2F
R397 2K7R2J
C334 SC3300P50V2KX
5130_INV3
5130_FB3

OCP_1.05V

DCBATOUT
5130_TRIP1
R408 15KR3
C346 SCD1U16V3KX
close to IC

OCP_1.8V -1

DCBATOUT
5130_TRIP2
R407 15KR3
C345 SCD1U16V3KX
close to IC

OCP_1D5V

DCBATOUT
5130_TRIP3
R394 20KR3
C332 SCD1U16V3KX
close to IC

G28 GAP-CLOSE

5V_DC_S5
D24 BAW56-1

5130_LH1
C115 SCD1U50V5KX
5130_LL1
5130_LL1 39
5130_OUT1U
5130_OUT1D
5130_OUT1U 39
5130_OUT1D 39
5130_TRIP1
5130_TRIP2
DCBATOUT
5130_OUT2D
5130_OUT2D 39

5130_FLT
C116 SCD01U16V3KX
5130_FLT
5130_INV1

U23

INV1 FLT LH1 OUT1_LL1 OUT1_D OUTGND1 TRIP1 VIN_SENSE1.2 TRIP2 OUTGND2 OUT2_D

FB1
SS_STBY1
INV2
FB2
SS_STBY2
PWM_SEL
CT
GND
REF
STBY_VREF5
STBY_VREF3.3
STBY_LDO

LL2
OUT2_U
LH2
VIN
VREF3.3
VREF5
REG5V_IN
LDO_IN
LDO_CUR
LDO_GATE
LDO_OUT
INV_LDO

TPS5130

5130_FB1
5130_SS_STBY1
5130_INV2
5130_FB2
5130_SS_STBY2
5130_PWM_SEL
5130_CT
5130_REF
STBY_REF
R392 1KR3
20,37 1999_S5ENABLE

C114 SCD1U50V5KX
5130_LH2
5130_LL2
5130_LL2 39
close to IC
5130_OUT2U
5130_OUT2U 39
DCBATOUT
C344 SCD1U
5V_DC_S5
5V_S5
G52 GAP-CLOSE-PWR
R552 0R2-0
5V_S3
C463 SCD1U
C93 SC4D7U10V5ZY

SS_STBY3 FB3 INV3 PGOUT PG_DELAY TRIP3 VIN_SENSE3 LH3 OUT3_U LL3 OUT3_D OUTGND3

TPS5130PT-U

5130_SS_STBY3
5130_FB3
5130_INV3
5130_OUT3D
5130_LL3
5130_OUT3U
5130_OUT3D 39
5130_OUT3U 39
5130_LH3
C94 SCD1U50V5KX
5130_LL3 39
C95 SC1000P25V
D23
5V_DC_S5
BAT54-1
DCBATOUT
5130_TRIP3
3D3V_S0
R170 10KR2
U37A
20 VCCP_PWGD
PM_SLP_S3#
CPU_SHDN# 36
TSLCX08-U

HW Thermal Throttling

For 1.5V
SETTING=1.505V

5V_AUX
R360 100KR2
U51 2N7002S
PM_SLP_S3#
5130_SS_STBY1
C119 SC1500P50V3KX

5V_AUX
R359 100KR2
U50 2N7002S
17,21,31,37 PM_SLP_S4#
5130_SS_STBY2
C118 SC4700P50V3KX

5130_CT
C117 SC47P50V2JN

5130_REF
C97 SCD1U16V3KX

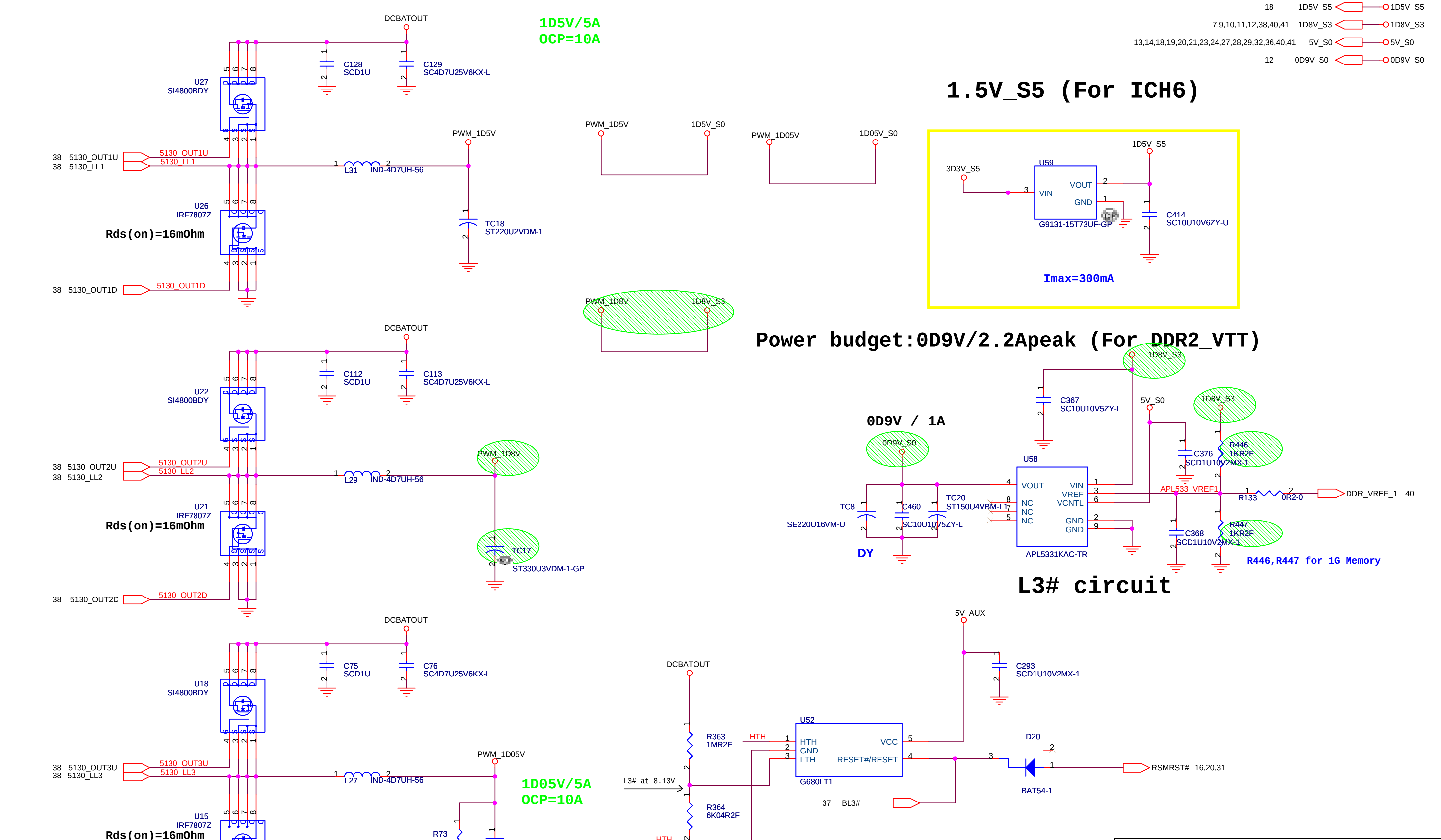
5V_AUX
R361 100KR2
U53 2N7002S
PM_SLP_S3#
5130_SS_STBY3
C335 SC1500P50V3KX

5V_AUX
R383 300KR2J
5130_PWM_SEL
17,21,28,31,37,40 PM_SLP_S3#
Q25
R1
R2
IN
OUT
GND
DTC115EE-U

華創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***DC/DC 2D5V/1D5V/1D05V***		
Size A3	Document Number ***Leopard 3***		Rev ***-1***
Date: Monday, August 15, 2005		Sheet 38 of 41	

TI TPS5130 for 2.5V, 1.5V, 1.05V

(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)

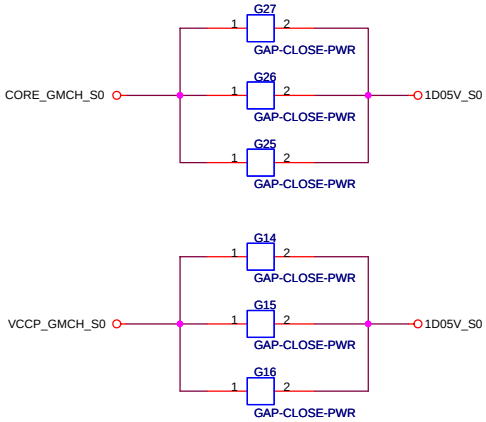


14,35,37,38,40,41 DCBATOUT
DCBATOUT
17,18,19,21,25,29,31,35,37,40 3D3V_S5
3D3V_S5
14,15,35,37,38 5V_AUX
5V_AUX
18 1D5V_S5
1D5V_S5
7,9,10,11,12,38,40,41 1D8V_S3
1D8V_S3
13,14,18,19,20,21,23,24,27,28,29,32,36,40,41 5V_S0
5V_S0
12 0D9V_S0
0D9V_S0
1D5V/5A
OCP=10A
DCBATOUT
C128
SCD1U
C129
SC4D7U25V6KX-L
U27
SI4800BDY
38 5130_OUT1U
38 5130_LL1
5130_OUT1U
5130_LL1
L31
IND-4D7UH-56
PWM_1D5V
U26
IRF7807Z
Rds(on)=16mOhm
TC18
ST220U2VDM-1
38 5130_OUT1D
5130_OUT1D
PWM_1D5V
1D5V_S0
PWM_1D05V
1D05V_S0
1.5V_S5 (For ICH6)
3D3V_S5
1D5V_S5
U59
VIN
VOUT
GND
G9131-15T73UF-GP
C414
SC10U10V6ZY-U
Imax=300mA
PWM_1D8V
1D8V_S3
Power budget:0D9V/2.2Apeak (For DDR2_VTT)
DCBATOUT
C112
SCD1U
C113
SC4D7U25V6KX-L
U22
SI4800BDY
38 5130_OUT2U
38 5130_LL2
5130_OUT2U
5130_LL2
L29
IND-4D7UH-56
PWM_1D8V
U21
IRF7807Z
Rds(on)=16mOhm
TC17
ST330U3VDM-1-GP
38 5130_OUT2D
5130_OUT2D
1D8V_S3
C367
SC10U10V5ZY-L
5V_S0
1D8V_S3
0D9V / 1A
0D9V_S0
U58
VOUT
NC
NC
NC
VIN
VREF
VCNTL
GND
GND
APL5331KAC-TR
TC8
SE220U16VM-U
C460
SC10U10V5ZY-L
TC20
ST150U4VBM-L1
DY
C376
SCD1U10V2MX-1
R446
1KR2F
APL533_VREF1
R133
0R2-0
DDR_VREF_1 40
C368
SCD1U10V2MX-1
R447
1KR2F
R446,R447 for 1G Memory
L3# circuit
DCBATOUT
C75
SCD1U
C76
SC4D7U25V6KX-L
U18
SI4800BDY
38 5130_OUT3U
38 5130_LL3
5130_OUT3U
5130_LL3
L27
IND-4D7UH-56
PWM_1D05V
1D05V/5A
OCP=10A
U15
IRF7807Z
Rds(on)=16mOhm
R73
1KR2
DY
TC5
ST220U4VDM-10
38 5130_OUT3D
5130_OUT3D
DCBATOUT
R363
1MR2F
HTH
L3# at 8.13V
R364
6K04R2F
HTH
R323
174KR2F
U52
HTH
GND
LTH
VCC
RESET#/RESET
G680LT1
37 BL3#
5V_AUX
C293
SCD1U10V2MX-1
D20
BAT54-1
RSMRST# 16,20,31

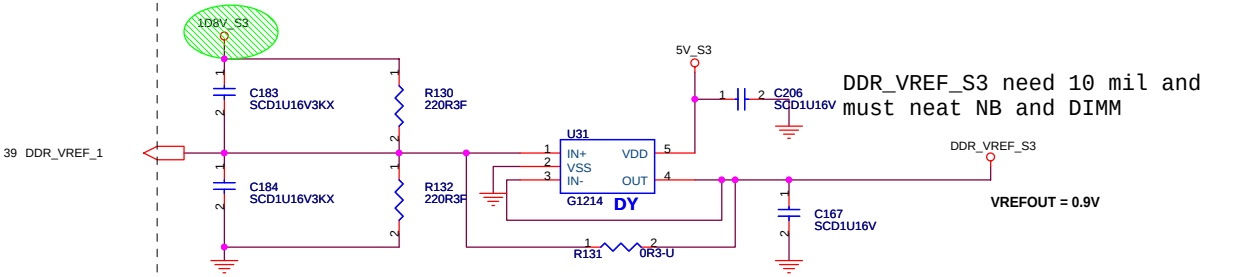
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	39.DC/DC 1D8V/1D5V/1D05V_2	
Size A3	Document Number: Leopard 3	Rev -1
Date: Thursday, August 18, 2005	Sheet 39 of 41	

FOR GMCH Power



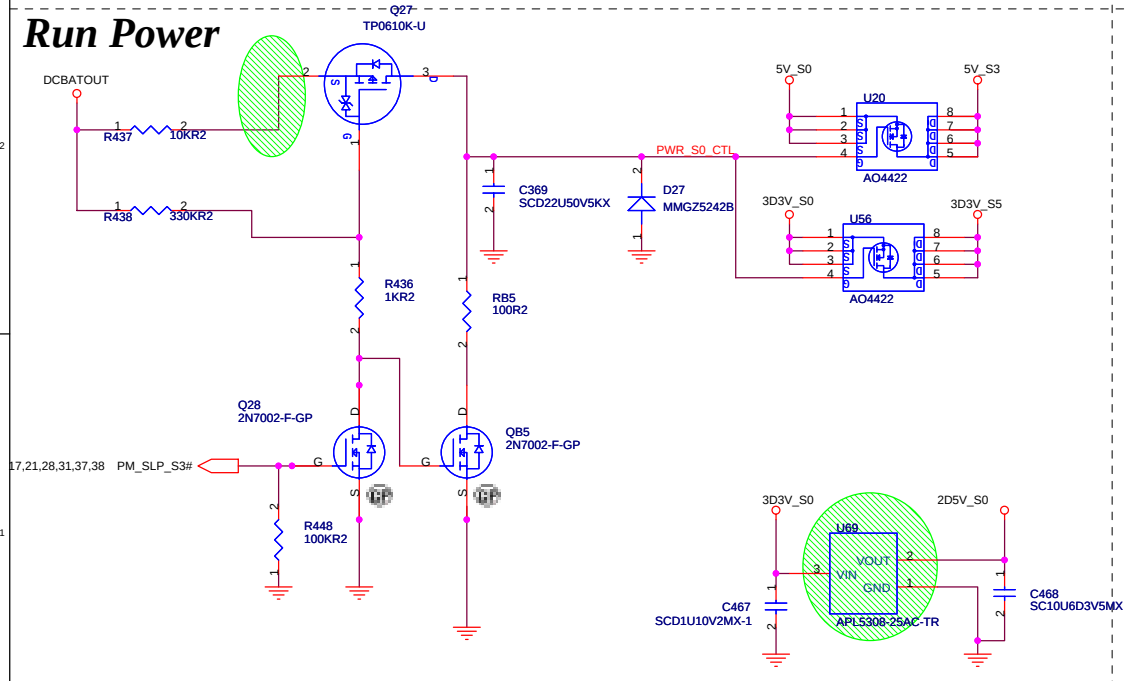
3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,41 3D3V_S0 — 3D3V_S0
13,14,30 3D3V_S3 — 3D3V_S3
17,18,19,21,25,29,31,35,37,39 3D3V_S5 — 3D3V_S5
13,14,18,19,20,21,23,24,27,28,29,32,36,39,41 5V_S0 — 5V_S0
13,14,26,28,30,32,37,38,41 5V_S3 — 5V_S3
14,18,20,36,38 5V_S5 — 5V_S5
7,9,15,18 2D5V_S0 — 2D5V_S0
7,9,10,11,12,38,39,41 1D8V_S3 — 1D8V_S3
7,11 DDR_VREF_S3 — DDR_VREF_S3
14,35,37,38,39,41 DCBATOUT — DCBATOUT
38,39,41 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,16,18,36,41 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,41 CORE_GMCH_S0 — CORE_GMCH_S0



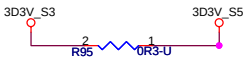
DDR_VREF_S3 need 10 mil and must neat NB and DIMM

FOR DDR 2 Power

Run Power



Suspend Power



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Title: PWRPLANE&RESETLOGIC		
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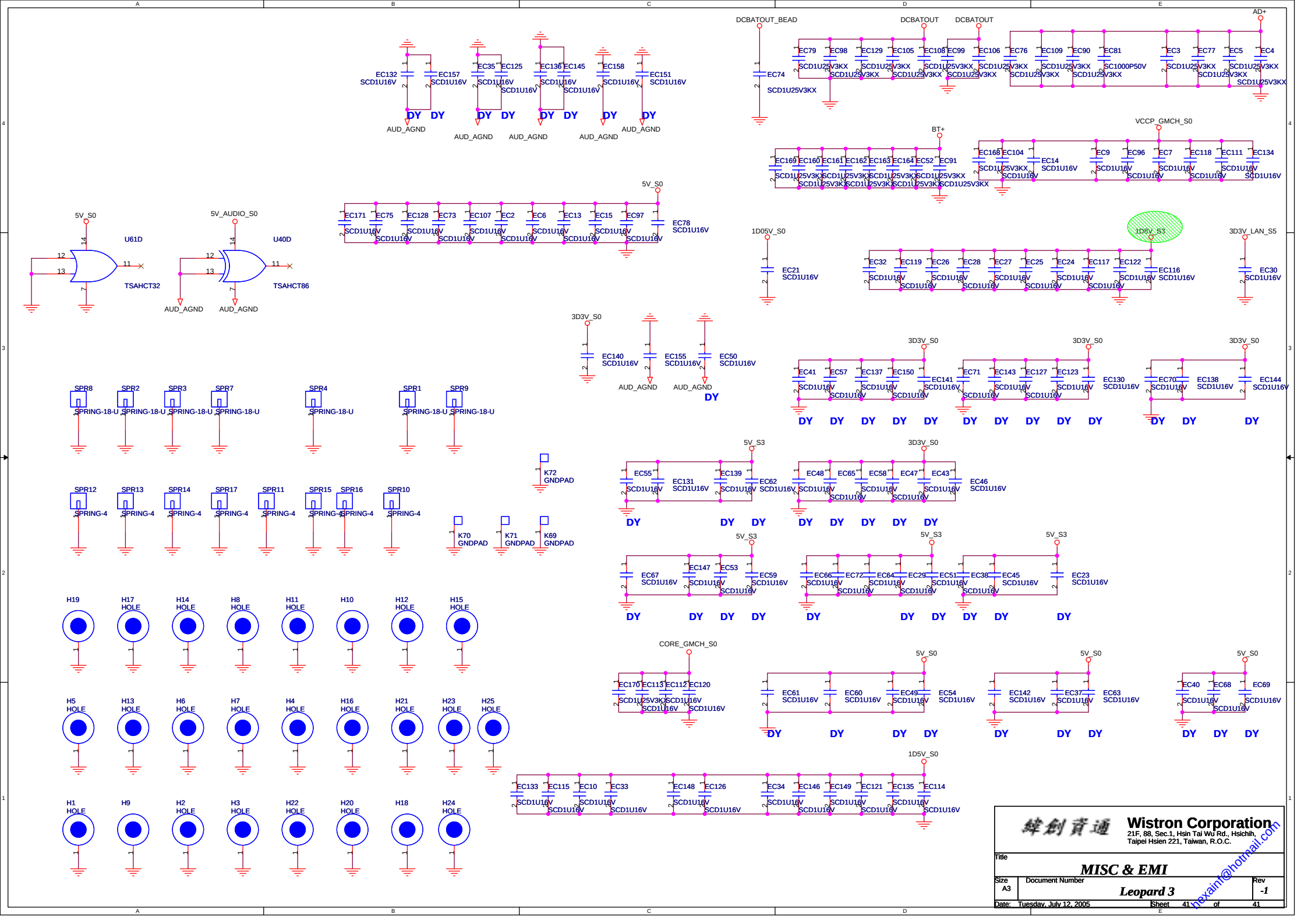
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DCBATOUT
DCBATOUT
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EC79
EC98
EC129
EC105
EC108
EC99
EC106
EC76
EC109
EC90
EC81
EC3
EC77
EC5
EC4
SCD1U25V3KX
SC1000P50V
BT+
VCCP_GMCH_S0
EC169
EC160
EC161
EC162
EC163
EC164
EC52
EC91
EC168
EC104
EC14
EC9
EC96
EC7
EC118
EC111
EC134
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5V_S0
EC171
EC75
EC128
EC73
EC107
EC2
EC6
EC13
EC15
EC97
EC78
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U61D
U40D
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EC21
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3D3V_LAN_S5
EC30
3D3V_S0
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HOLE
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