Compal confidential

Schematics Document
Mobile Merom uFCPGA with Satna Rosa Platform

2007-01-08
REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.		
Title: *Cover Sheet*		
Size: Custom	Document Number: *LA-3732P*	Rev: 0.2
Date: Wednesday, March 14, 2007	Sheet 1 of 40	

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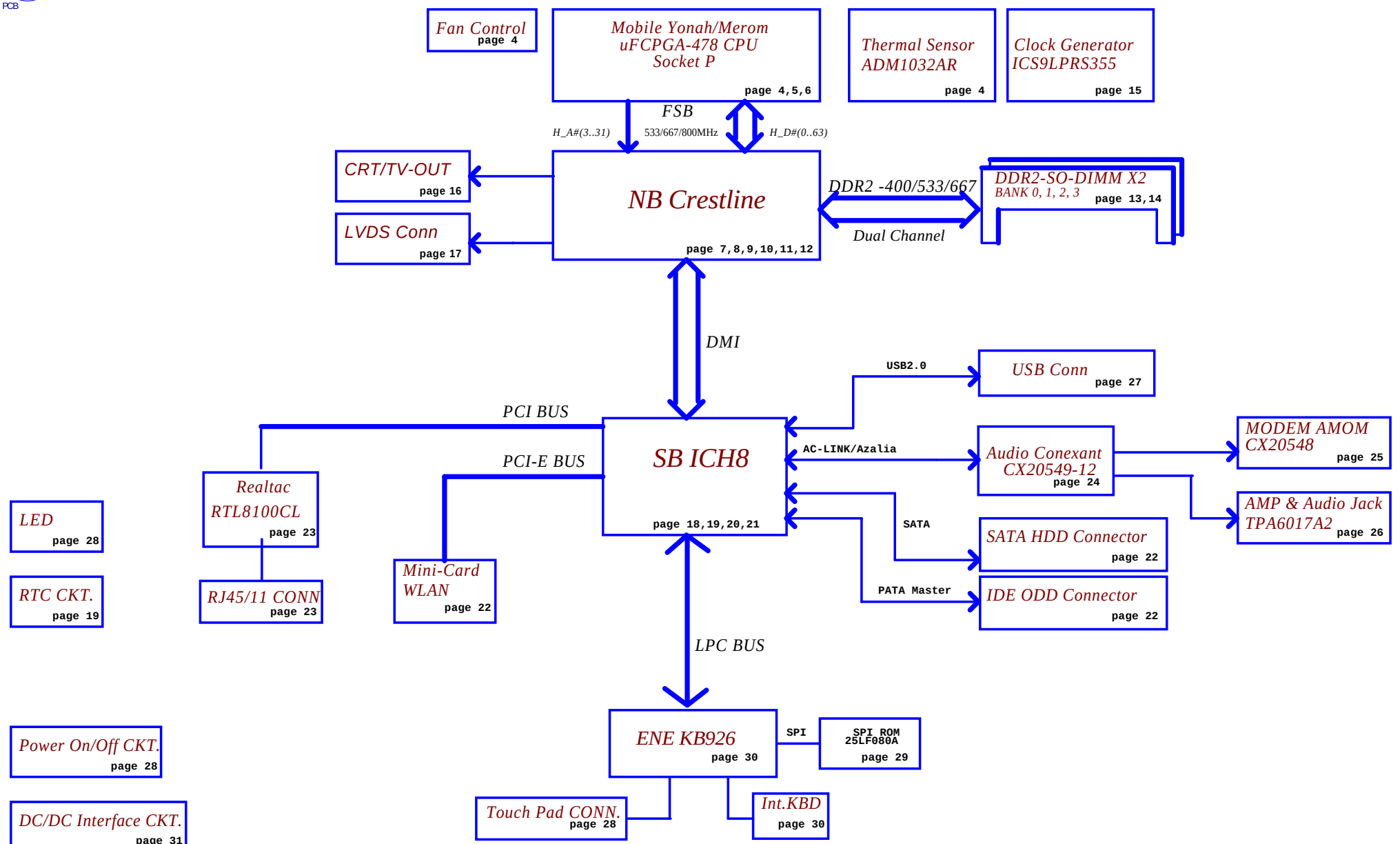
File Name : LA-3732P

Spartan 1.0 (Merom +Crestline+ICH8)

ZZZ1

PCB



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Block Diagram

Size: Custom | Document Number: LA-3732P | Rev: 0.2

Date: Wednesday, March 14, 2007 | Sheet 2 of 40

Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD22	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43XXXXXX

Jump-Short: PJP?

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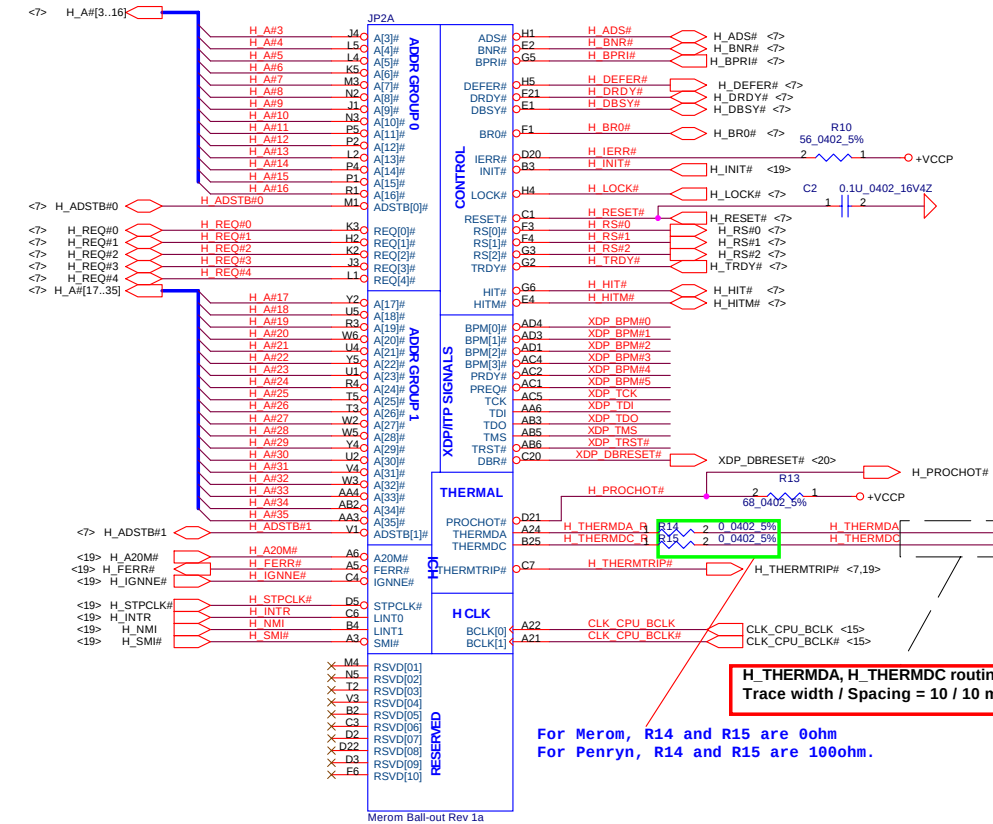
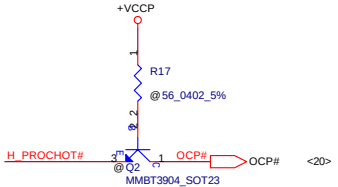
Title: *Notes List*

Size | Document Number: *LA-3732P* | Rev: 0.2

Date: Wednesday, March 14, 2007 | Sheet 3 of 40



SP07000FP00 S SOCKET TYCO 2-1871873-2 478P H3 CPU
SP07000FD00 S SOCKET FOXCONN PZ4782A-274M-41 478P H3

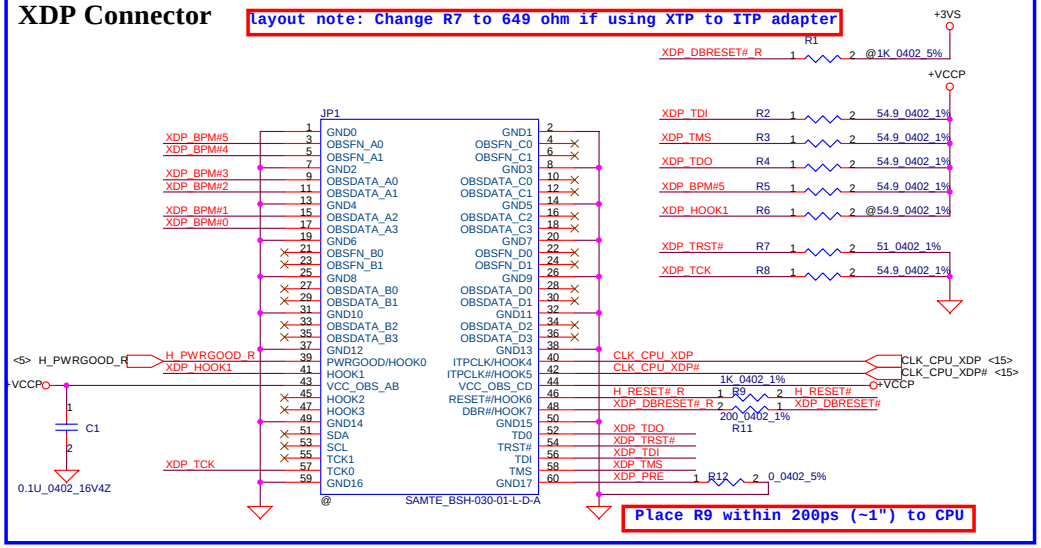


For Merom, R14 and R15 are 0ohm
For Penryn, R14 and R15 are 100ohm.

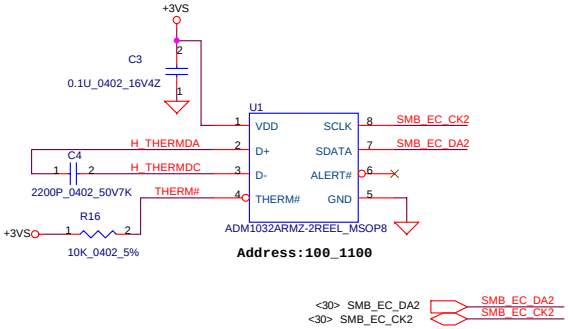
H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

XDP Connector

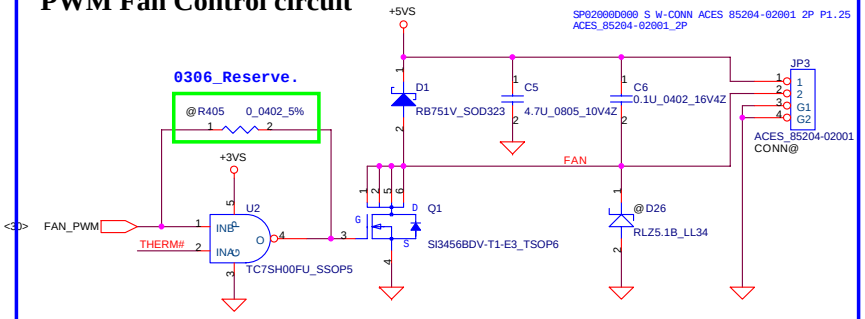
layout note: Change R7 to 649 ohm if using XTP to ITP adapter



Thermal Sensor ADM1032ARMZ



PWM Fan Control circuit



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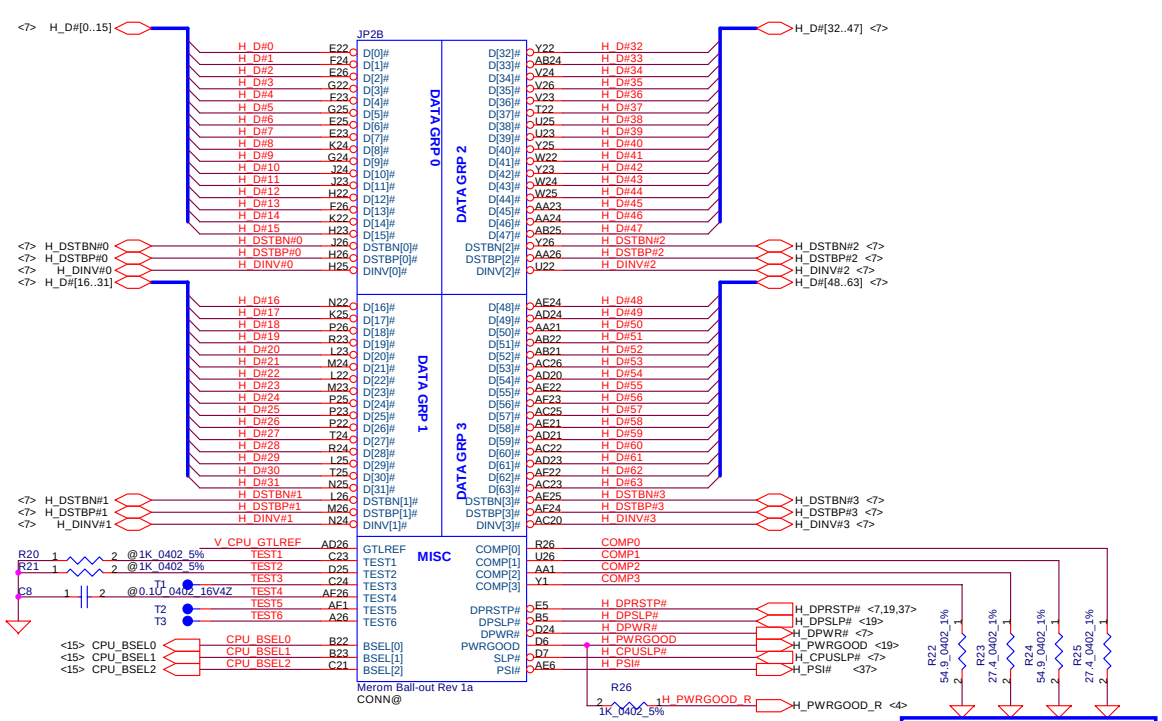
Issued Date	2006/02/13	Deciphered Date	2006/03/10

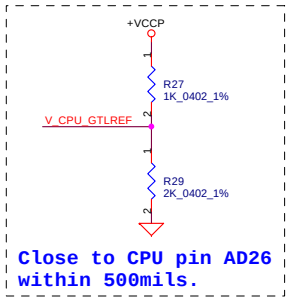
Compal Electronics, Inc.			
Title: Merom(1/3)-AGTL+/XDP			
Size: Custom	Document Number: LA-3732P		Rev: 0.2
Date: Wednesday, March 14, 2007	Sheet 4 of 40		



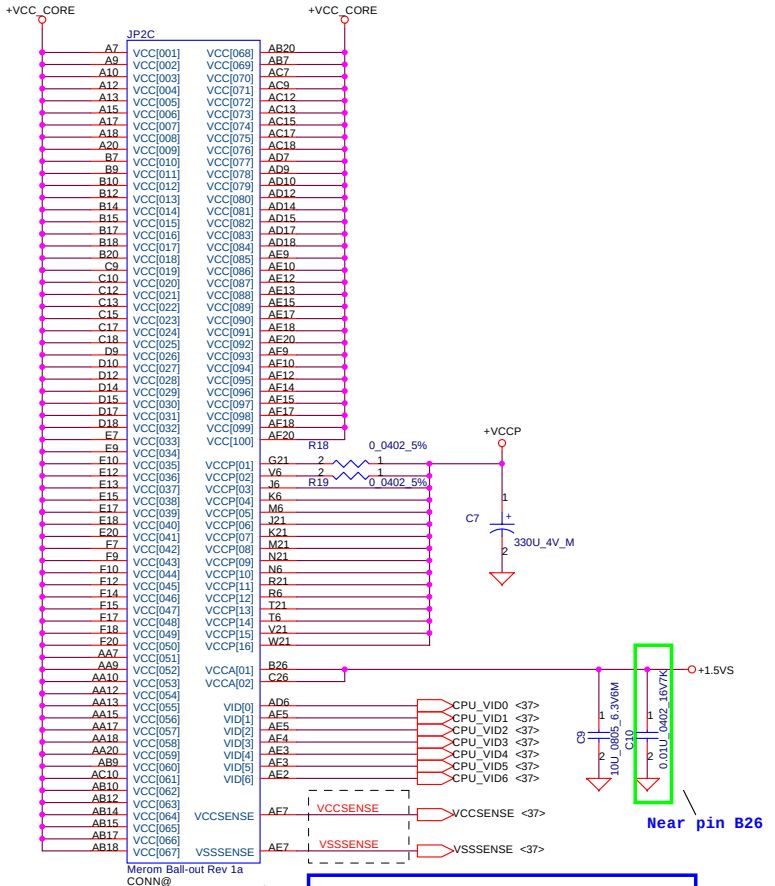
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

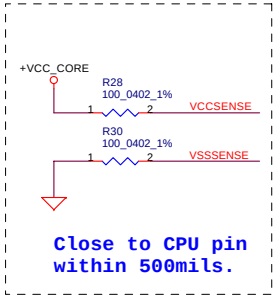
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Close to CPU pin AD26 within 500mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

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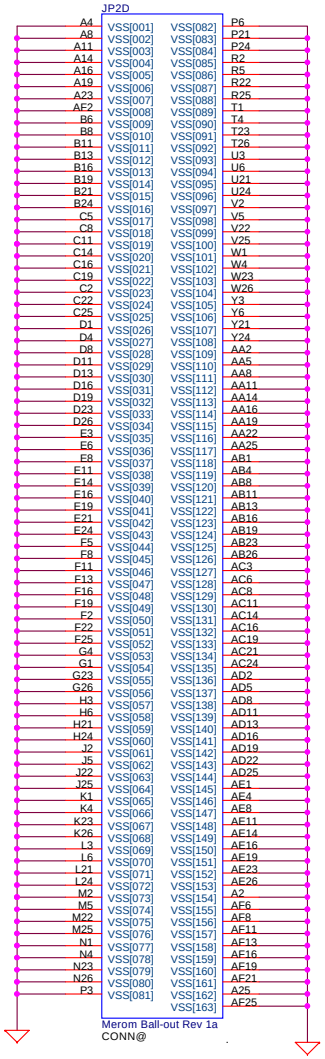
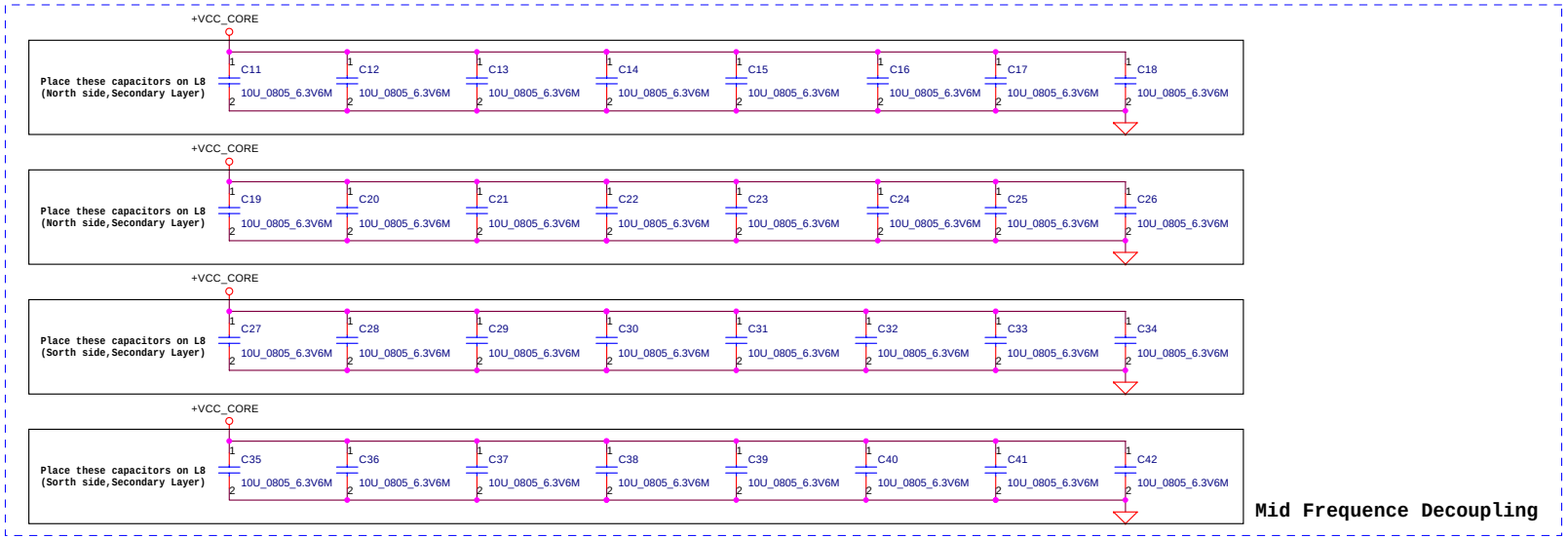
Compal Electronics, Inc.

Title: Merom(2/3)-AGTL+/PWR

Size	Document Number	Rev
Custom	LA-3732P	0.2

Date: Wednesday, March 14, 2007 Sheet 5 of 40

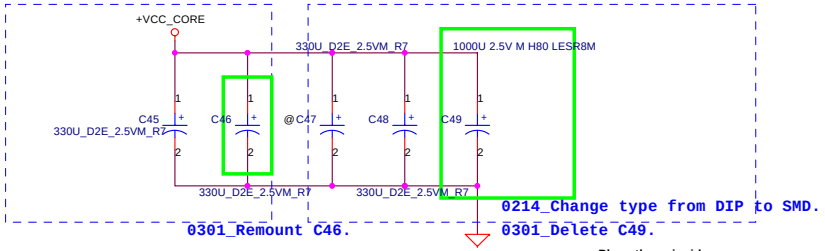




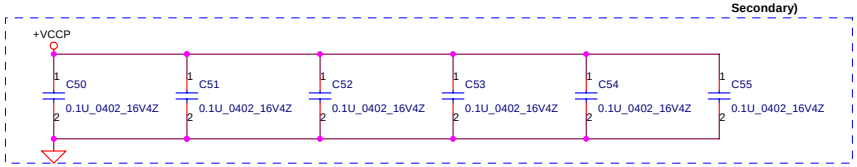
Mid Frequence Decoupling

Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



Place these inside socket cavity on L8 (North side Secondary)



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Compal Electronics, Inc.			
Title: Merom(3/3)-GND&Bypass			
Size: Custom	Document Number: LA-3732P		Rev: 0.2
Date: Wednesday, March 14, 2007	Sheet 6 of 40		

For Crestline: 20ohm
For Calero: 80.6ohm

layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

within 100 mils from NB

Near B3 pin

Layout Note:
V_DDR_MCH_REF
trace width and spacing is 20/20.

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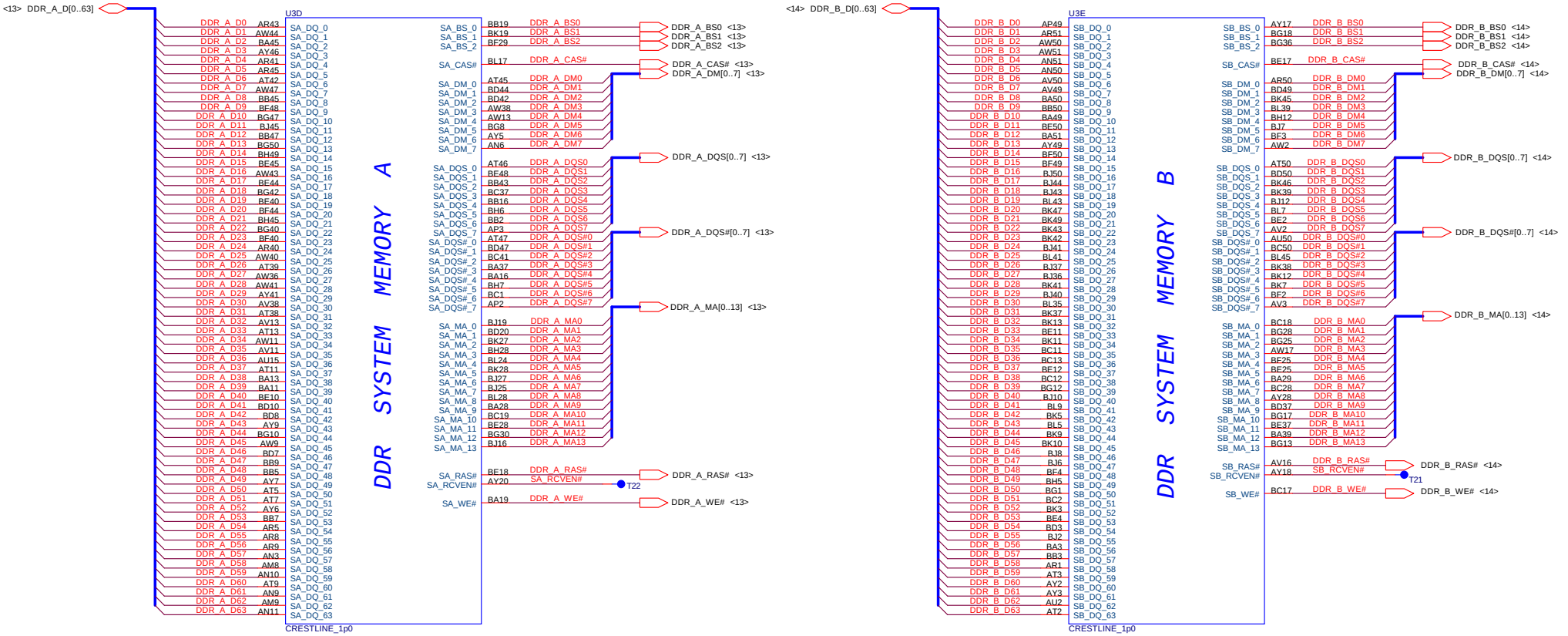
Compal Electronics, Inc.

Title: CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size	Document Number	Rev
Custom	LA-3732P	0.2

Date: Wednesday, March 14, 2007 | Sheet 7 of 40



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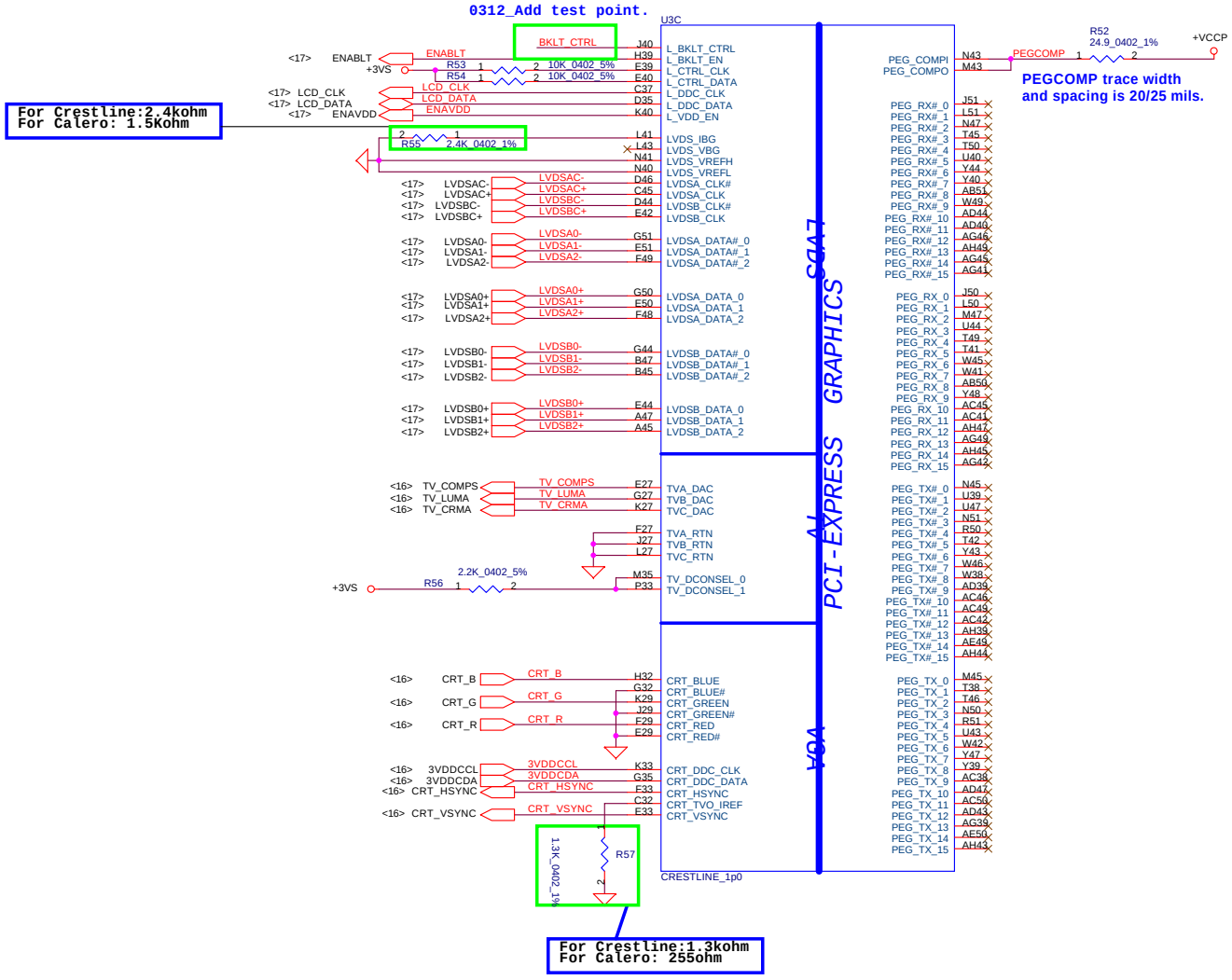
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **CRESTLINE((2/6)-DDR2 A/B CH**

Size	Document Number	Rev
Custom	LA-3732P	0.2

Date: Wednesday, March 14, 2007 Sheet 8 of 40



Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

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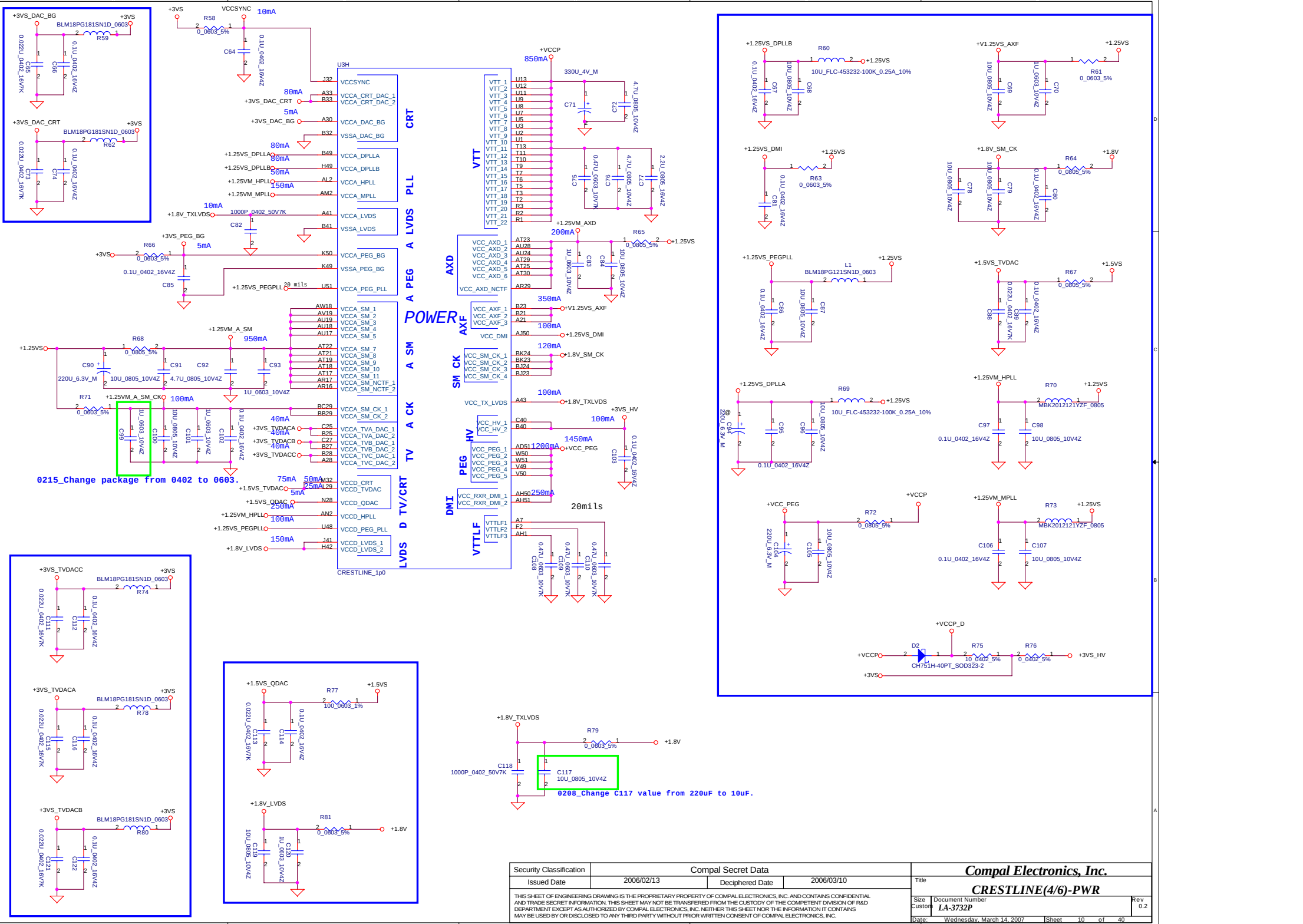
Title: CRESTLINE((3/6)-VGA/LVDS/TV

Size	Document Number	Rev
Custom	LA-3732P	0.2

Date: Wednesday, March 14, 2007 Sheet 9 of 40



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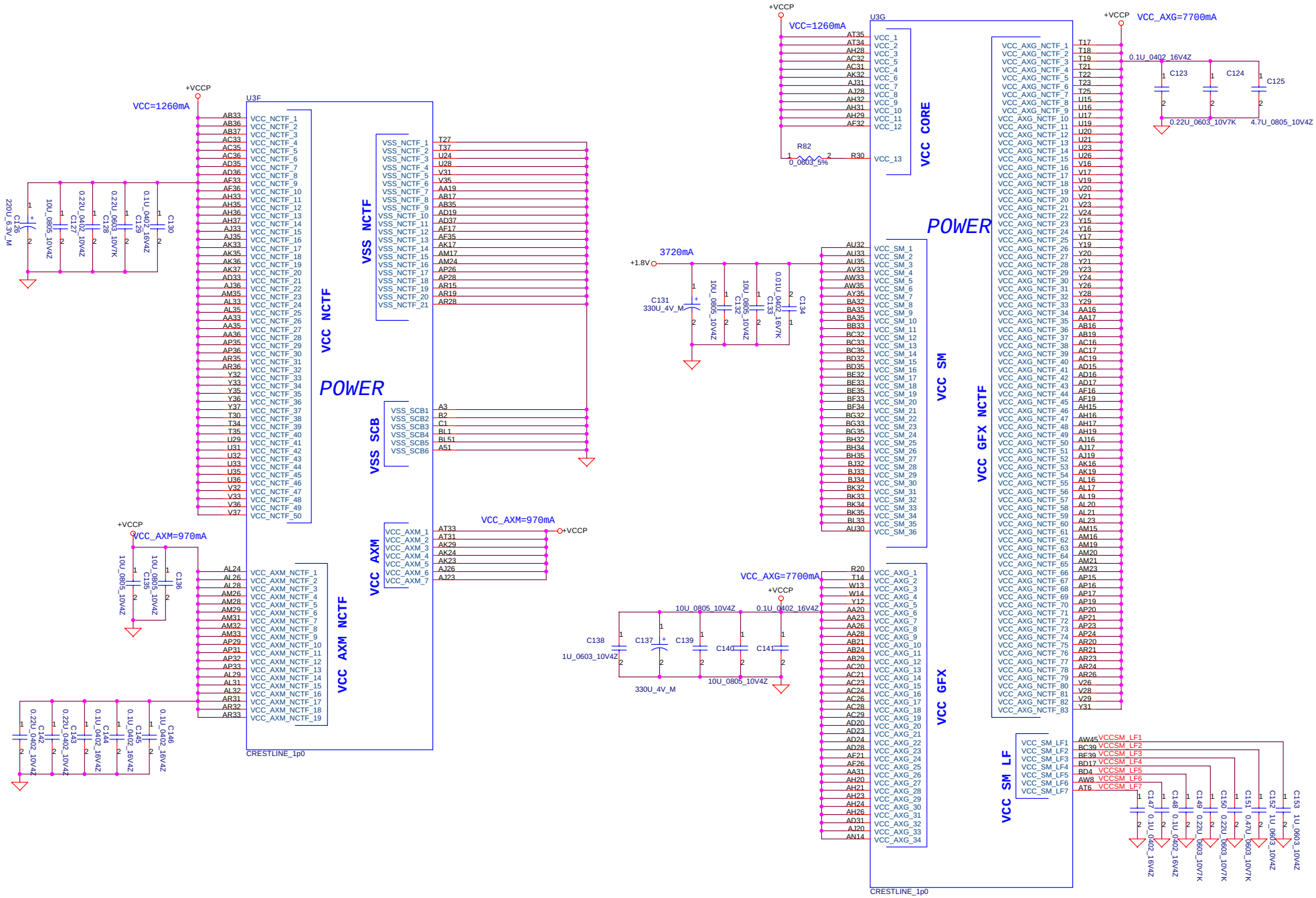
Compal Electronics, Inc.

Title: **CRESTLINE(4/6)-PWR**

Size	Document Number	Rev
Custom	LA-3732P	0.2

Date: Wednesday, March 14, 2007 Sheet 10 of 40



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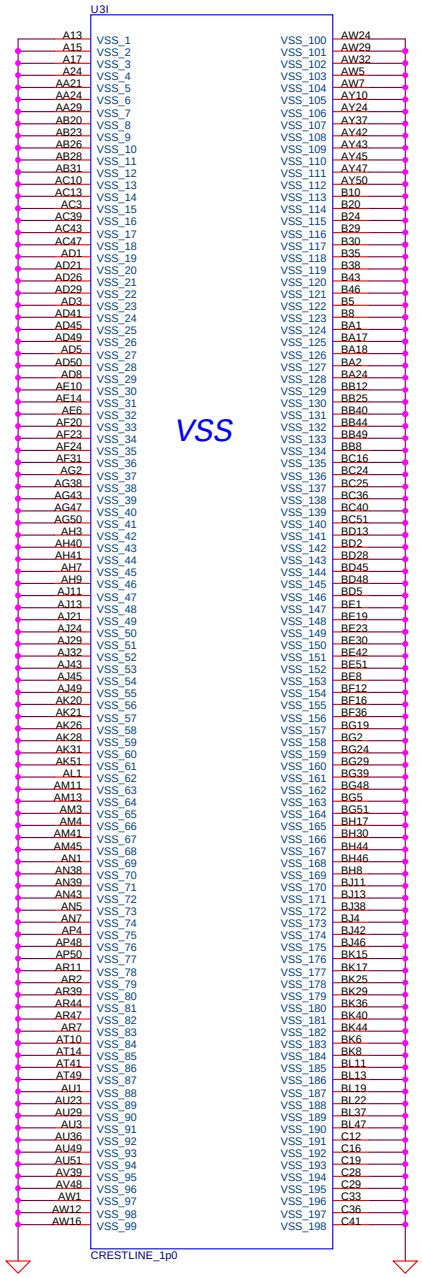
Issued Date	2006/02/13	Deciphered Date	2006/03/10

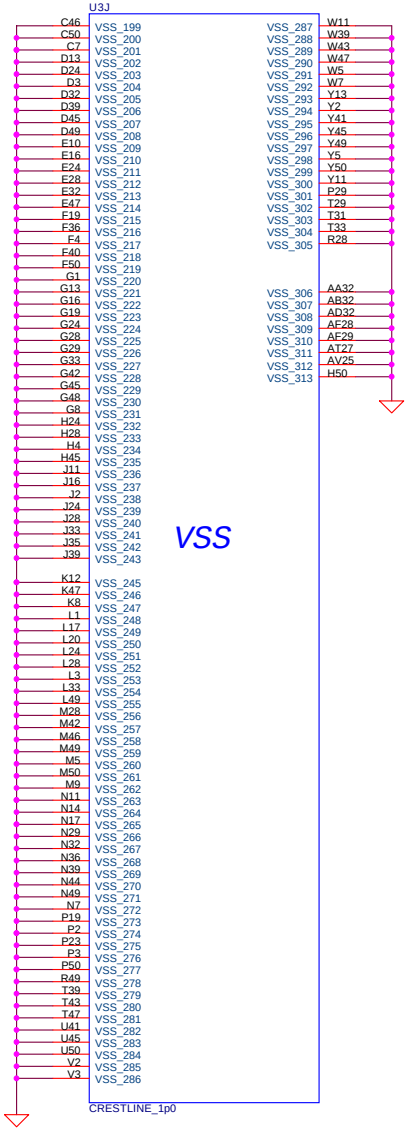
Compal Electronics, Inc.

Title: **CRESTLINE((5/6)-PWR/GND**

Size	Document Number	Rev
Custom	LA-3732P	0.2

Date: Wednesday, March 14, 2007 | Sheet 11 of 40





Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

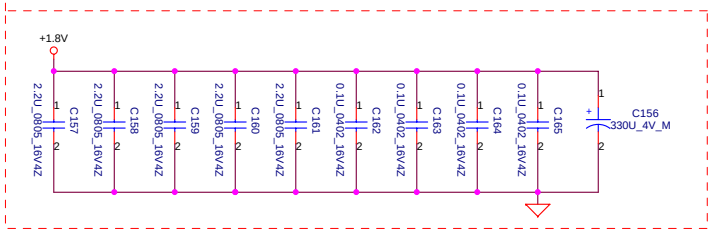
Title: **CRESTLINE((6/6)-PWR/GND**

Size	Document Number	Rev
Custom	LA-3732P	0.2

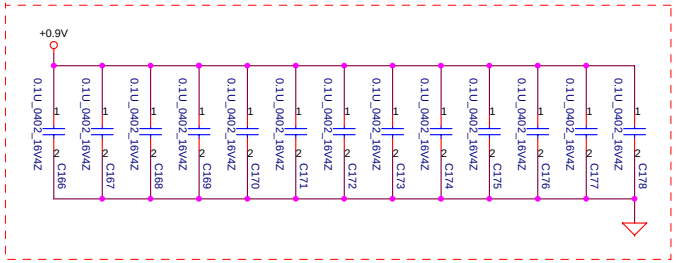
Date: Wednesday, March 14, 2007 Sheet 12 of 40

<8> DDR_A_DQS#[0..7]
<8> DDR_A_D[0..63]
<8> DDR_A_DM[0..7]
<8> DDR_A_DQS[0..7]
<7,8> DDR_A_MA[0..14]

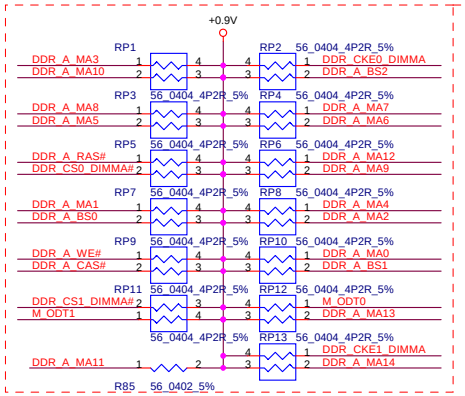
Layout Note:
Place near JP34



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP34,all trace length Max=1.5"



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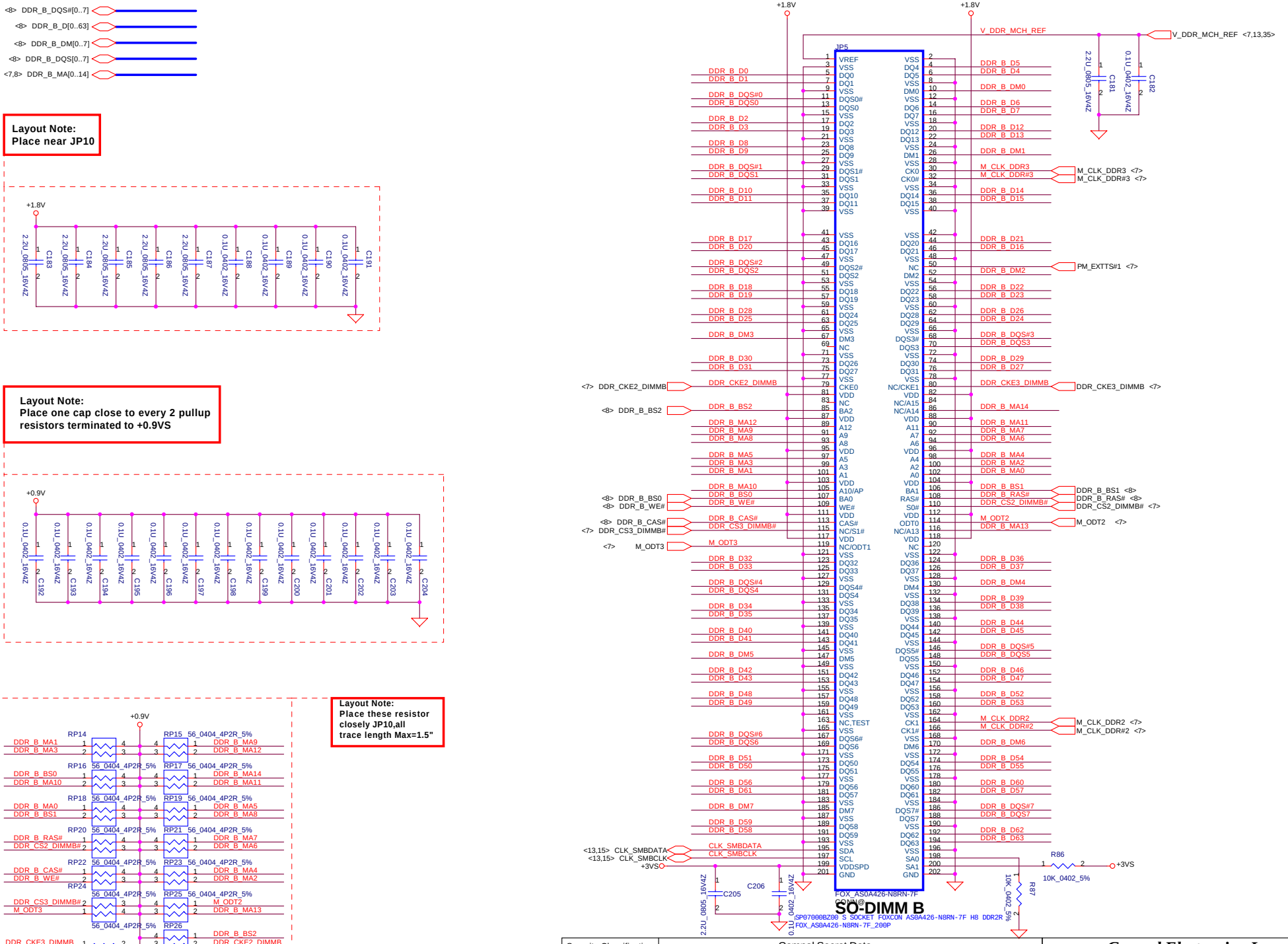
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	LA-3732P	0.2

Date: Wednesday, March 14, 2007 | Sheet 13 of 40


Layout Note:
Place near JP10
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
Layout Note:
Place these resistor
closely JP10,all
trace length Max=1.5"
JP5
SO-DIMM B
FOX_AS0A426-N8RN-7F
CONN@
SP07000BZ00 S SOCKET FOXCON AS0A426-N8RN-7F H8 DDR2R
FOX_AS0A426-N8RN-7F_200P
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Compal Secret Data
Issued Date
2006/02/13
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2006/03/10
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DDRII-SODIMM SLOT2
Size
Document Number
LA-3732P
Rev
0.2
Date: Wednesday, March 14, 2007
Sheet 14 of 40

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
	No Stuff	R1083	R1107	R1128			
		R1113	R1098				
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083	R1086	R1098	R1128		
		R1074	R1107	R1113			

Place close to U4

0308_Change R89 and R92 form 0 ohm to bead, C209, C211, C216, C218 from 0.1uF to 680pF.

SB, MINI PCI

CLRP4,CLRP5 for 667/800 FSB select
SHORT CLRP5, NO SHORT CLRP4 -- CPU option
SHORT CLRP4, NO SHORT CLRP5 -- FSB 667

0301_Change R105 from 22 ohm to 0 ohm.
0312_Change R106, 107, 109 from 22 to 33 ohm.

Routing the trace at least 10mil

For Layout request:
1. Change MINI_CLKREQ# from pin 32 to pin 43.
2. Change CLK_PCIE_MCARD from SRC9 to SRC6.

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1= Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

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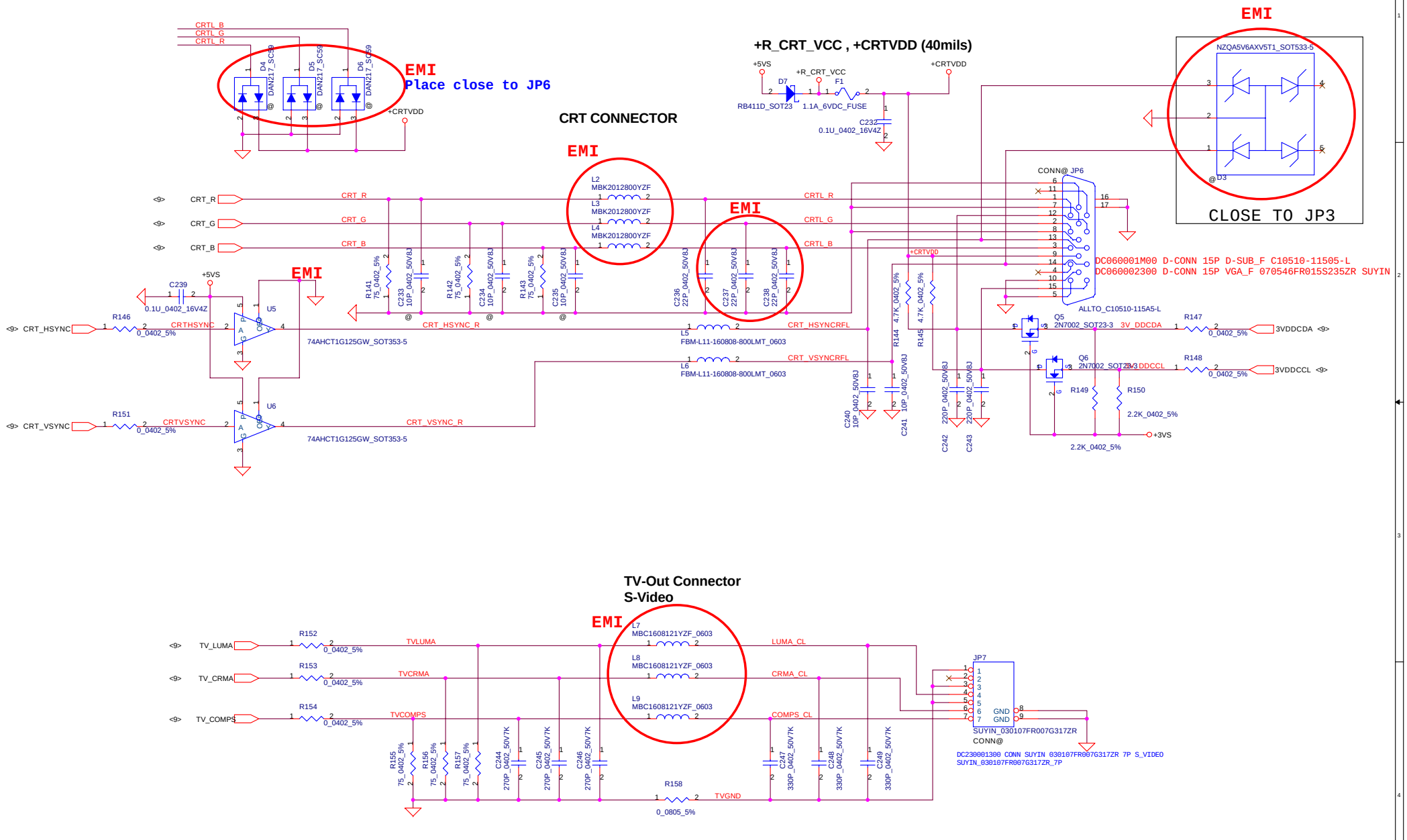
Compal Electronics, Inc.

Title: Clock generator

Size: | Document Number: LA-3732P | Rev: 0.2

Date: Wednesday, March 14, 2007 | Sheet 15 of 40



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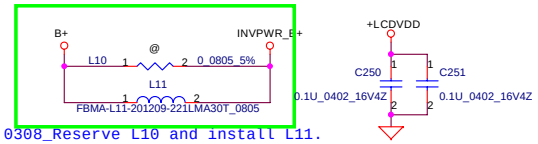
Compal Electronics, Inc.

Title: **CRT & TVout Connector**

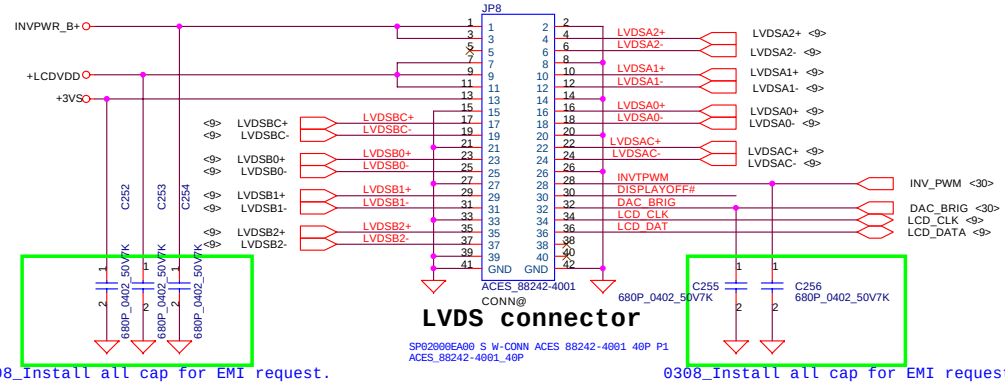
Size	Document Number	Rev
	LA-3732P	0.2

Date: Wednesday, March 14, 2007 | Sheet 16 of 40

LVDS CONN



0308_Reserve L10 and install L11.

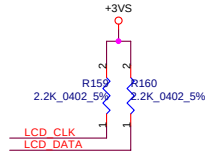


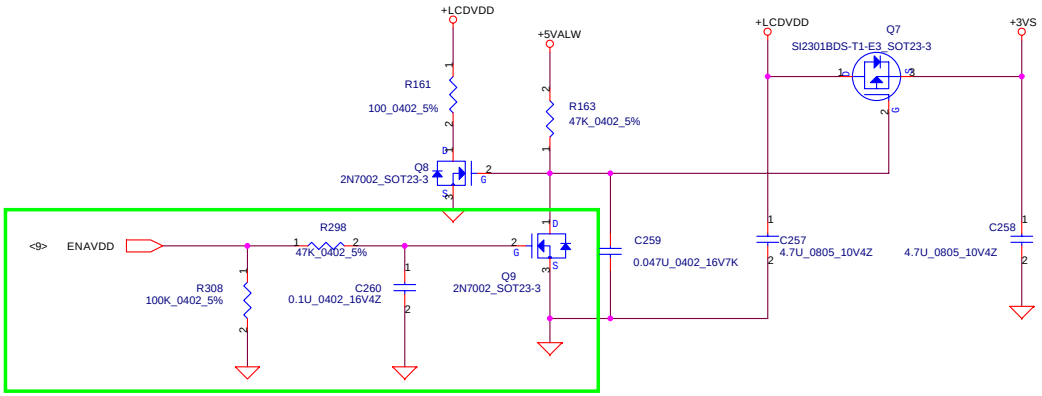
LVDS connector

SP02000EA00 S W-CONN ACES 88242-4001 40P P1
ACES_88242-4001_40P

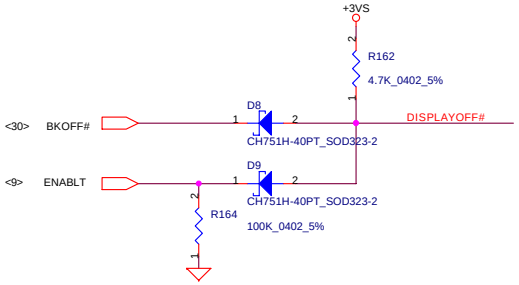
0308_Install all cap for EMI request.

0308_Install all cap for EMI request.





Avoid Panel display garbage after power on.



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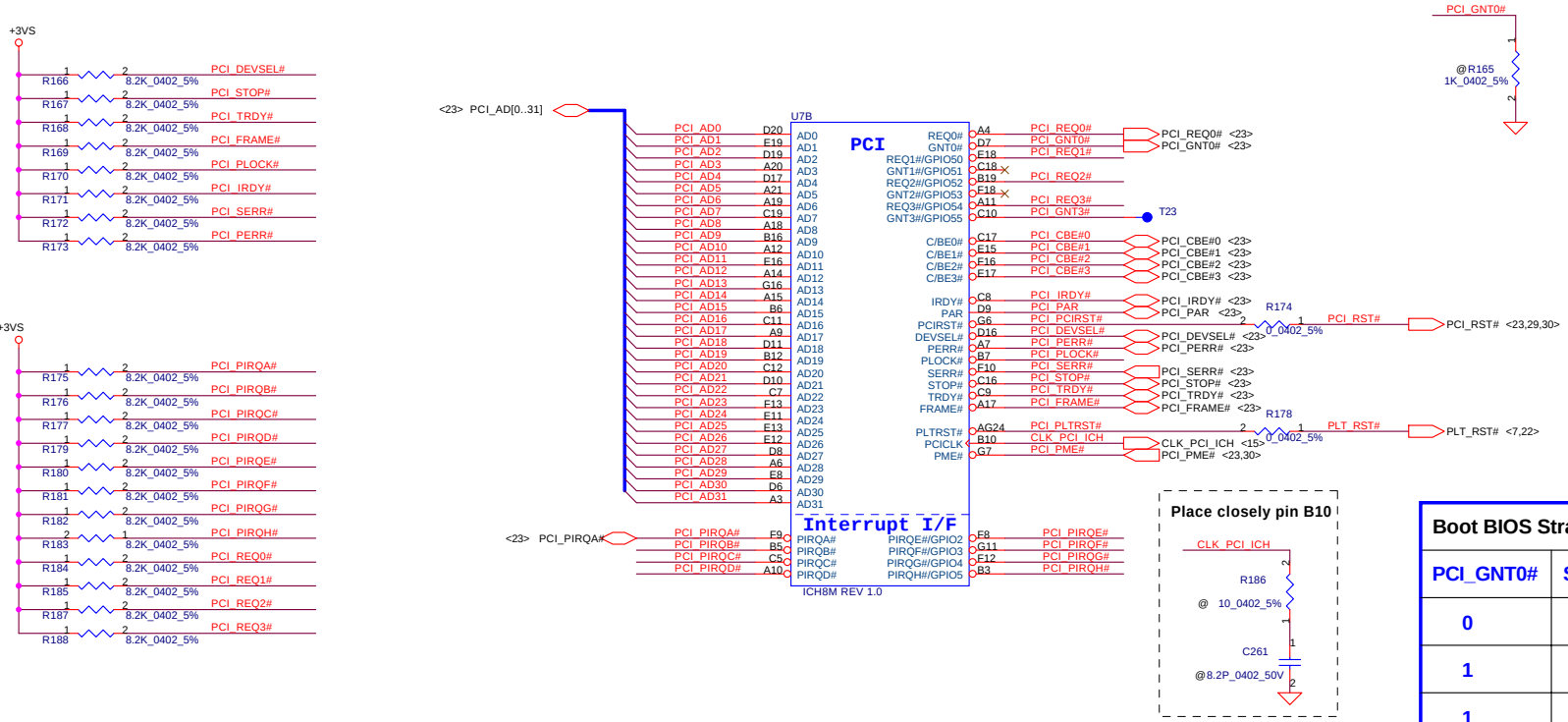
Compal Electronics, Inc.

Title: **LCD CONN.**

Size	Document Number	Rev
	LA-3732P	0.2

Date: Wednesday, March 14, 2007 | Sheet 17 of 40



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

A16 swap override Strap	
PCI_GNT3#	*Low= A16 swap override Enble High= Default

Compal Electronics, Inc.

Title: ICH8(1/4)-PCI/INT

Size: | Document Number: LA-3732P | Rev: 0.2

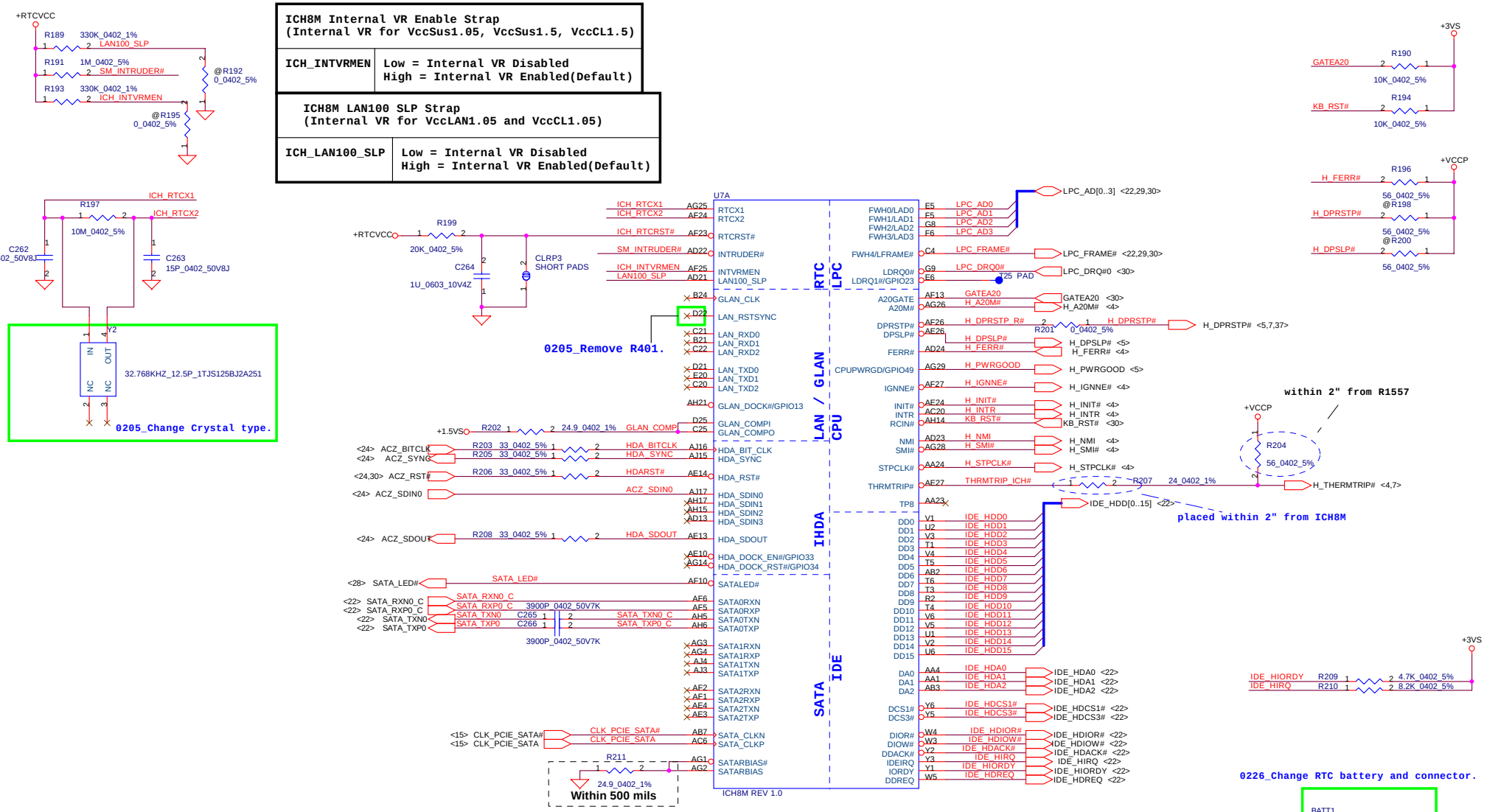
Date: Wednesday, March 14, 2007 | Sheet 18 of 40

ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



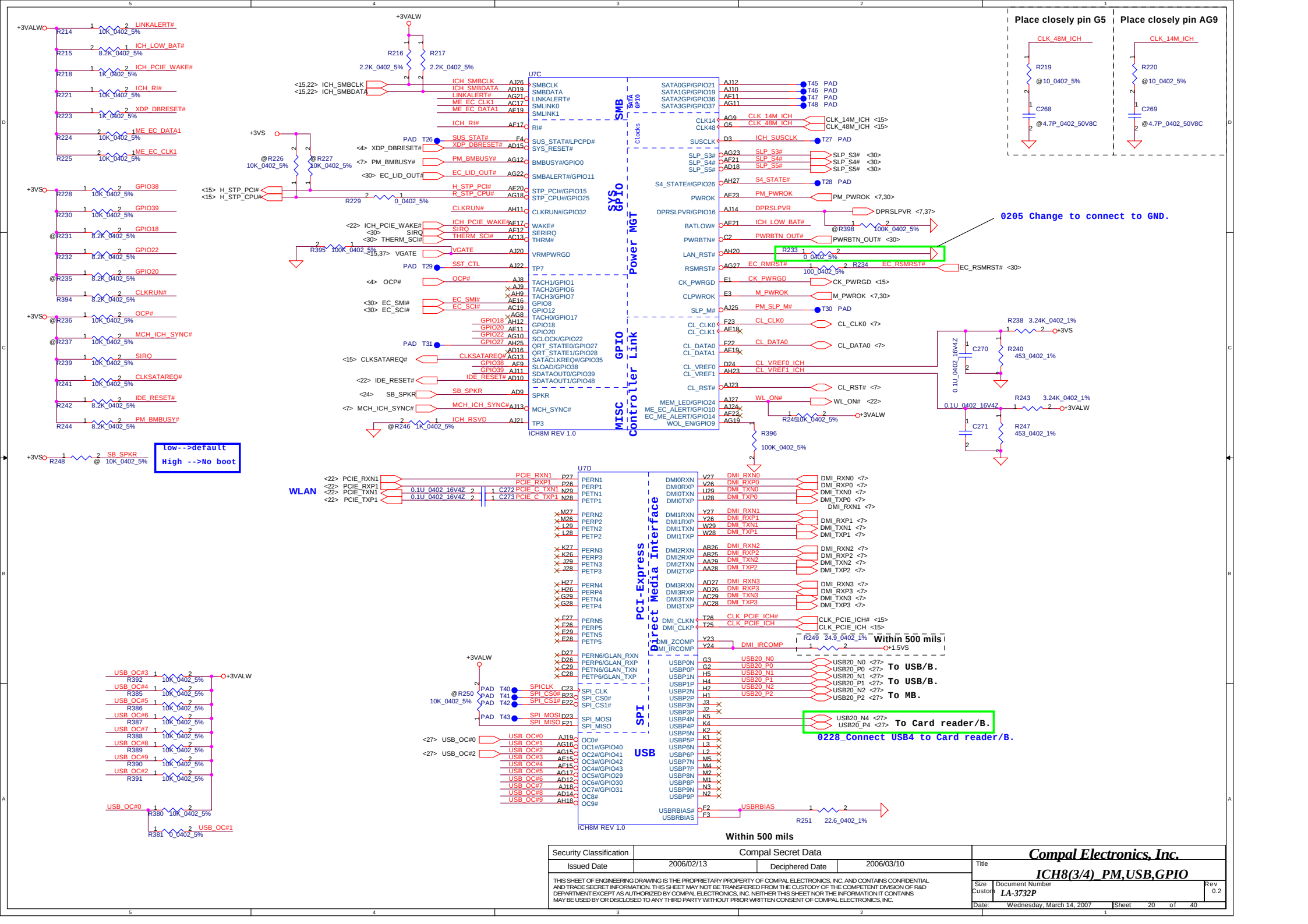
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **ICH8(2/4)_LAN,HD,IDE,LPC**

Size	Document Number	Rev
Custom	LA-3732P	0.2

Date: Wednesday, March 14, 2007 Sheet 19 of 40



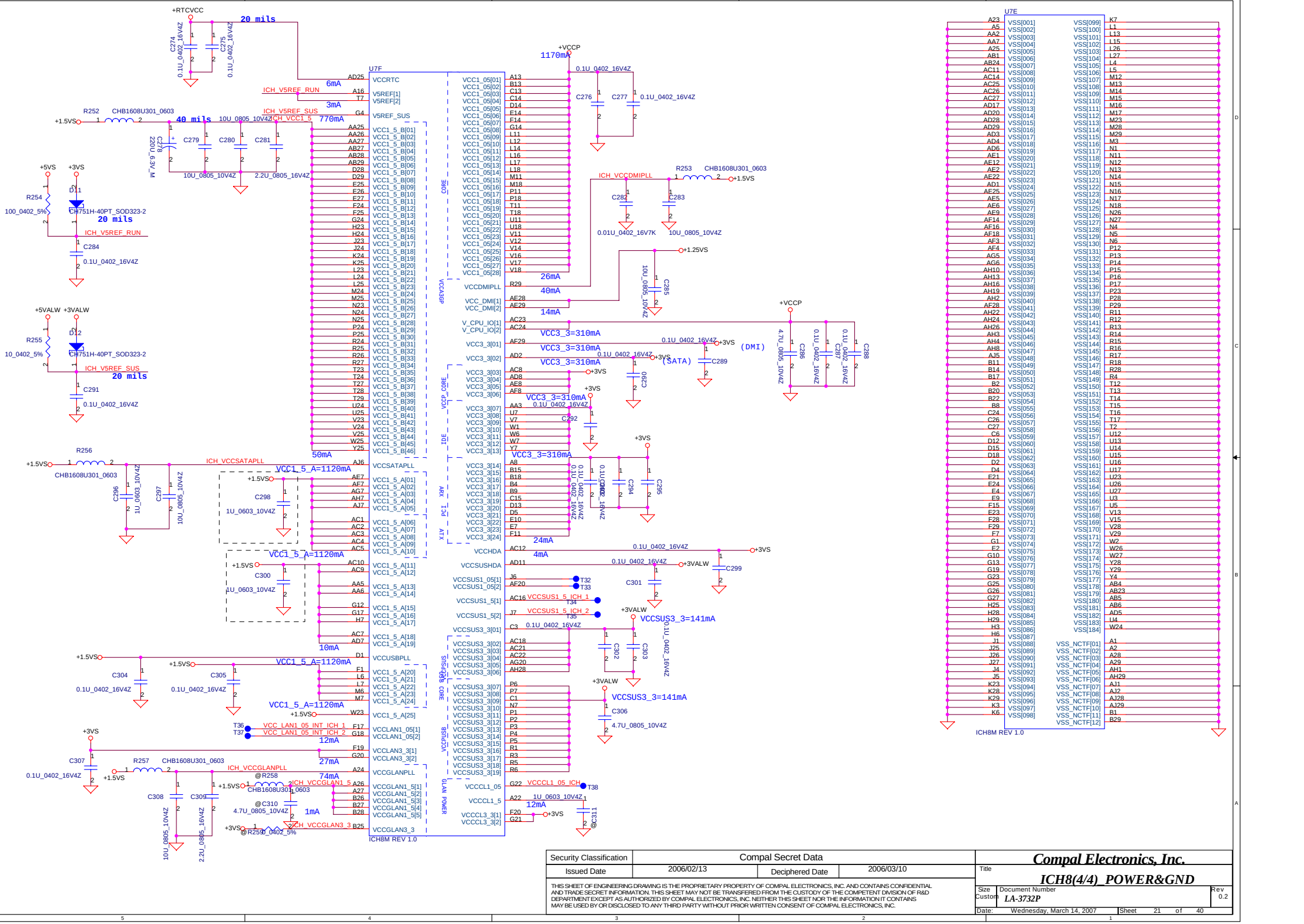
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH8(3/4)_PM,USB,GPIO

Size	Document Number	Rev
Custom	LA-3732P	0.2

Date: Wednesday, March 14, 2007 Sheet 20 of 40



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

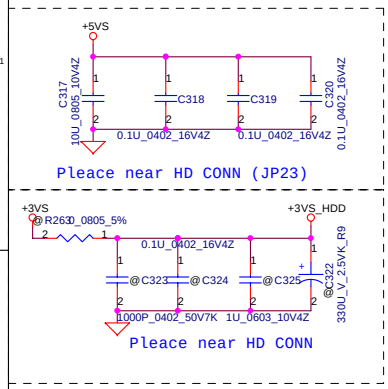
Compal Electronics, Inc.

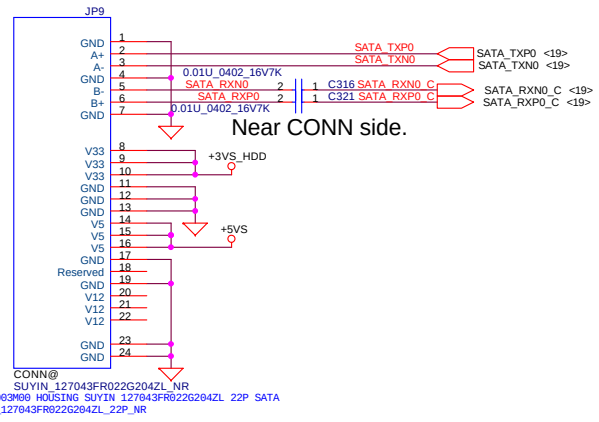
Title: **ICH8(4/4)_POWER&GND**

Size	Document Number	Rev
Custom	LA-3732P	0.2

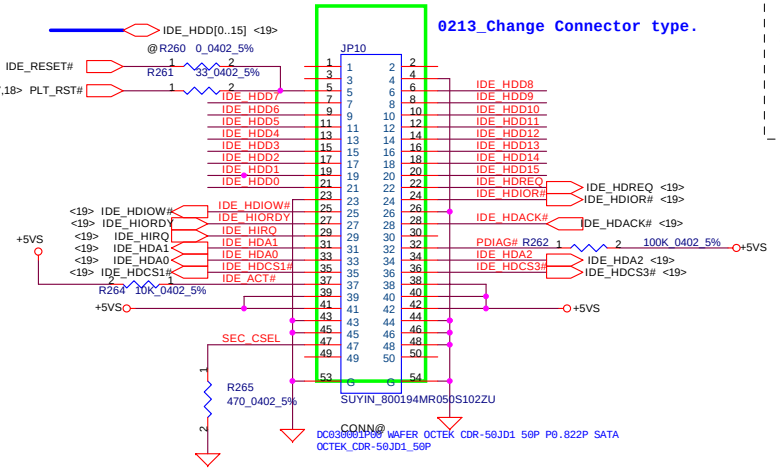
Date: Wednesday, March 14, 2007 | Sheet 21 of 40

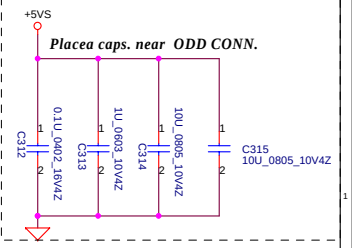
HDD Connector



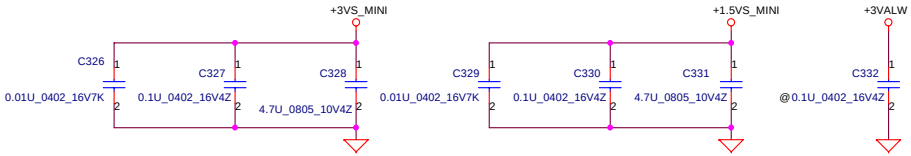


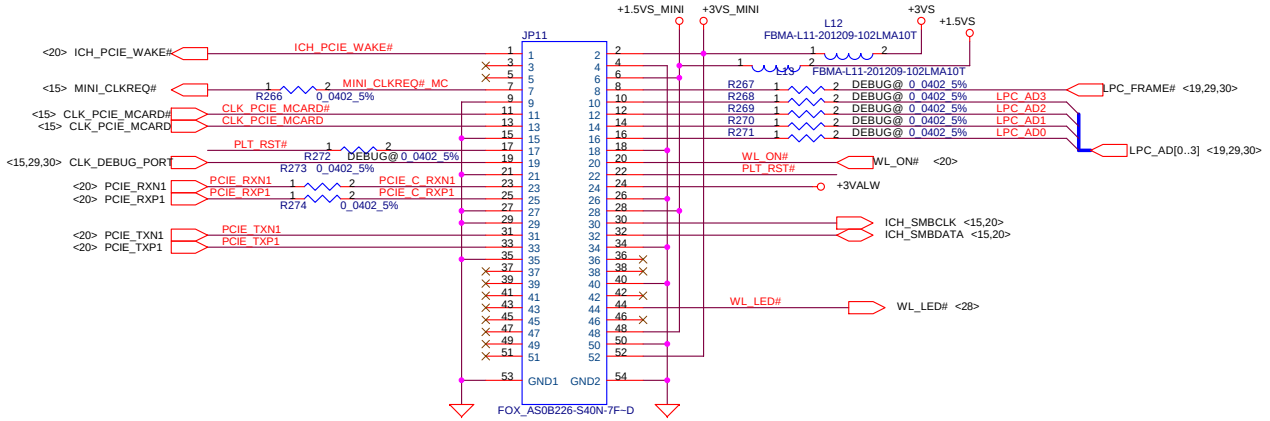
CD-ROM Connector





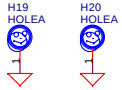
Mini-Express Card---WLAN





SP01000P700 S H-CONN ACES 88914-5204 52P P0.8

Mini Card STANDOFF



EC029000100 MINICARD_STANDOFF_8

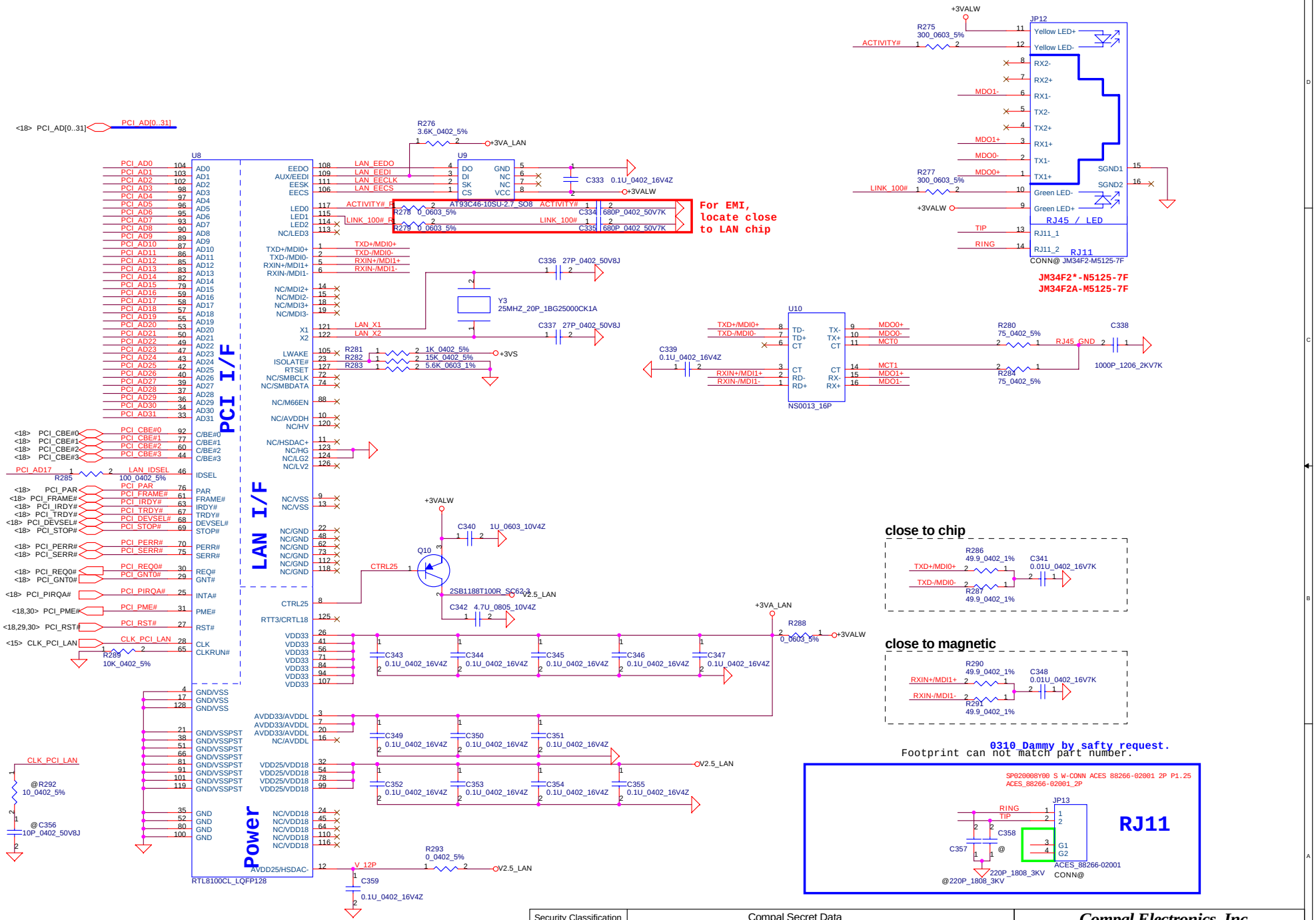
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2007/08/29

Compal Electronics, Inc.

Title: HDD/ODD/Mini Card CONN.

Size	Document Number	Rev
	LA-3732P	0.2

Date: Wednesday, March 14, 2007 Sheet 22 of 40



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2007/08/29

Compal Electronics, Inc.

Title: LAN-8100CL

Size: | Document Number: LA-3732P | Rev: 0.2

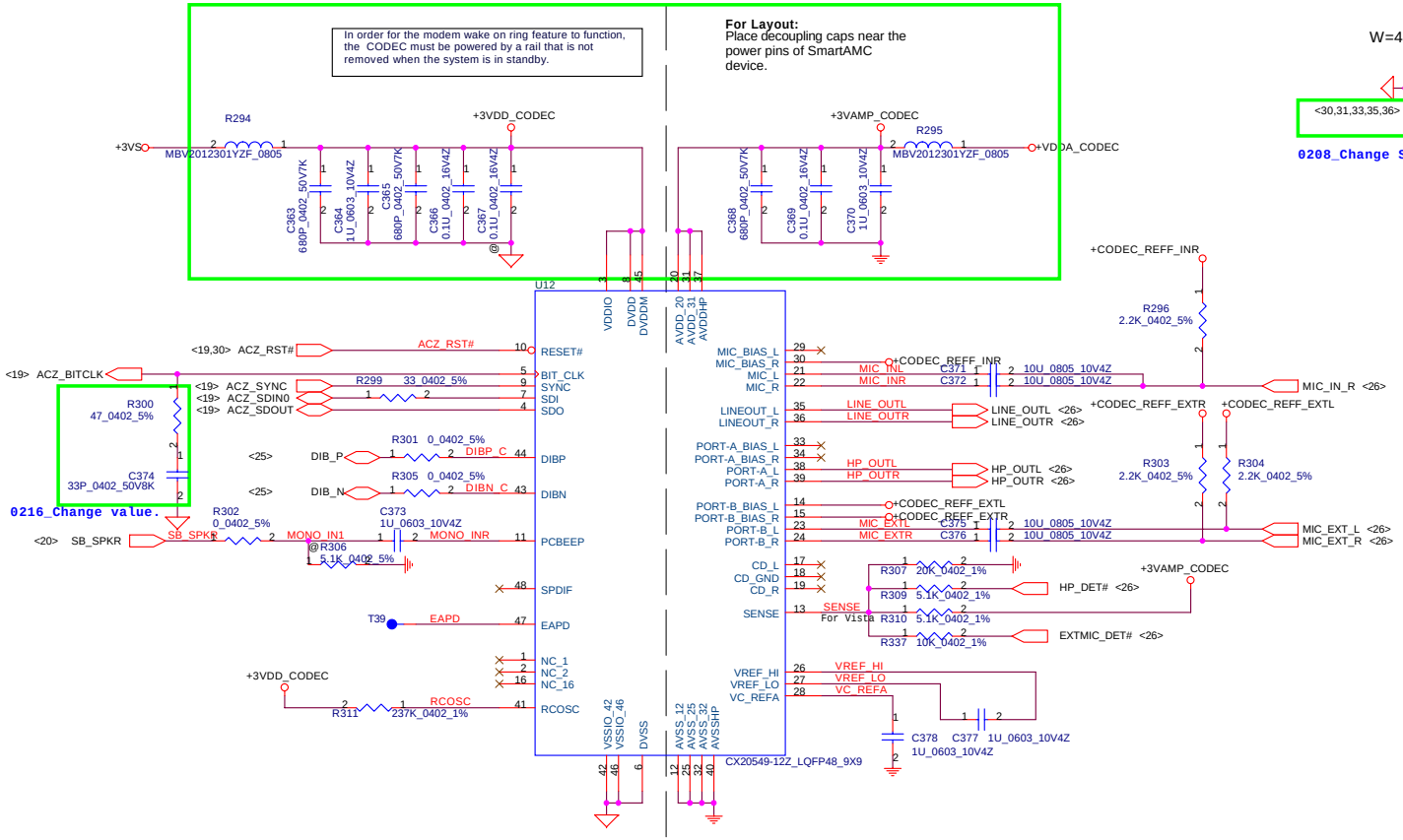
Date: Wednesday, March 14, 2007 | Sheet 23 of 40

AUDIO CODEC

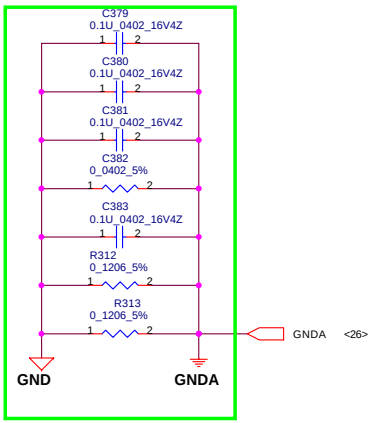
0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.



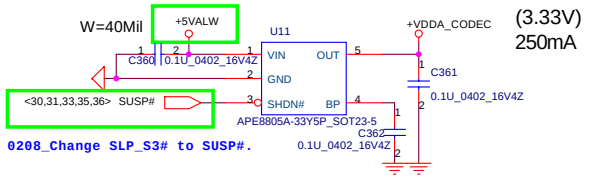
DIGITAL **ANALOG**



0312_Mount C379~383, R313.

CODEC POWER

0212_Change to +5VALW.



0208_Change SLP_S3# to SUSP#.

HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0(LOW)	0(LOW)	OFF	ON	ON	Disable
0(LOW)	NC	OFF	ON	OFF	Disable
NC	0(LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

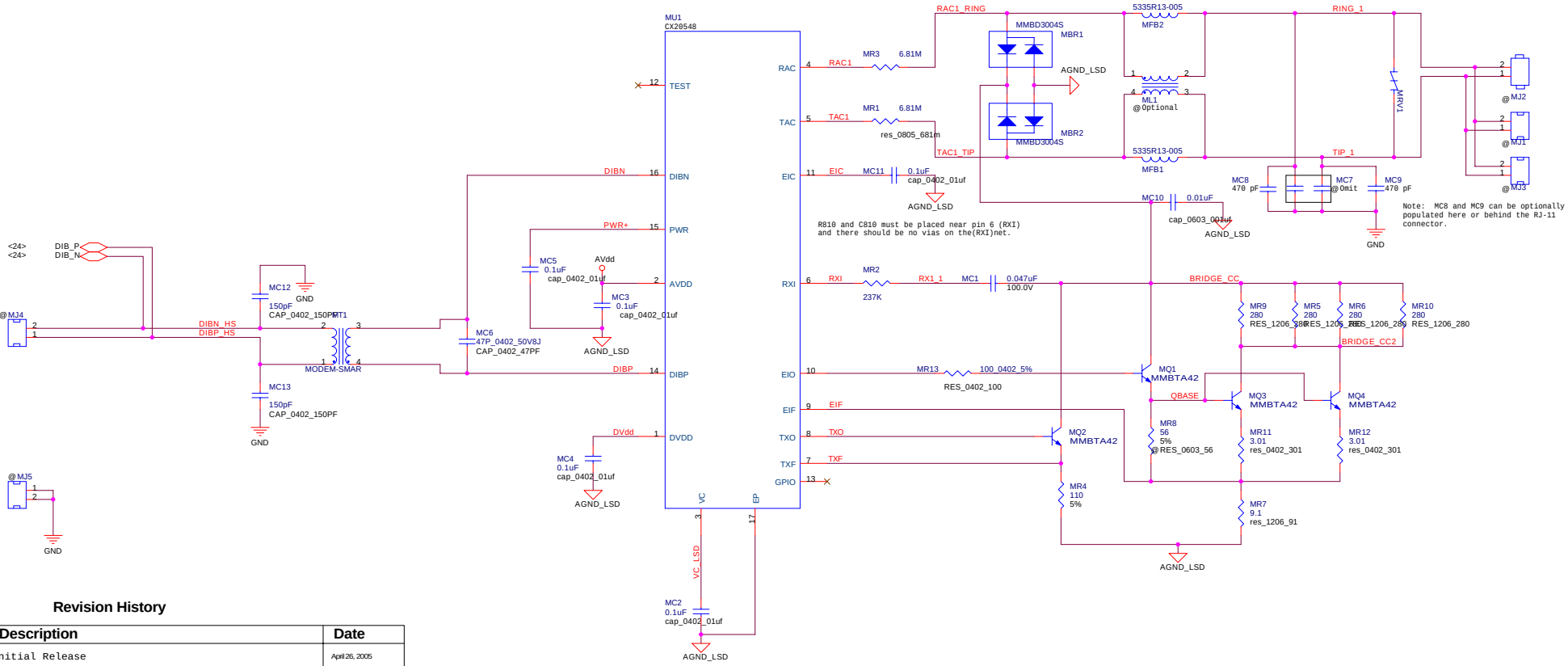
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: AMOM_codec

Size: Custom | Document Number: LA-3732P | Rev: 0.2

Date: Wednesday, March 14, 2007 | Sheet 24 of 40



Revision History

REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	August 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

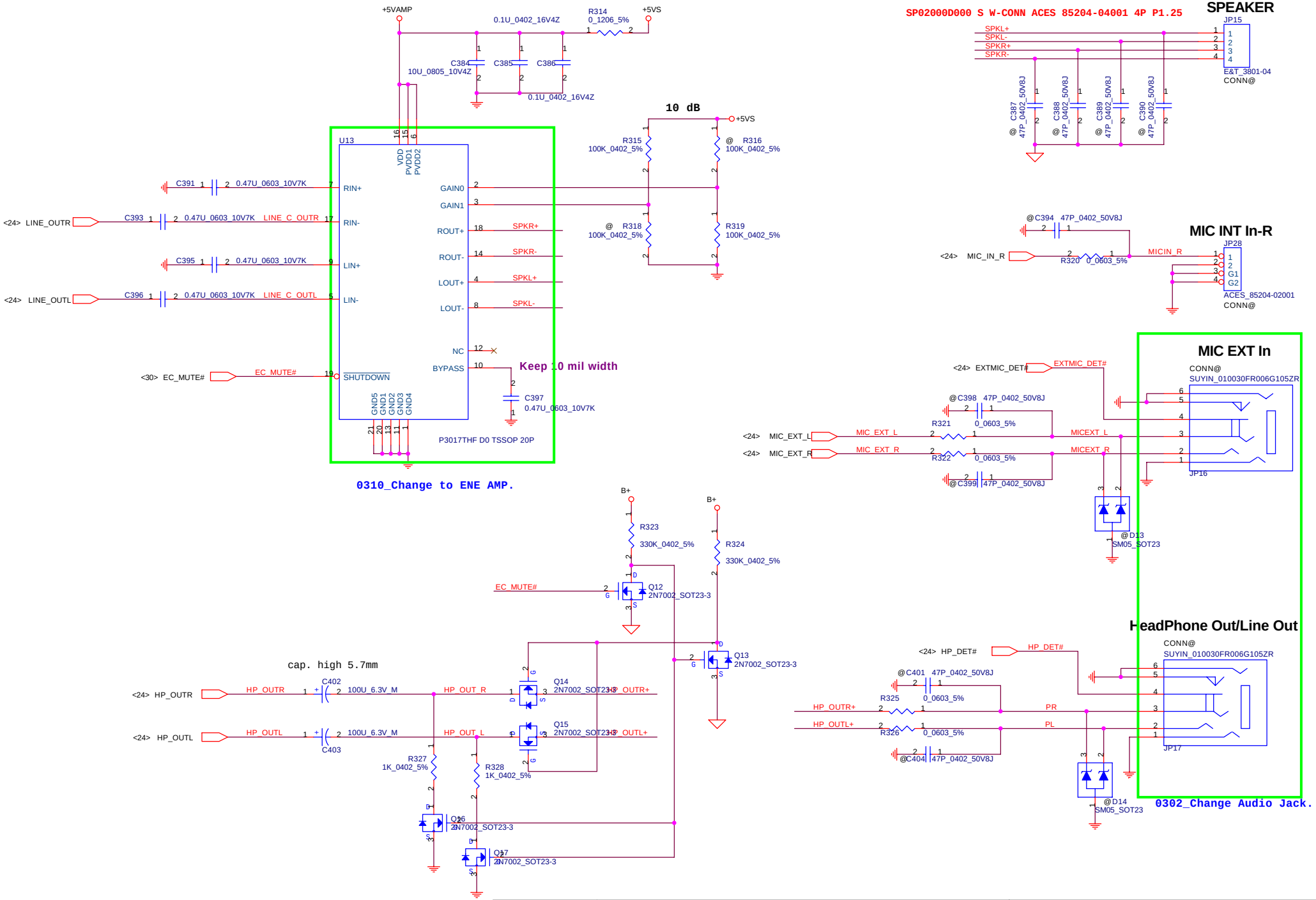
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2007/07/26

Compal Electronics, Inc.

Title: **AMOM-CX20548**

Size | Document Number: **LA-3732P** | Rev: 0.2

Date: Wednesday, March 14, 2007 | Sheet 25 of 40



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2007/08/29

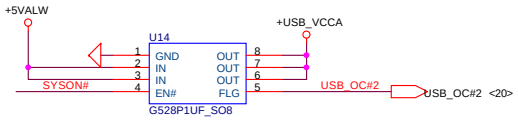
Compal Electronics, Inc.

Title: **AMP & Audio Jack**

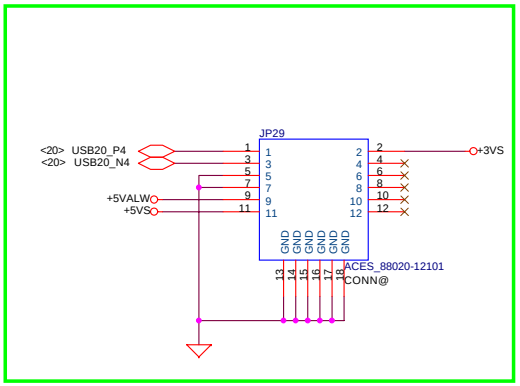
Size	Document Number	Rev
	LA-3732P	0.2

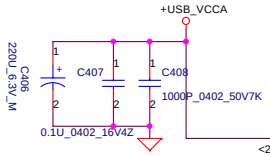
Date: Wednesday, March 14, 2007 Sheet 26 of 40

USB Port

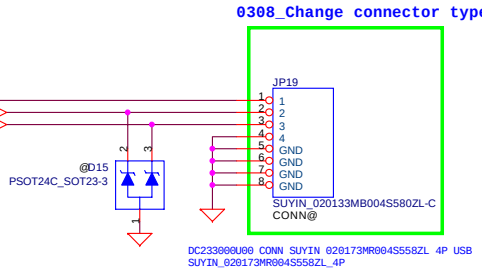


0228_Add JP29 for USB card reader.

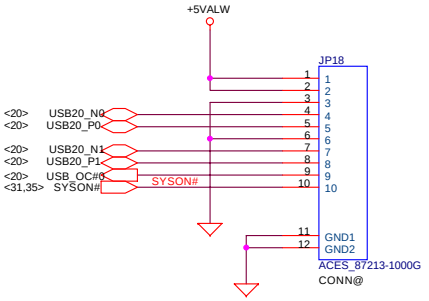




0308_Change connector type.



DC233000U00 CONN SUYIN 020173MR004S558ZL 4P USB
SUYIN_020173MR004S558ZL_4P



SP02000DX00 S W-CONN ACES 87213-1000G 10P P1.0
ACES_87213-1000G_10P

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

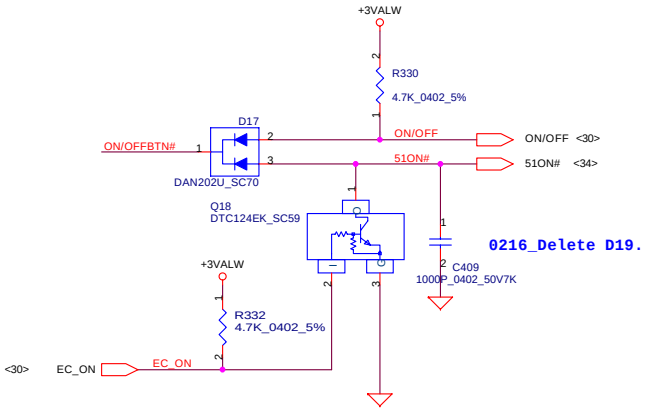
Compal Electronics, Inc.

Title: **USB CONN.**

Size: | Document Number: **LA-3732P** | Rev: 0.2

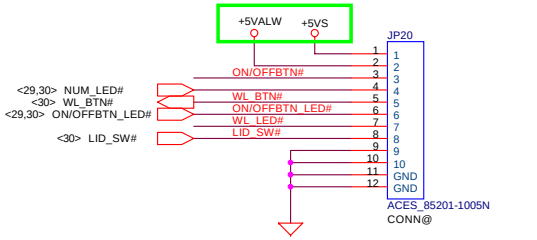
Date: Wednesday, March 14, 2007 | Sheet 27 of 40

Power ON/OFF

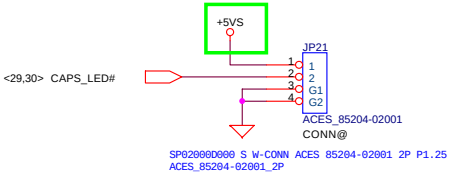


M/BtoS/B

0301_Change Voltage from 3V to 5V.

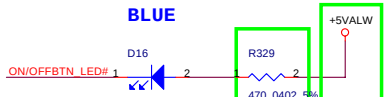


M/B to SB(Caps Lock LED)



POWER LED(Left 1)

BLUE

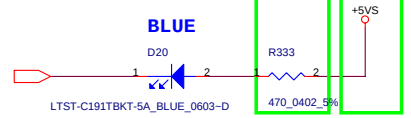


Battery Charge LED(Left 2)

BLUE

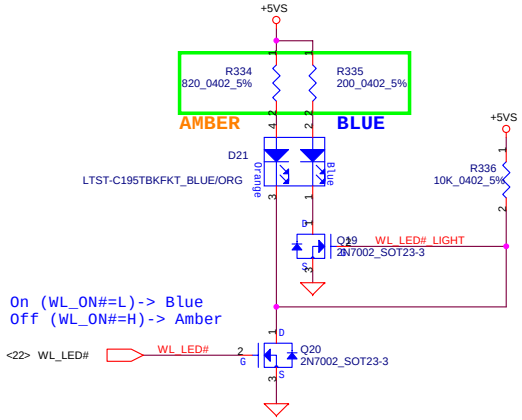
HDD LED(Left 3)

BLUE



0208_Change Voltage from 3V to 5V.

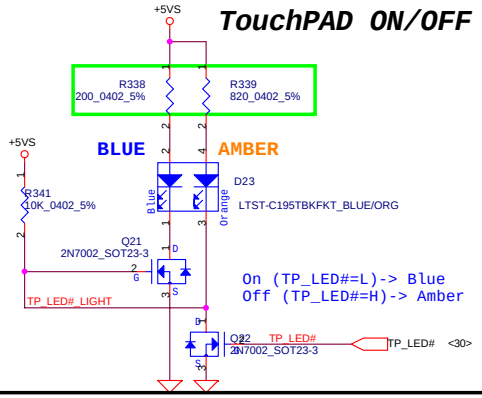
Wireless ON/OFF LED(Left 4)



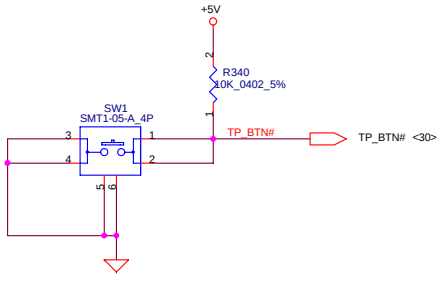
0208_Change R329, R331, R333 to 470 ohm, R334 and R339 to 820 ohm, R335 and R338 to 200 ohm.

0208_Delete reserve component (D25、SW2) for 14.1". D21, D25, D23 Footprint can not match part number.

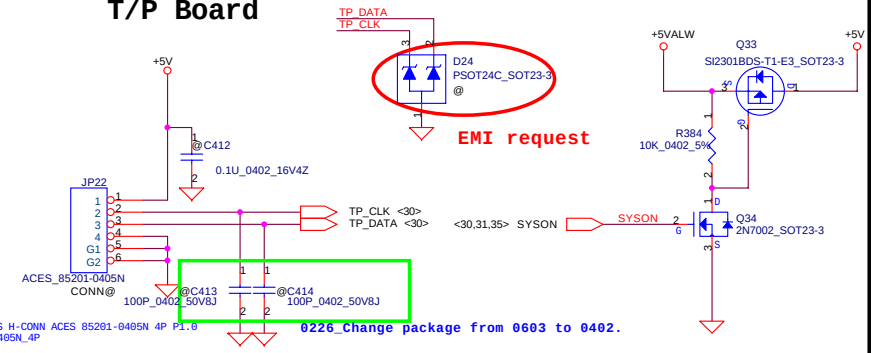
TouchPAD ON/OFF LED



TP ON/OFF



T/P Board



0226_Change package from 0603 to 0402.

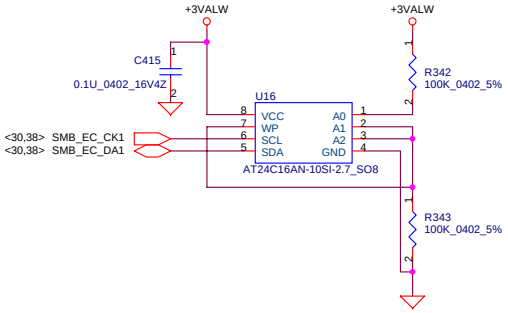
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

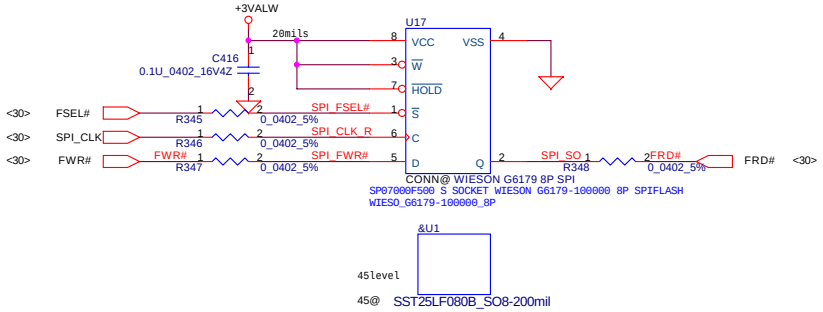
Title: LED/SW

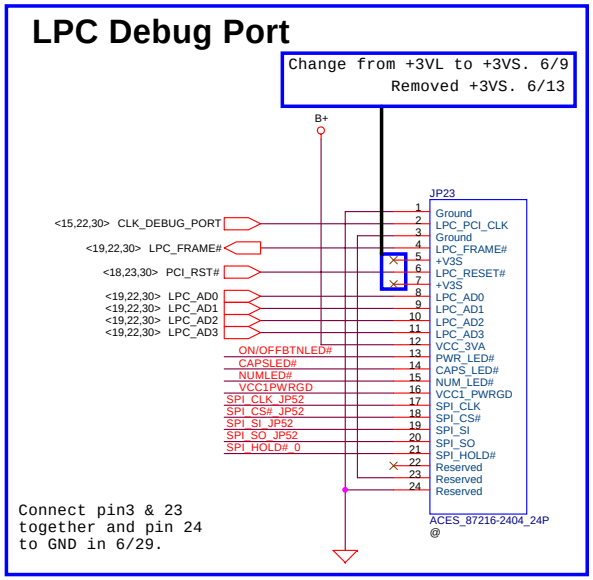
Size	Document Number	Rev
	LA-3732P	0.2

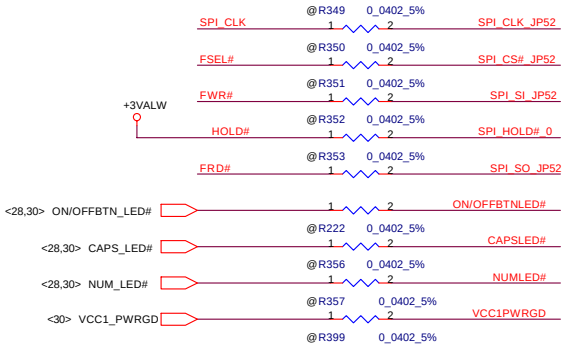
Date: Wednesday, March 14, 2007 Sheet 28 of 40



SPI ROM





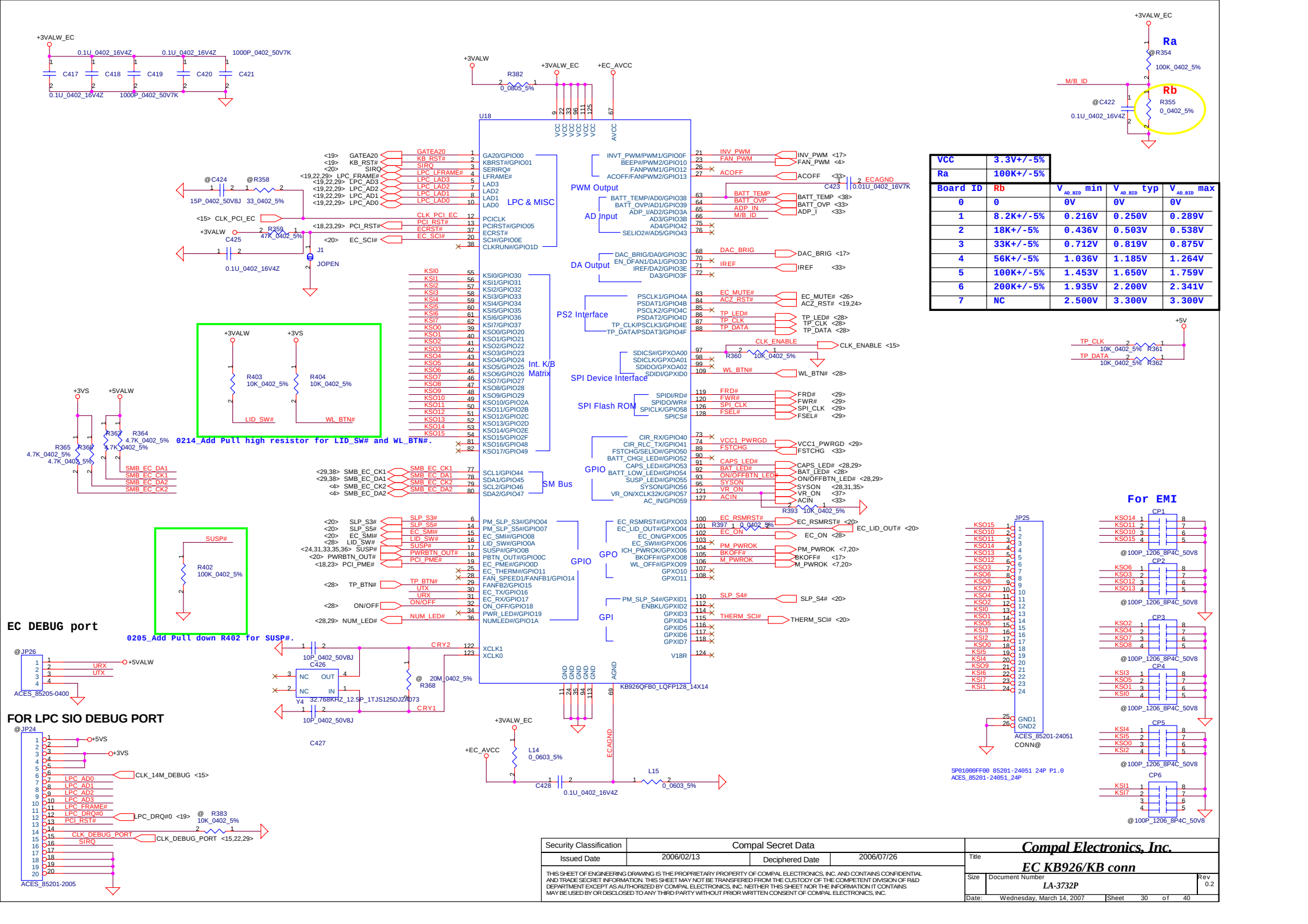


Compal Electronics, Inc.

Title: **BIOS ROM**

Size	Document Number	Rev
	LA-3732P	0.2

Date: Wednesday, March 14, 2007 | Sheet 29 of 40



VCC	3.3V+/-5%
Ra	100K+/-5%

Board ID	Rb	V AD_BID min	V AD_BID typ	V AD_BID max
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	18K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

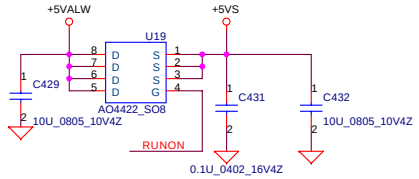
Compal Electronics, Inc.

Title: EC KB926/KB conn

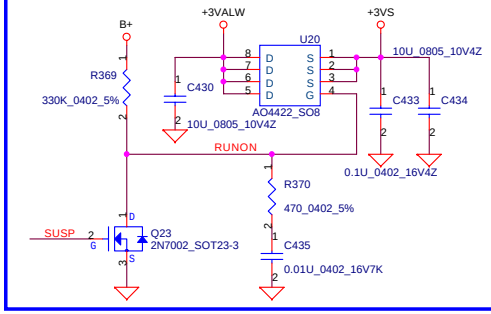
Size	Document Number	Rev
	LA-3732P	0.2

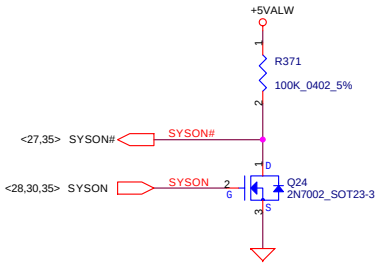
Date: Wednesday, March 14, 2007 Sheet 30 of 40

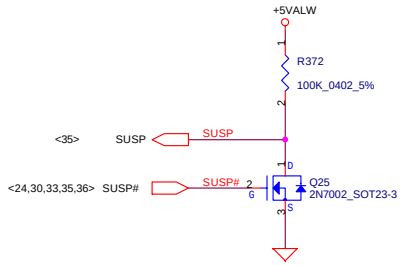
+5VALW to +5VS Transfer

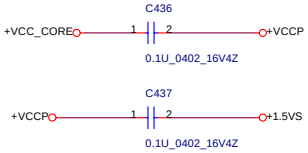


+3VALW to +3VS Transfer

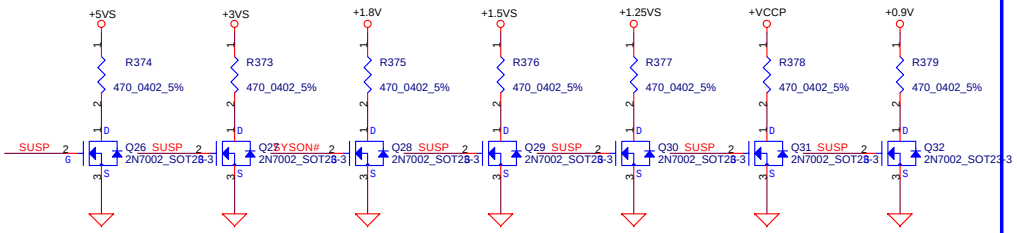


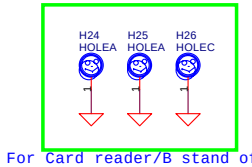




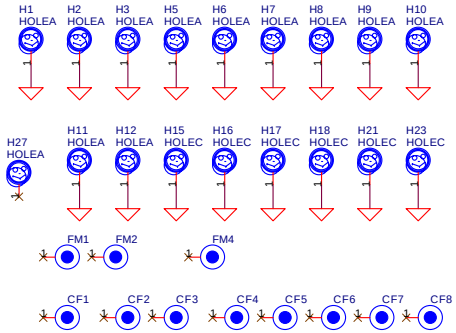


Discharge circuit





For Card reader/B stand off.



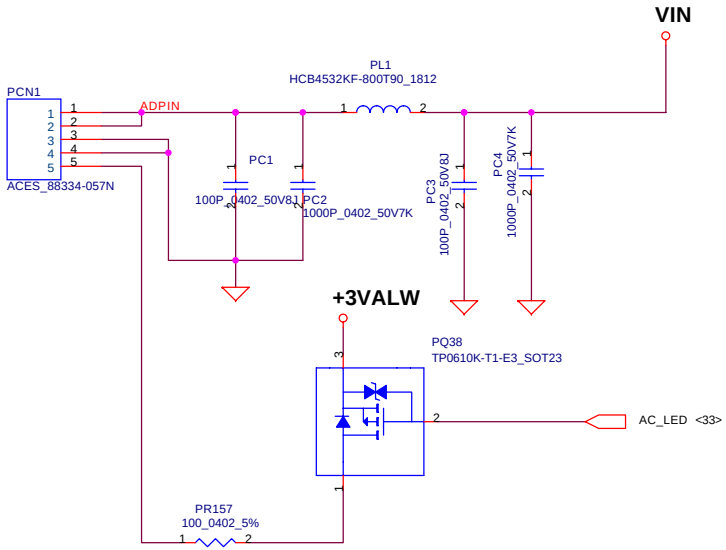
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **DC/DC Interface**

Size | Document Number: **LA-3732P** | Rev: 0.2

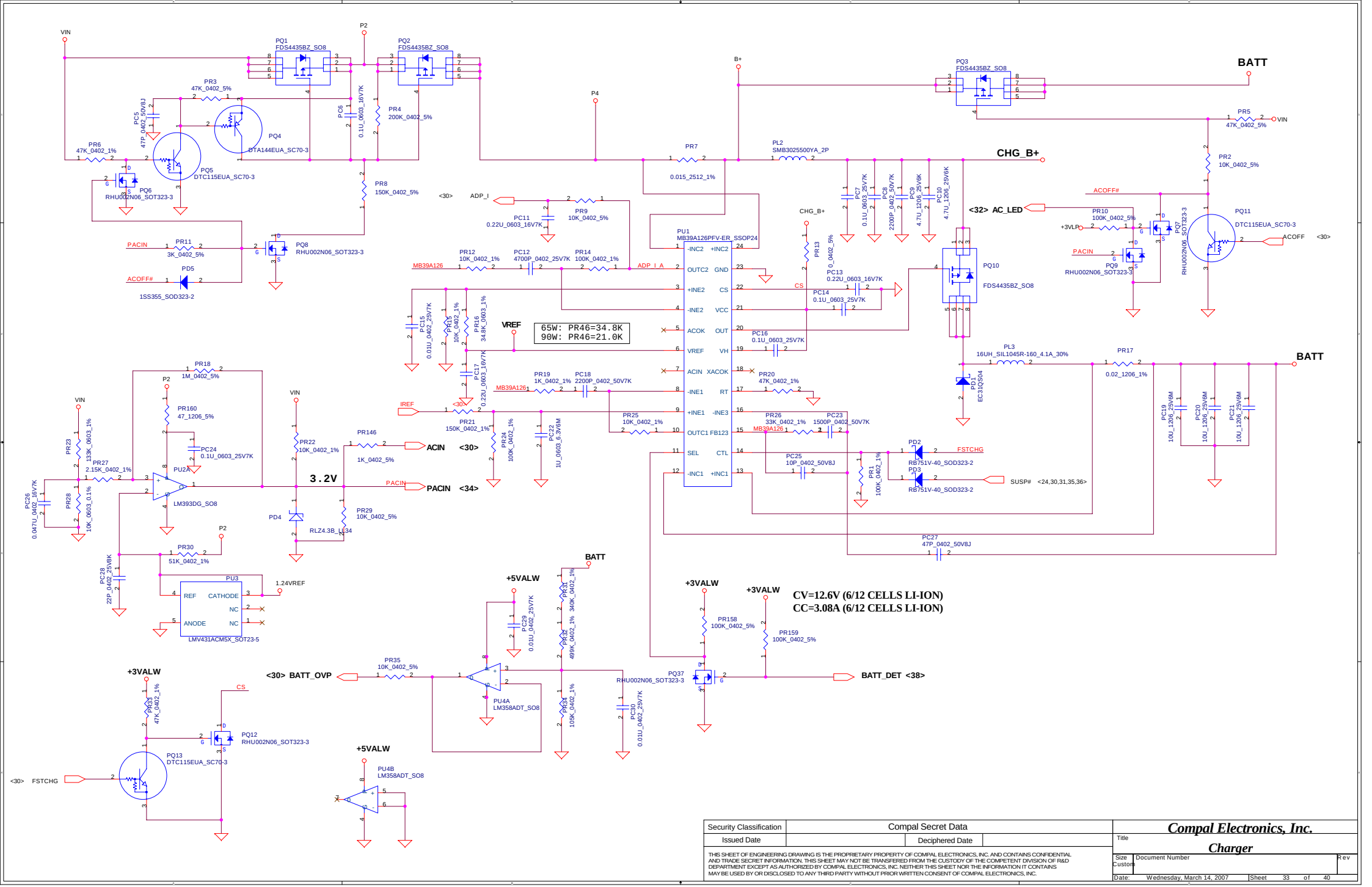
Date: Wednesday, March 14, 2007 | Sheet 31 of 40



Title: ***DC CONN***

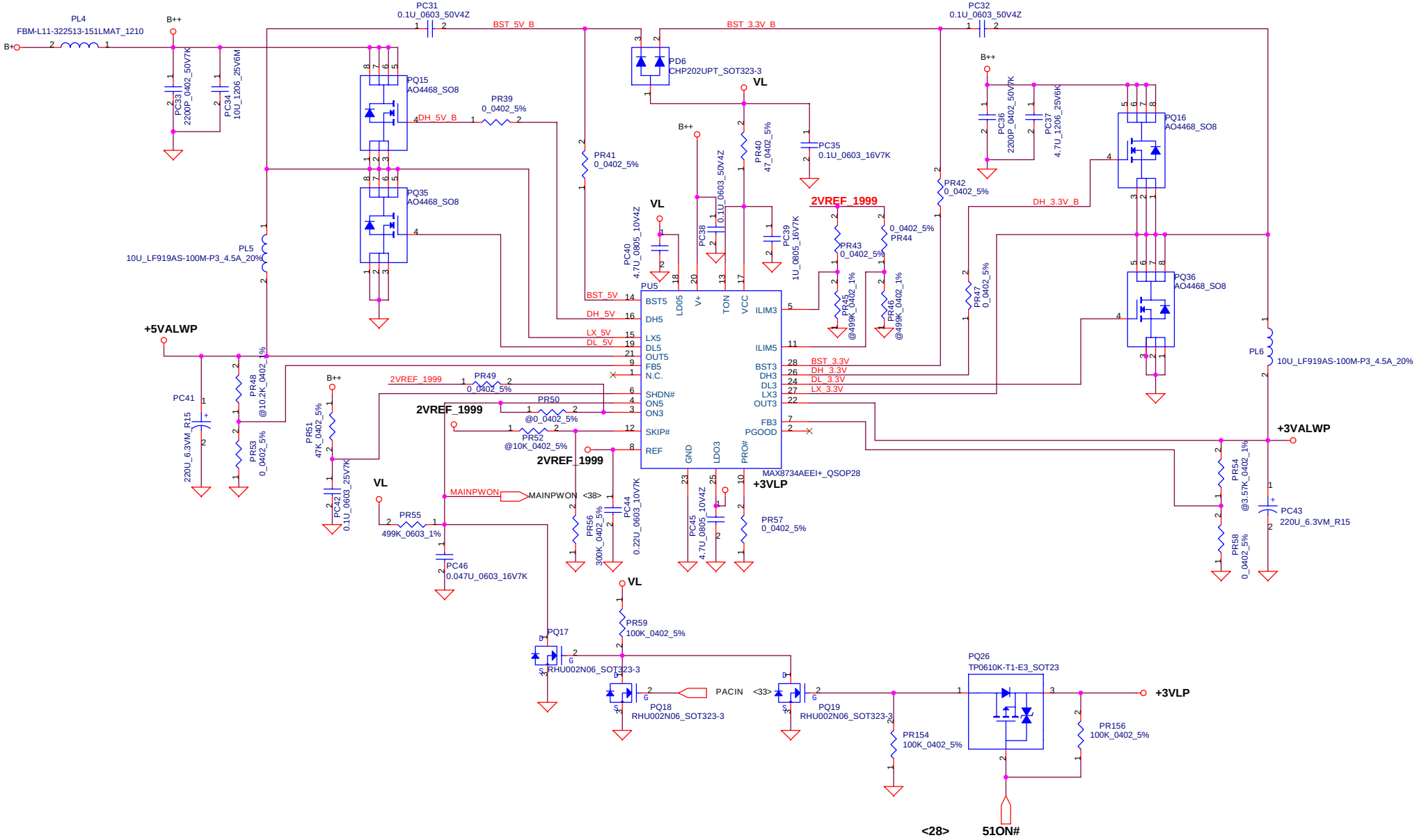
Size	Document Number	Rev
Custom	LA-3732P	

Date: Wednesday, March 14, 2007 Sheet 32 of 40



Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.		
Title: Charger		
Size: Custom	Document Number	Rev
Date: Wednesday, March 14, 2007	Sheet 33 of 40	



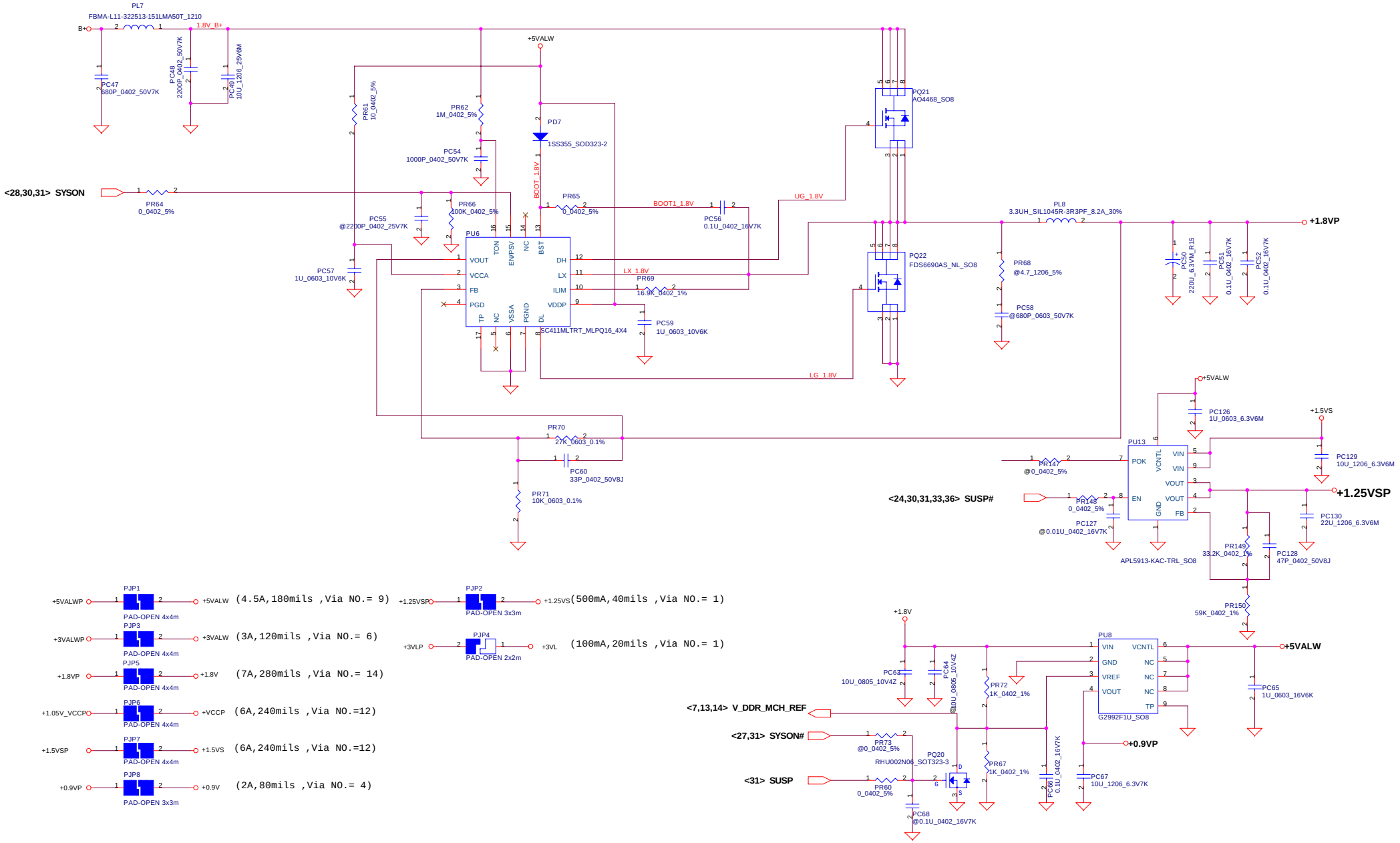
Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: **3.3VALWP / 5VALWP**

Size | Document Number | Rev

Date: Wednesday, March 14, 2007 | Sheet 34 of 40



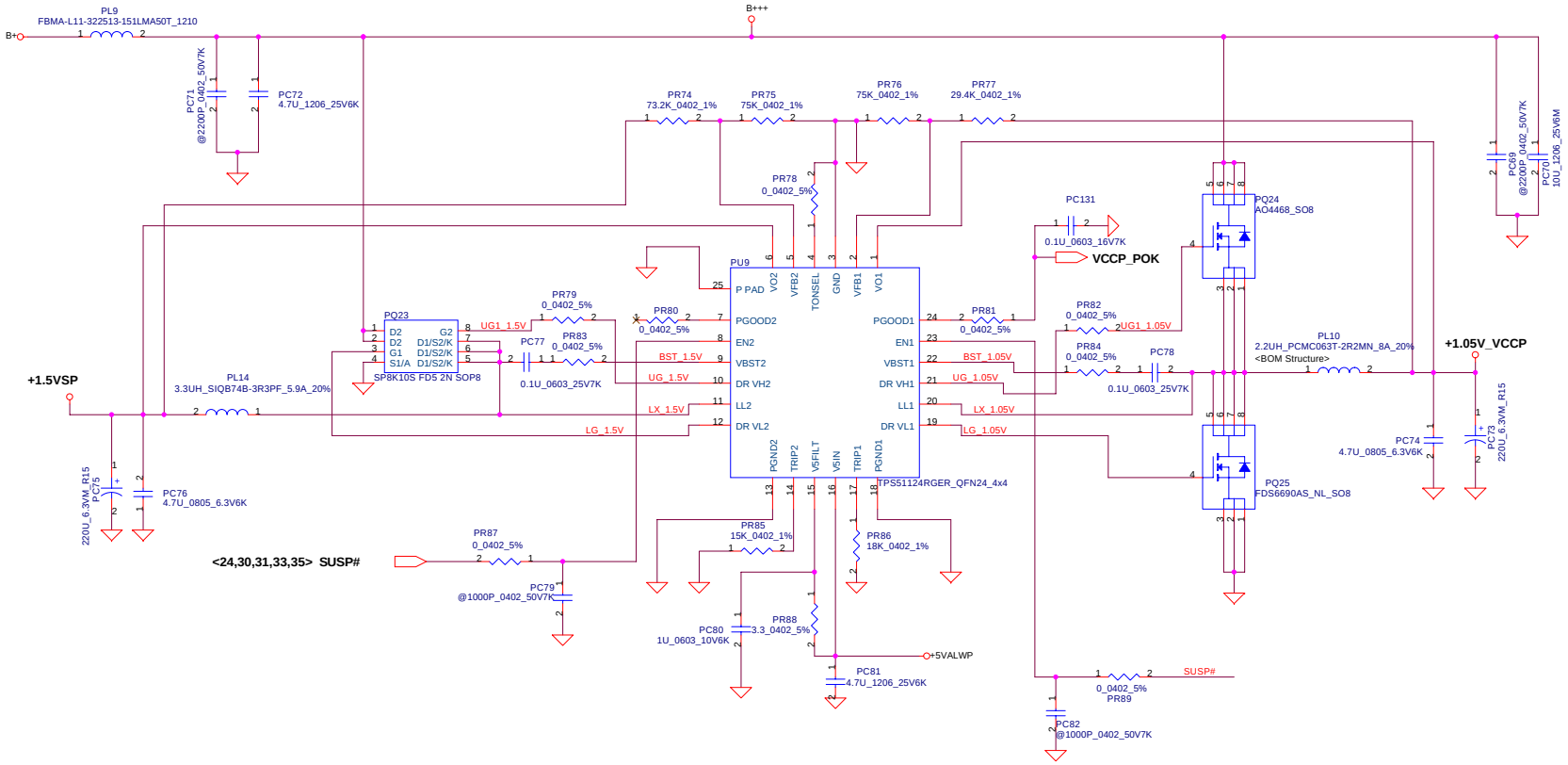
Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: **1.8VP/0.9VSP/2.5VSP**

Size	Document Number	Rev
	LA-3732P	0.2

Date: Wednesday, March 14, 2007 Sheet 35 of 40



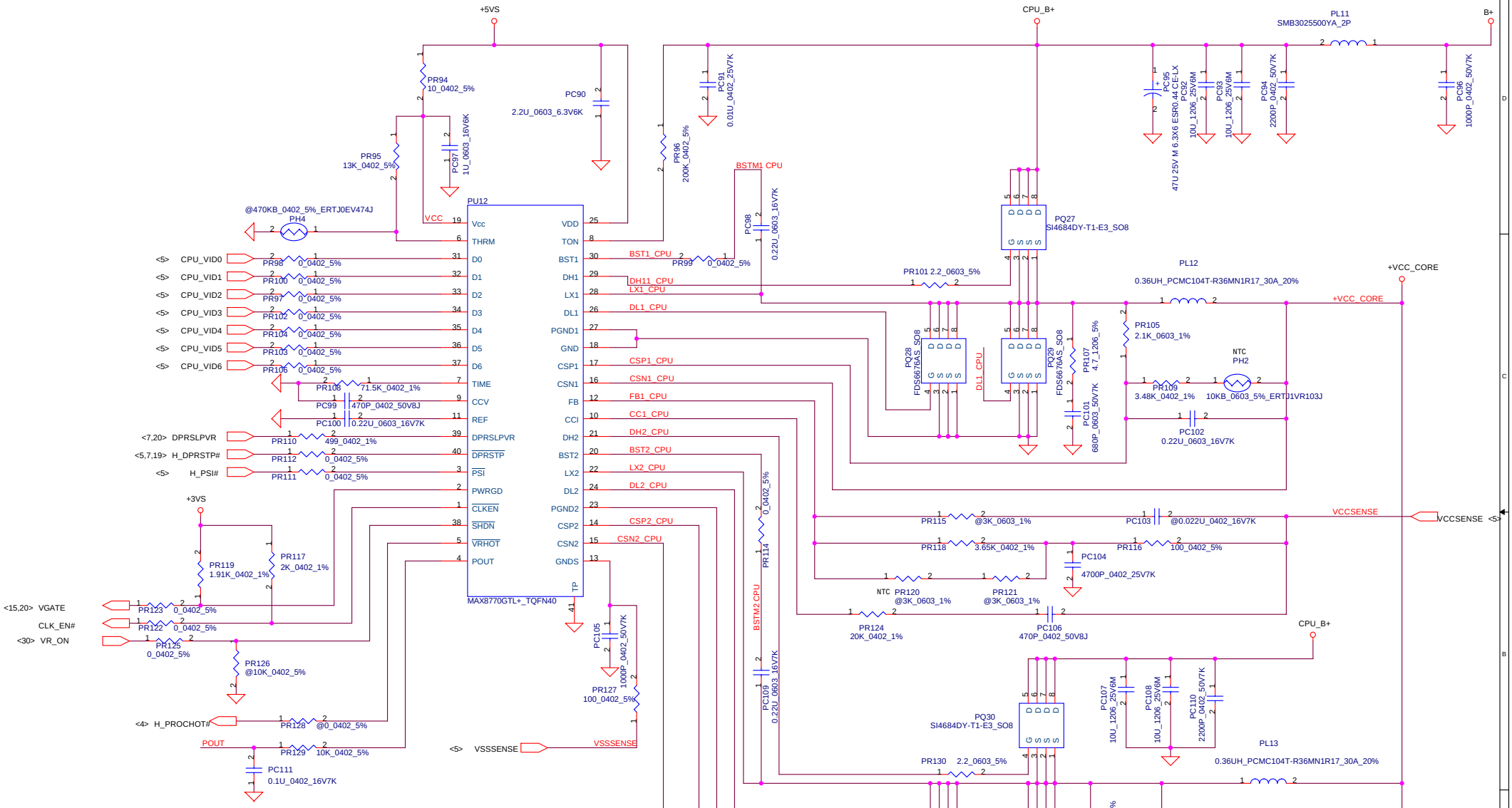
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **1.2V_VP/1.5VSP/1.05VP**

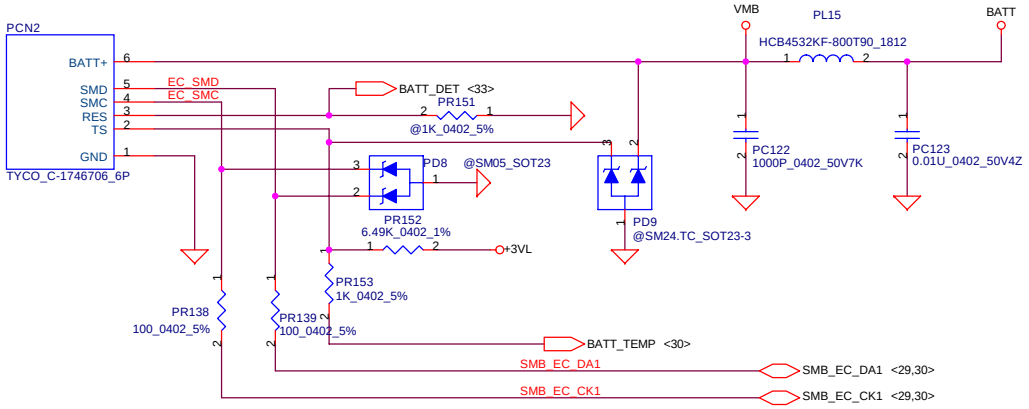
Size	Document Number	Rev
	LA-3732P	0.2

Date: Wednesday, March 14, 2007 Sheet 36 of 40

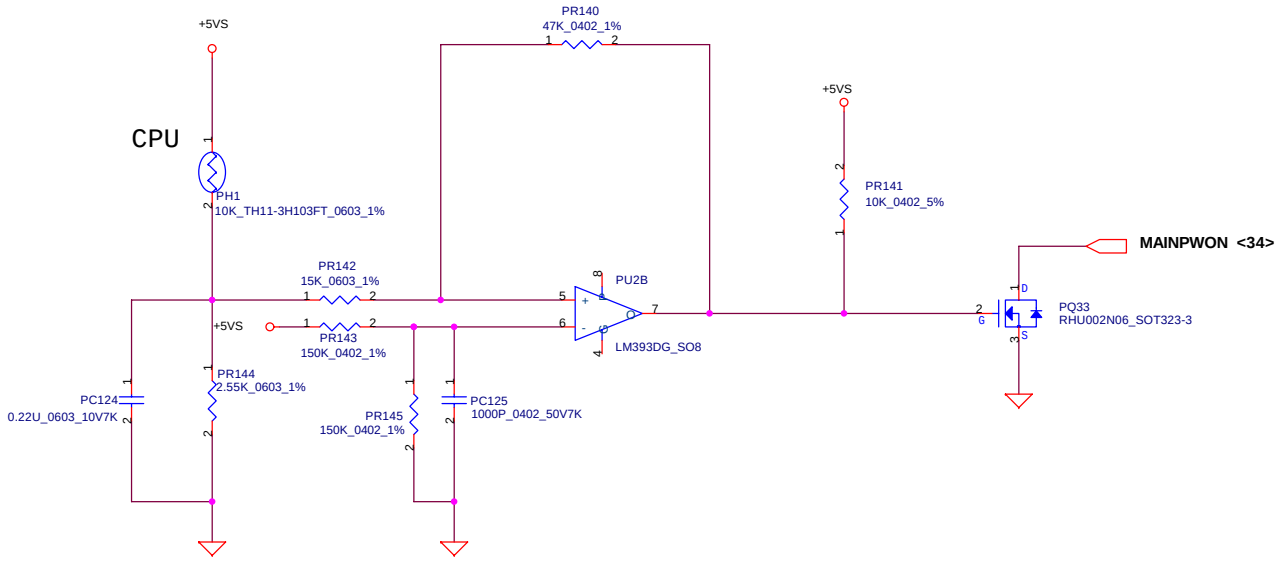


Compal Electronics, Inc.

Title	+CPU_CORE	
Size	Document Number	Rev
Custom		0.2
Date: Wednesday, March 14, 2007	Sheet 37 of 40	



PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: **BATTERY CONN**

Size	Document Number	Rev
Custom	LA-3732P	

Date: Wednesday, March 14, 2007 | Sheet 40 of 38

Item	Reason for change	PG#	Modify List	Date	Phase
1	HW request.	35	Modify 1.25VSP enable signal from SLP_S3# to SUSP#.	2/13	
2	Change PR152 from 210K to 6.49K	38	Change PR152 from 210K to 6.49K	2/13	
3	Follow Volga 2.0 design.	37	Delete PC118,PC119,PC120,PC121,PR113,PR134.	3/6	
4	For layout concern.	37	Change PC95 location behind PL11.	3/8	
5	Prevent S3 leakage issue.	33	Change PD3 pin 2 connect from EC_ON to SUSP#	3/9	
6	Prevent LMV431 will oscillate.	33	Change PR30 from 75K to 51K.	3/9	
7	Prevent LMV431 will oscillate.	33	Change PC28 from 0.022u to 22P.	3/9	
8	EMI request add CPU core snabber and gate driver use 2.2_0603	34	Change PR101&PR130 from 0_0402 to 2.2_0603	3/12	
9	Modify DC in jack LED design for energy star.	35	Add PQ105.	3/12	

Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page		Date	Phase
1	Change C117 from 220uF to 10uF.	10		2/8	DB --> SI
2	Remove R401.	19		2/5	DB --> SI
3	Change Crystal Y2 type (the same as Abita).	19		2/5	DB --> SI
4	Connect LAN_RST# from EC_RAMRST# to GND.	20		2/5	DB --> SI
5	Change ODD connector type.	22		2/13	DB --> SI
6	Change U11 power from +5VS to +5VALW.	24		2/12	DB --> SI
7	Change U11 enable signal from SLP_S3# to SUSP#.	24		2/8	DB --> SI
8	Reverse JP19 USB Connector and need to double check layout symbol.	27		2/12	DB --> SI
9	Change Power and Battery charge LED power from +3VALW to +5VALW.	28		2/8	DB --> SI
10	Change HDD LED power from +3VS to +5VS.	28		2/8	DB --> SI
11	Delete reserve component (D25 BSW2) for 14.1".	28		2/8	DB --> SI
12	Change R329, R333, R470 from 200 ohm to 470 ohm.	28		2/8	DB --> SI
13	Change R334, R339 from 200 ohm to 820 ohm.	28		2/8	DB --> SI
14	Add pull down resistor R402 (100k ohm) for SUSP#.	30		2/5	DB --> SI
15	Change C44, C49 type from DIP to SMD.	06		2/14	DB --> SI
16	Add R402 pull high resistor for LID_SW#.	30		2/14	DB --> SI
17	Add R403 pull high resistor for WL_BTN#.	30		2/14	DB --> SI
18	Delete D19.	28		2/16	DB --> SI
19	Change R300 from 10 ohm to 47 ohm and C374 from 10pF to 33pF.	24		2/16	DB --> SI
20	Delete JP27, R317, C392.	26		2/16	DB --> SI
21	Delete R297.	24		2/16	DB --> SI
22	Change RTC battery and connector.	19		2/26	DB --> SI
23	Change C413 and 414 package from 0603 to 0402.	28		2/26	DB --> SI
24	Add JP28 for USB card reader.	27		2/28	DB --> SI
25	Change R105 from 22 ohm to 0 ohm.	15		3/1	DB --> SI
26	Delete C49 and remount C46.	06		3/1	DB --> SI
27	Change JP16 and JP17 Audio Jack.	26		3/2	DB --> SI
28	Add R405.	04		3/6	DB --> SI
29	Change USB connector (JP19) type.	27		3/8	DB --> SI

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Title: HW Changed-List History-1

Size | Document Number: LA-3732P | Rev: 0.2

Date: Wednesday, March 14, 2007 | Sheet 40 of 40