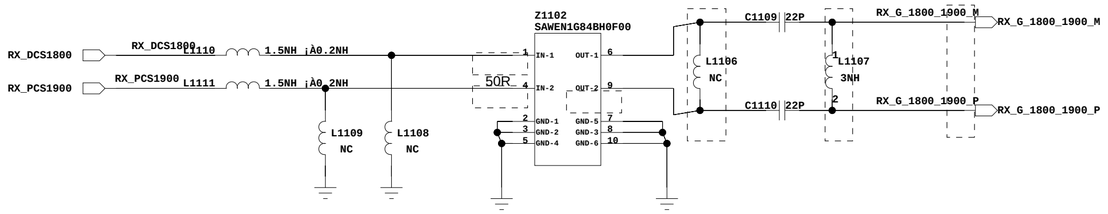
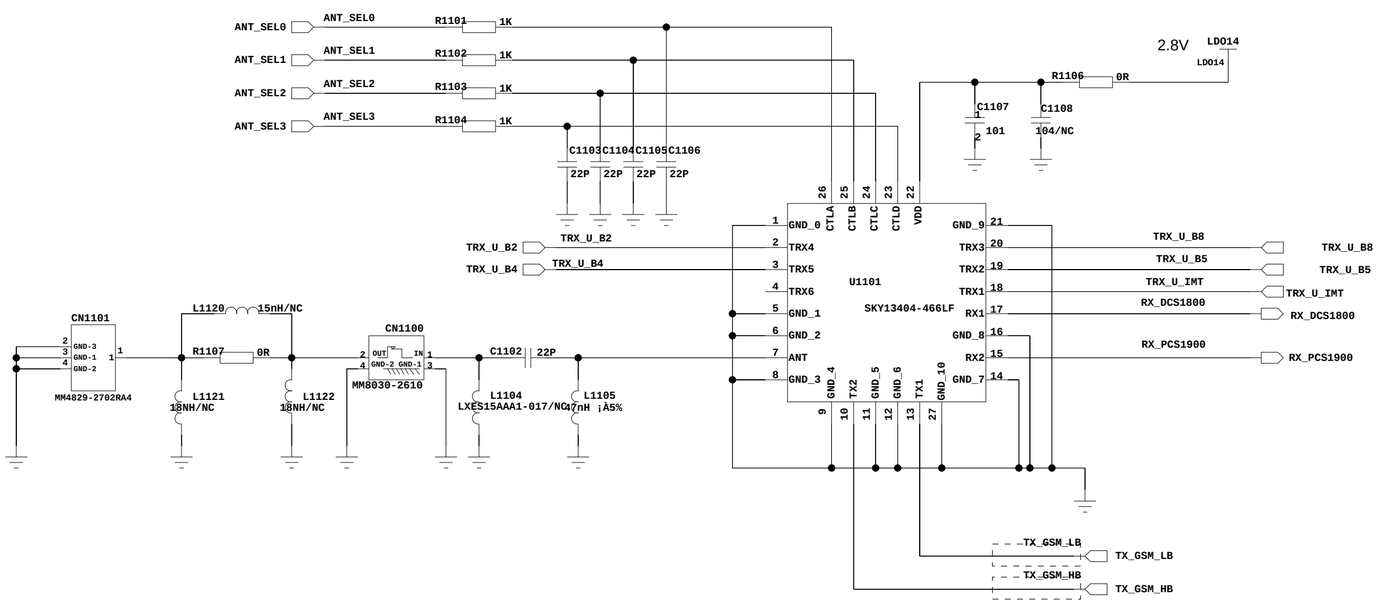
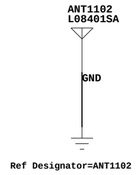
GSM/EDGE RX

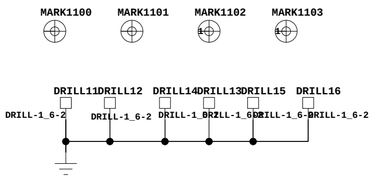


ANT SWITCH

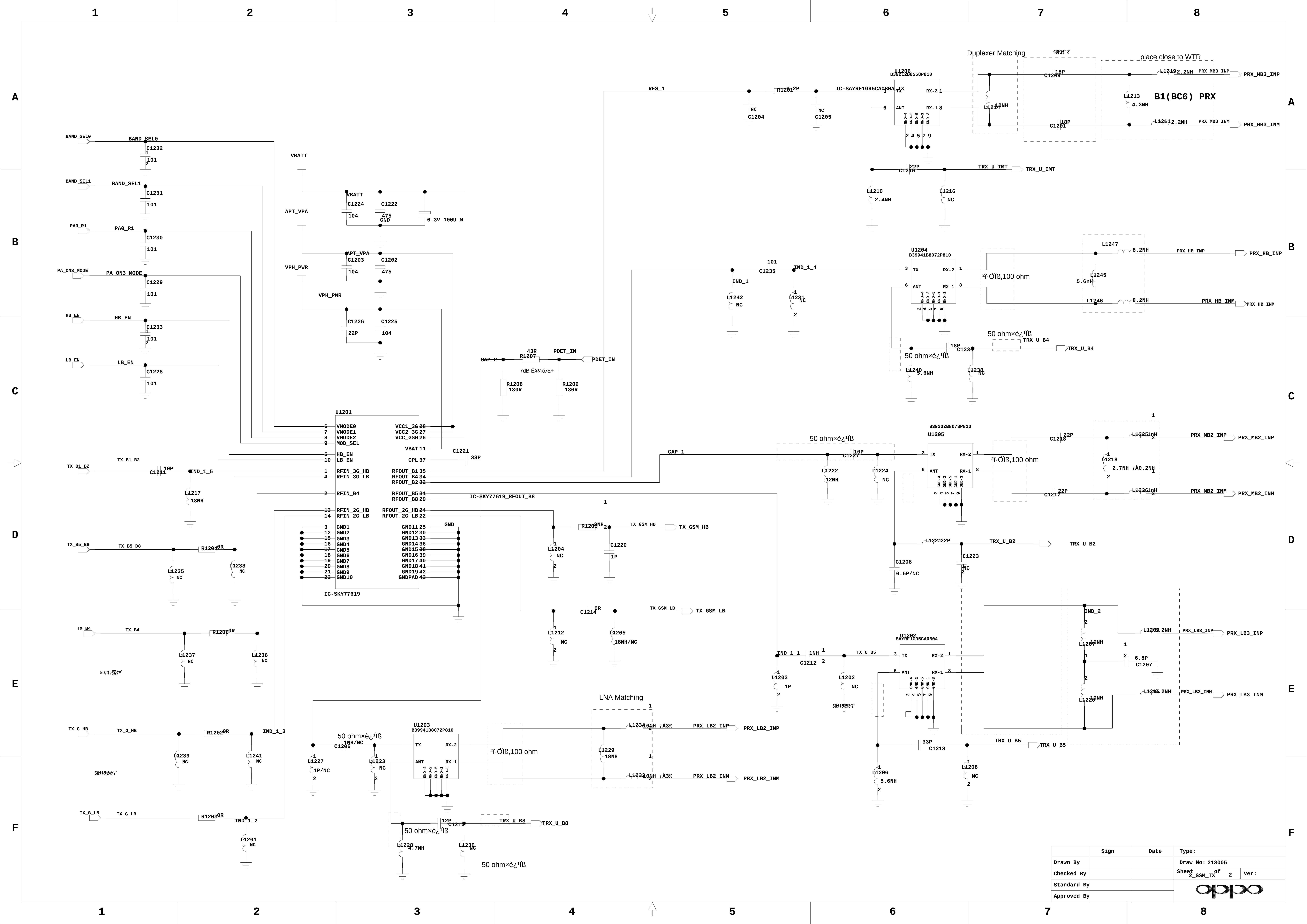




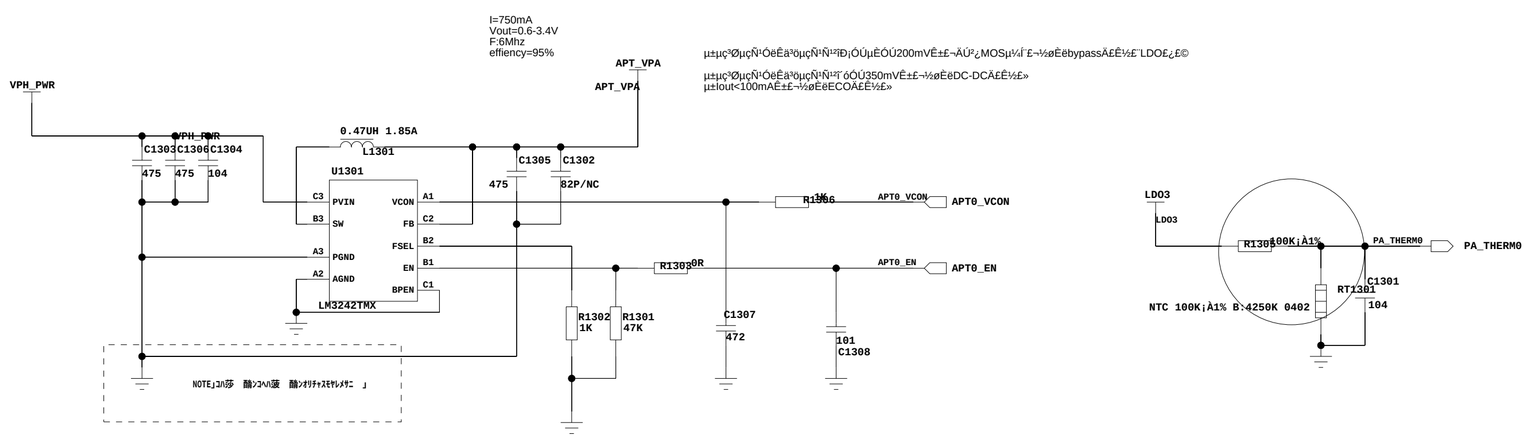
MODE	ANT_SEL0	ANT_SEL1	ANT_SEL2	ANT_SEL3
GSM850/900 (TX1)	H	H	L	L
DCS1800/PCS1900 (TX2)	H	L	L	L
IMT_(TRX1)	L	L	H	L
U_B5_ (TRX2)	H	L	H	L
U_B8_(TRX3)	H	H	H	L
U_B2_(TRX4)	H	L	H	H
RX_PCS1900_(RX2)	L	H	L	L
RX_DCS1800_(RX1)	L	H	H	L
U_B4_(TRX5)	H	H	H	H



	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet of 2 Ver:
Standard By			
Approved By			



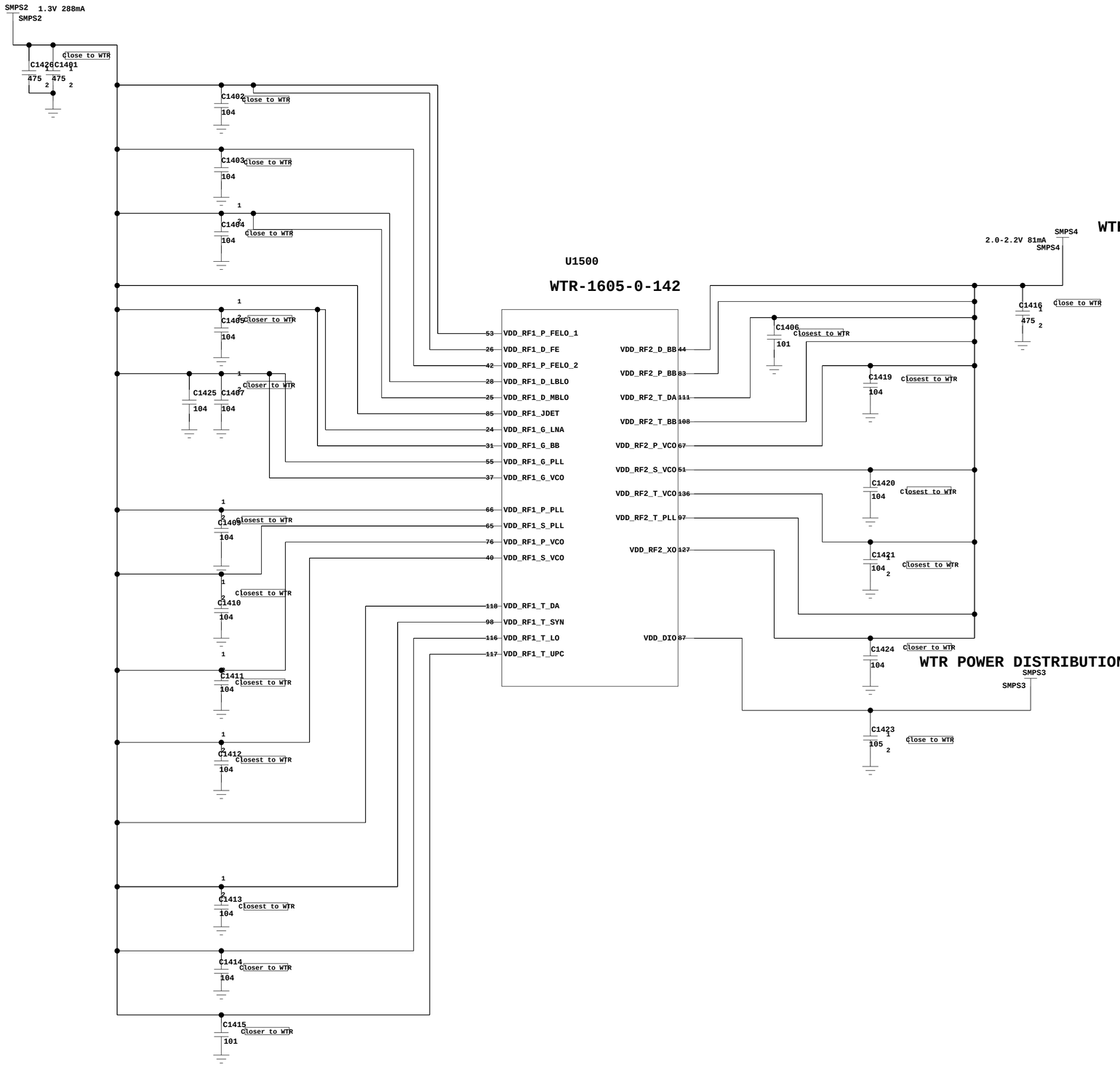
Duplexer Matching
place close to WTR
B1(BC6) PRX
U1206
IC-SAYRF1G95CA0B0A_TX
RES_1
R1201
C1204
C1205
C1209 18P
C1201 18P
L1214 10NH
L1213 4.3NH
L1219 2.2NH
L1211 2.2NH
PRX_MB3_INP
PRX_MB3_INM
TRX_U_IMT
C1219 22P
L1210 2.4NH
L1216 NC
BAND_SEL0
BAND_SEL1
PA0_R1
PA_ON3_MODE
HB_EN
LB_EN
C1232 101
C1231 101
C1230 101
C1229 101
C1233 101
C1228 101
VBATT
APT_VPA
VPH_PWR
C1224 104
C1222 475
6.3V 100U M
C1203 104
C1202 475
C1226 22P
C1225 104
CAP_2
R1207 43R
PDET_IN
7dB
R1208 130R
R1209 130R
U1204
B39941B8072P810
IND_1_4
C1235 101
IND_1
L1242 NC
L1231 NC
L1247 8.2NH
L1245 5.6nH
L1246 8.2NH
PRX_HB_INP
PRX_HB_INM
50 ohm
100 ohm
C1234 18P
TRX_U_B4
L1240 5.6NH
L1238 NC
U1201
VMODE0
VMODE1
VMODE2
MOD_SEL
HB_EN
LB_EN
RFIN_3G_HB
RFIN_3G_LB
RFIN_B4
RFIN_2G_HB
RFIN_2G_LB
VCC1_3G
VCC2_3G
VCC_GSM
VBAT
CPL
RFOUT_B1
RFOUT_B4
RFOUT_B2
RFOUT_B5
RFOUT_B8
RFOUT_2G_HB
RFOUT_2G_LB
GND1 … GND10
GND11 … GND19
GNDPAD
IC-SKY77619
IC-SKY77619_RFOUT_B8
C1221 33P
TX_B1_B2
C1211 10P
IND_1_5
L1217 18NH
TX_B5_B8
R1204 0R
L1235 NC
L1233 NC
TX_B4
R1206 0R
L1237 NC
L1236 NC
TX_G_HB
R1202 0R
IND_1_3
L1239 NC
L1241 NC
TX_G_LB
R1203 0R
IND_1_2
L1201 NC
CAP_1
U1205
B39202B8078P810
C1227 10P
L1222 12NH
L1224 NC
C1218 22P
C1217 22P
L1225 1nH
L1226 1nH
L1218 2.7NH
PRX_MB2_INP
PRX_MB2_INM
R1205 3NH
TX_GSM_HB
L1204 NC
C1220 1P
C1214 0R
TX_GSM_LB
L1212 NC
L1205 18NH/NC
L1221 22P
TRX_U_B2
C1208 0.5P/NC
C1223 NC
U1202
SAYRF1G95CA0B0A
IND_1_1
C1212 1NH
TX_U_B5
L1203 1P
L1202 NC
IND_2
L1207 10NH
L1220 10NH
C1207 6.8P
L1209 8.2NH
L1215 8.2NH
PRX_LB3_INP
PRX_LB3_INM
C1213 33P
TRX_U_B5
L1206 5.6NH
L1208 NC
LNA Matching
U1203
B39941B8072P810
C1206 1NH/NC
L1227 1P/NC
L1223 NC
L1234 10NH
L1229 18NH
L1232 10NH
PRX_LB2_INP
PRX_LB2_INM
C1210 12P
TRX_U_B8
L1228 4.7NH
L1230 NC
Sign
Date
Type:
Drawn By
Draw No: 213005
Checked By
Sheet 2 of 2
GSM_TX
Ver:
Standard By
Approved By
oppo



	Sign	Date	Type:
Drawn By			Draw No: 213005
Checked By			Sheet of Ver:
Standard By			
Approved By			

3_TD_B34339_4G

WTR POWER DISTRIBUTION 1.3V

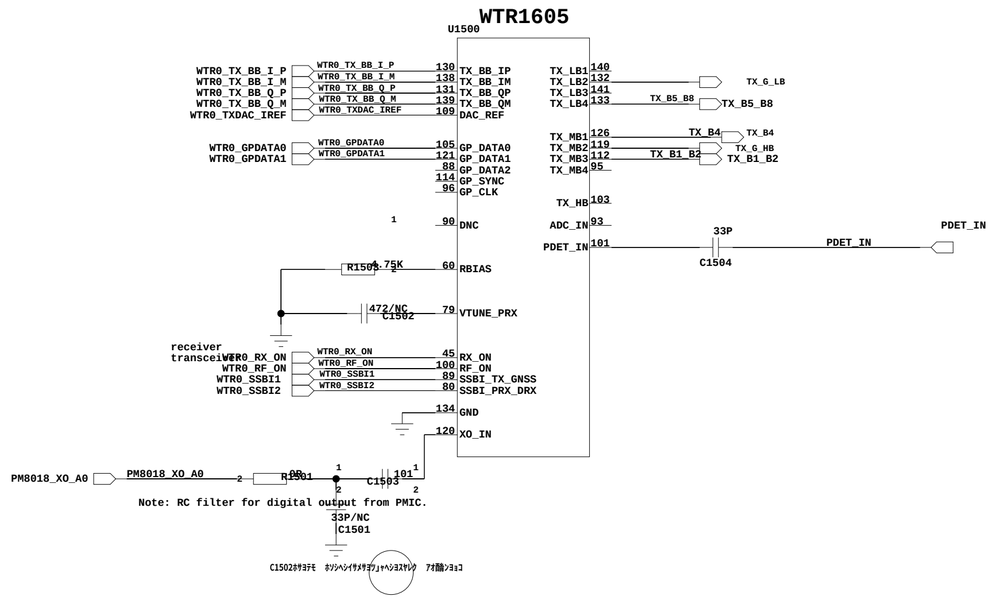


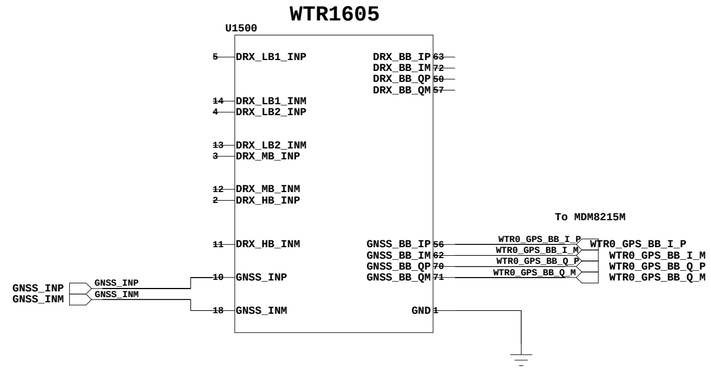
WTR POWER DISTRIBUTION 2.05V(Rev.B)

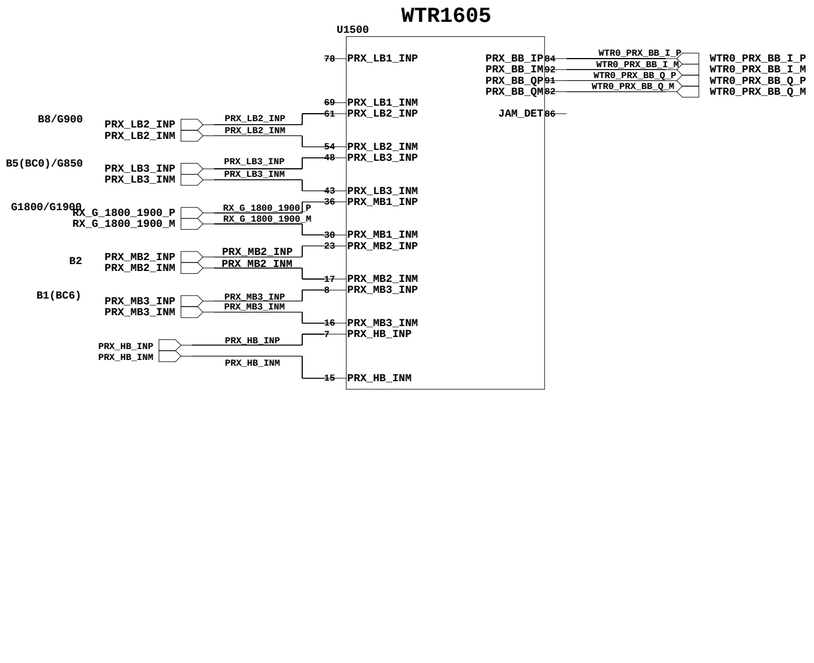
WTR POWER DISTRIBUTION 1.8V

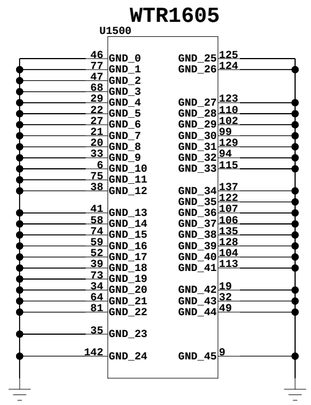
	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet of
Standard By			6_WTR1605L_POWER
Approved By			

oppo



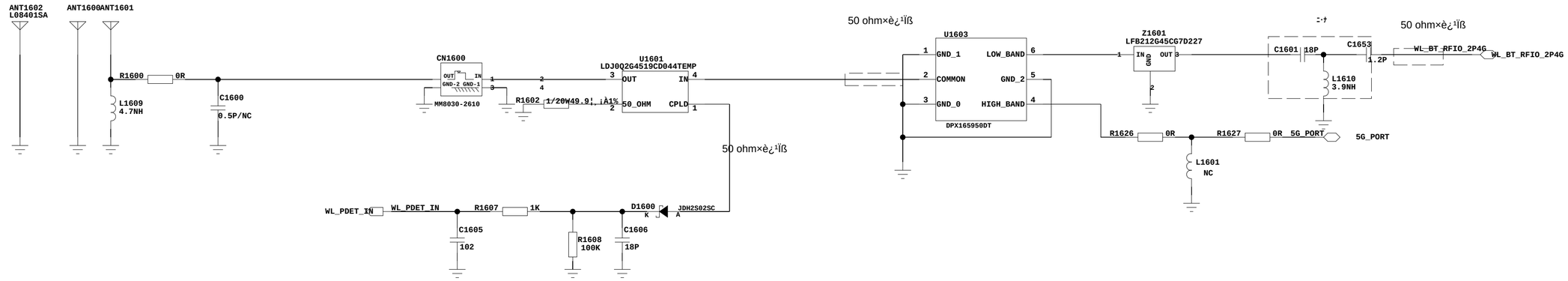


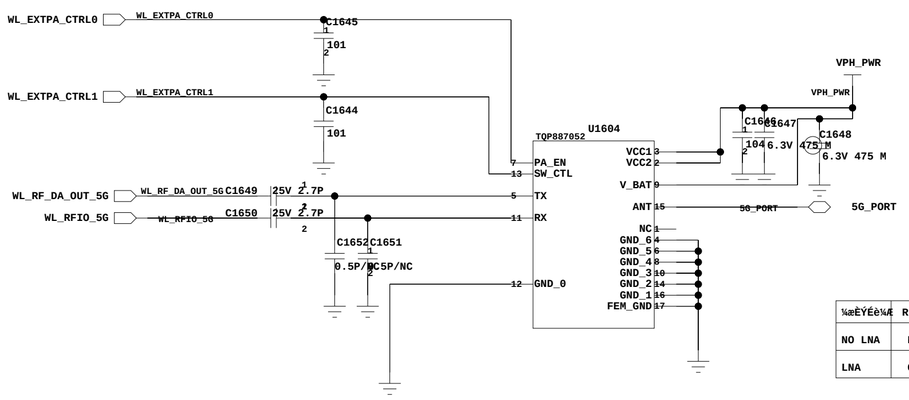




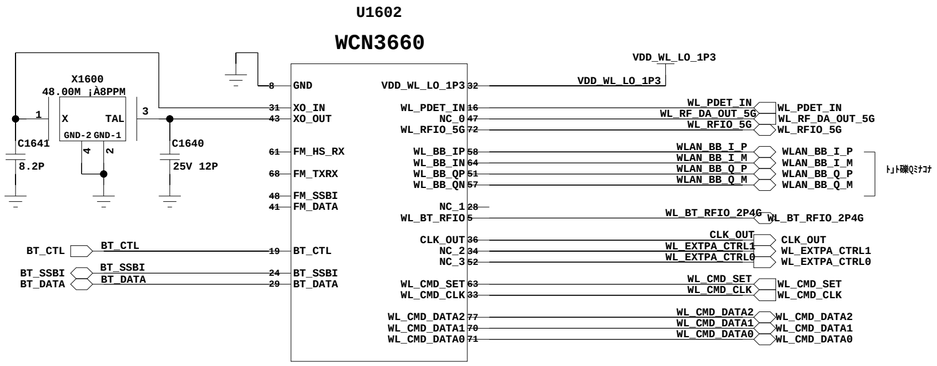
	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet of Ver:
Standard By			7_WTR1605L_RF
Approved By			

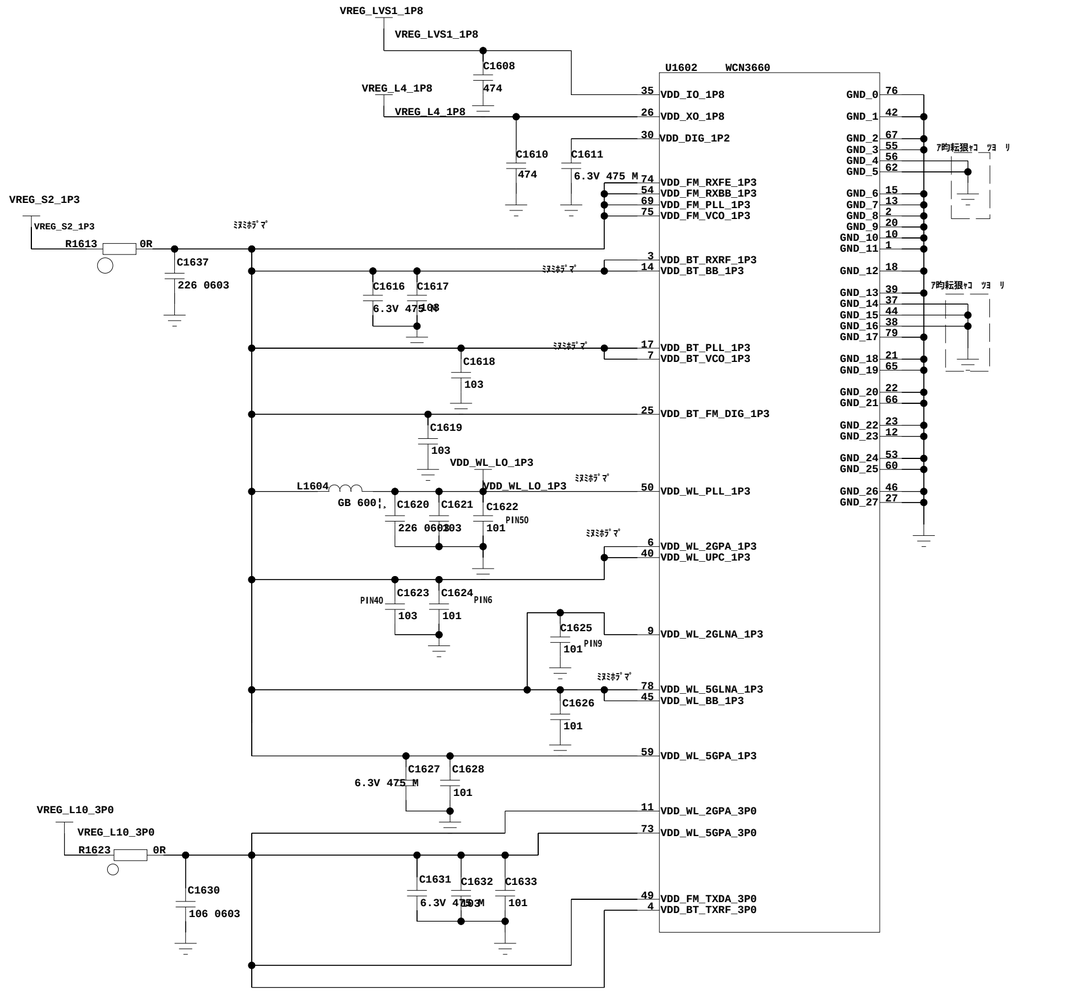
WIFI+BT





¼æÈÝÉè¼Æ	R1630	R1631	R2028	R2029
NO LNA	NC	OR	NC	OR
LNA	OR	NC	OR	NC





If 2.4 GHz WLAN spurs are observed around 2.6 to 2.7 GHz,
replace R1612 with 20 nH inductor.

	Sign	Date	Type:
Drawn By			Draw No: 213005
Checked By			Sheet of 6_WIFI_BT2 Ver:
Standard By			
Approved By			

NFC

note1:ｵ認ﾘｵ酳ﾅﾝ撃篁ﾌﾄｸﾓﾐﾖ時ﾚｷﾀﾖｵｵ酳ｹﾅ　ﾃﾋﾄｸｸ　ﾅﾏﾞﾖｵｻｻﾝﾐ　ﾅｵ
ｸﾃﾃﾌﾄｸﾊｽ　ｹﾄﾌｭｷﾓ/VEN_MONｽｷｵﾄｵ酳ｽﾗﾆﾌｯﾁﾗﾋ　ｨ｣ｻ

note2:Hard ware design guide/ﾏｲｸﾛﾝﾍﾝｽｲﾒ鯣BATﾍﾋ　ｵ酳ﾝｺ±1UF;

NFC_ENABLE
NFC_ENABLE
VBATT
VBATT
VREG_L23_1P8_NFC
VREG_L23_1P8_NFC
R1717
1K
Q1701
C1728
104
R1701
1M
PN65O
U1701
RESET/HW Power down
VEN
VEN Enable/disable LDO
TP1703
D8 VBAT
F8 VBAT2
B7 VEN
D1 VCO_VDD
C1 VDHF
C1729 C1730 LDO6
104 106 0603
VREG_L23_1P8_NFC
VREG_L23_1P8_NFC
change by xyl
A1 PMUVCC
A4 PVDD
G7 PMU_GND
F6 VSS
C1721
105
G1 AVDD_IN
F2 AVDD_OUT
C1727 104
A5 DVDD
G8 TVDD
Transmitter supply:2.7-3.3V
C1722 105
F7 TVDD_OUT
E8 VEN_MON
ON BAT_MONITOR
OFF BAT_MONITOR
VEN_MON
E4 IFO
GND
B4 IF1
Host wake up PN544
host interface
RS232/rfu/I2C/SPI
I2C1_DATA_NFC
I2C1_DATA_NFC
C4 IF2
I2C1_CLK_NFC
I2C1_CLK_NFC
D4 IF3
to earse host interface communication
NFC_IRQ
NFC_IRQ
A3 IRQ
LDO6
TP1704
R1708
SE Selection
C1723 104
C8 SVDD
R1709 0R/NC
E7 SIGIN
0R NC
GND
D7 SIGOUT
UICC Connection
SIM_VCC
SIM_VCC
R1707 0R
B8 SIMVCC
SIM_SWP
SIM_SWP
C7 SWIO
UICC_TF
D6 EXT_SW_CTRL
TX1
TX1
H6 TX1
TX2
TX2
H7 TX2
RX
RX
H4 RX
antenna matching circuit connection
NFC_VMID
NFC_VMID
G4 VMID
ANT1
ANT1
G5 ANT1
ANT2
ANT2
G6 ANT2
HT80C51 Core
Code Mem:128KB ROM,44KB EEPROM
Data Mem:5KB SRAM,8KB EEPROM
note3:GPIO4Y//ｽｷﾃﾗﾋﾚﾘﾖﾆPN5441　ｱｷﾘﾄｶﾉﾊ
ÓÀÒÙ,ùÐÀPN544ÀíÀæµÁfirmware.

VREG_L23_1P8
R1716 0R
VREG_L23_1P8_NFC
C1704
104
VREG_L23_1P8_NFC
TEST1 A6
TEST2 B6
TEST3 C5
TEST4 D5
TEST5 E5
TEST6 H2
TEST7 E3
TEST8 G2
TEST9 G3
TEST10 C6
GPIO0 E3
GPIO1 D3
GPIO2 C3
GPIO3 C2
GPIO4 B1
GPIO5 B2
GPIO6 B3
GPIO7 A1
RFU1 A7
RFU2 E6
RFU3 H1
TP1701
Download mode
NFC_UPDATE
NFC_UPDATE
R1715 0R/NC
Interface Selection-I2C
IFSELO A2
IFSEL1 F4
IFSEL2 F5
TVSS2 H8
AVSS1-2 H5
PVSS B5
DVSS D2
AVSS2 H3
AVSS1-2 E2
XTAL1 E1
XTAL2 F1
VREG_L23_1P8_NFC
host interface setting
X1701
27.12M ¡Ã30PPM
TAL
GND-1 GND-2
C1720
10P
C1703
10P
PN544N\PN65N\PN65O ｼ貶ﾝﾉ需ﾆ
change by xyl
VREG_L23_1P8_NFC
R1713 0R/NC
R1714
0R
R1710
0R/NC
RX
RX
C1726 102 R1711 2.2K
R1712
1K
NFC_VMID
NFC_VMID
C1713 104
TX1
TX1
L1702 560NH ¡Ã5% 100mA
C1725
181
C1724
181
C1711 4.7P
C1712 22P
C1708 6.8
C1707 22P
C1706 22P
C1705 6.8
R1704 0R
ANT1704
TX2
TX2
L1701 560NH ¡Ã5% 100mA
C1710 4.7P
C1709 22P
R1705 0R
ANT1701
C1718 56P/NC
C1702 47P
C1701 47P
C1731 56P/NC
ANT1
ANT1
R1706
0R/NC
ANT2
ANT2

change by xyl

¼æÈÝÉè¼Æ	R1709	R1715	R1713	R1710	R1714
PN544 C2/C3	0R	0R	0R	0R	NC
PN65N	NC	NC	0R	0R	NC
PN65O/O+	NC	NC	NC	NC	0R

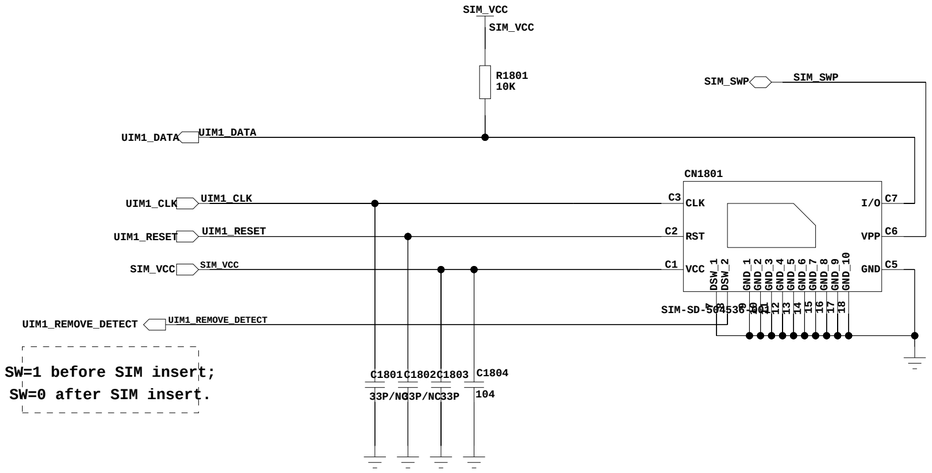
GPS

ANT1703 ANT1702
R1703 0R
NC
L1705
NC
L1703
L1708
9.1NH
Z1701
IN
GND-1
GND-2
OUT
GND-3
SAFEA1G58KA0F00
C1714 22P
L1710 5.6NH
C1716
22P/NC
U1702
RF_IN
GND-2
GND-1
RF_OUT
VCC
ENABLE
BGU7005
C1715 22P
LDO5
C1717
102
TP1702
TP-0.5
GPS_EXT_LNA_EN
GPS_EXT_LNA_EN
Z1702
IN
OUT1
OUT2
GND-1
GND-2
SAFEA1G58FB0F00
²ƒ·ÖÏß,100 ohm
L1706 9.1NH
GNSS_INM
GNSS_INM
C1719
1.2P
L1707 9.1NH
GNSS_INP
GNSS_INP

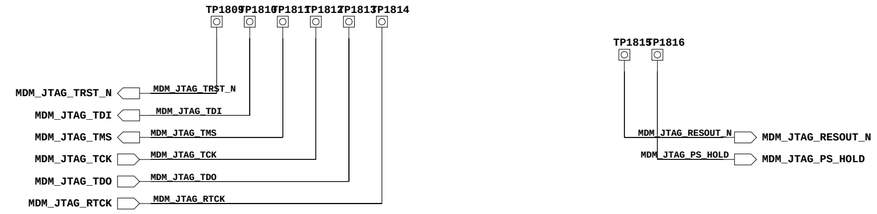
	Sign	Date	Type:
Drawn By			Draw No: 213005TD
Checked By			Sheet 7_NFC_GPS of 11 Ver:
Standard By			
Approved By			

oppo

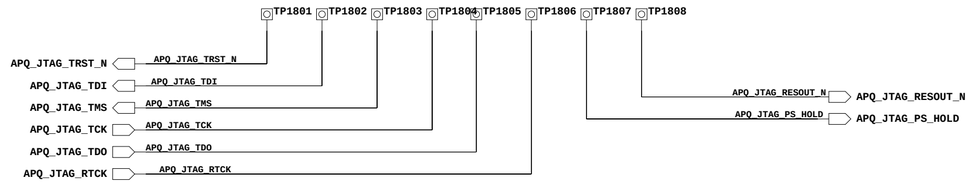
SIM CARD



MDM JTAG DEBUG

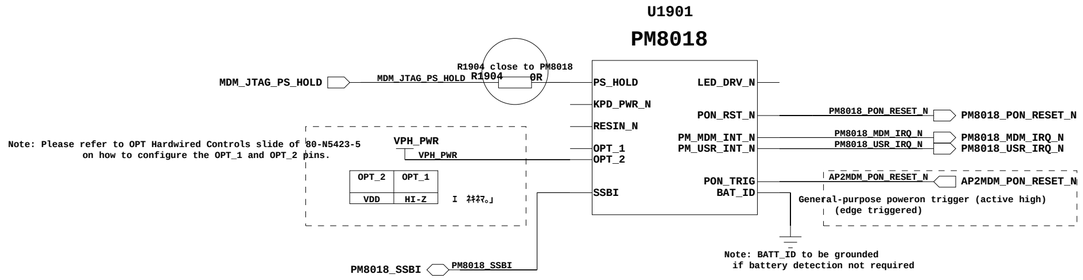


APQ8064 JTAG DEBUG

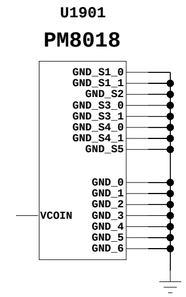


	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 28 of 28 Ver:
Standard By			
Approved By			

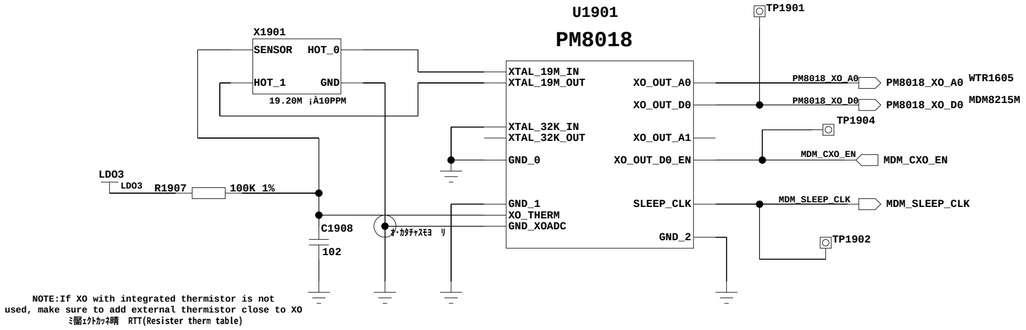
PM8018 : CONTROL



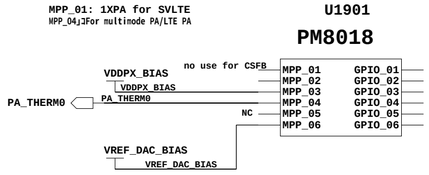
PM8018 : GND



PM8018 : CLOCKS



PM8018 : GPIO AND MPPS

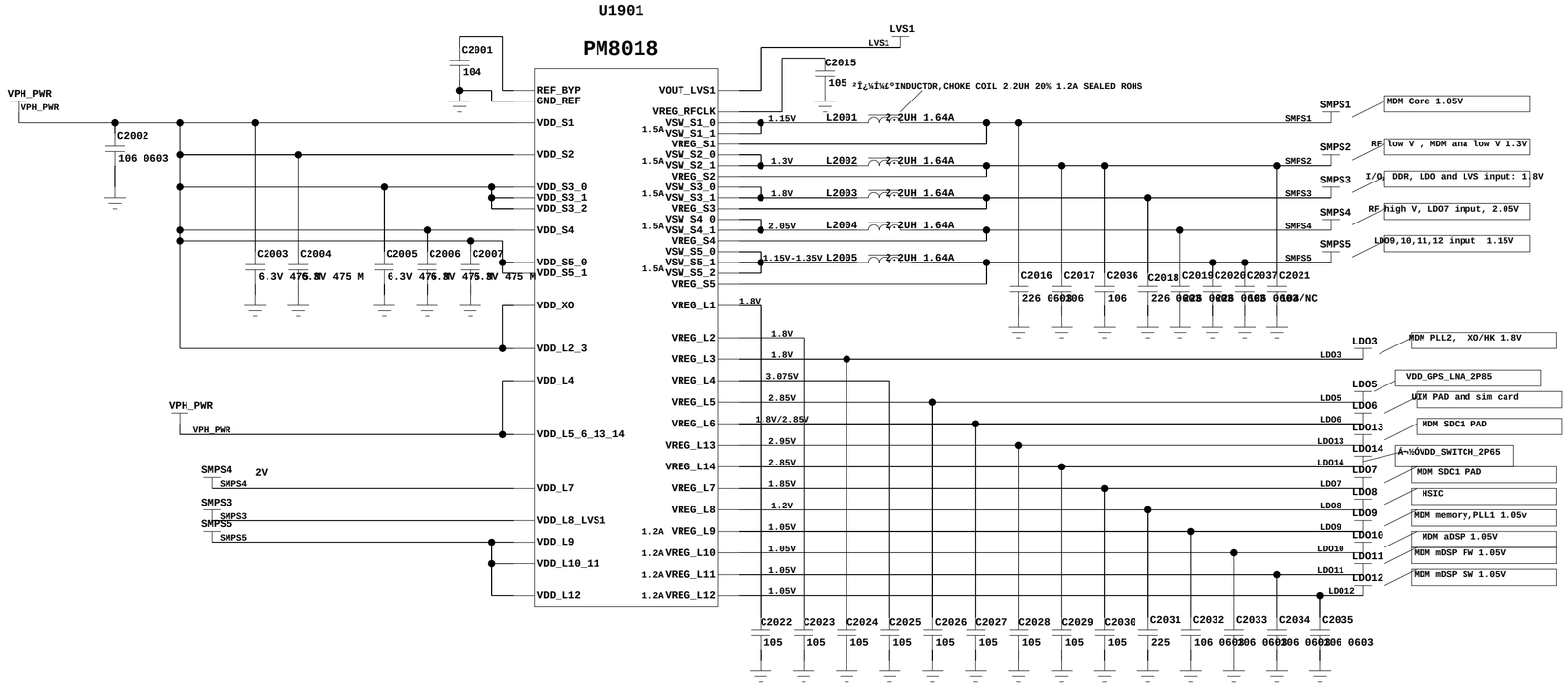


PM MPP/GPIO PADS
LDO6 1.8/2.85V
LDO5 1.8/2.85V
SMPS3 1.8V
LDO14 2.85V
LDO2 1.8V
LDO4 3.075V
VDD_L4 VBATT

	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 30 of 28 Ver:
Standard By			
Approved By			

oppo

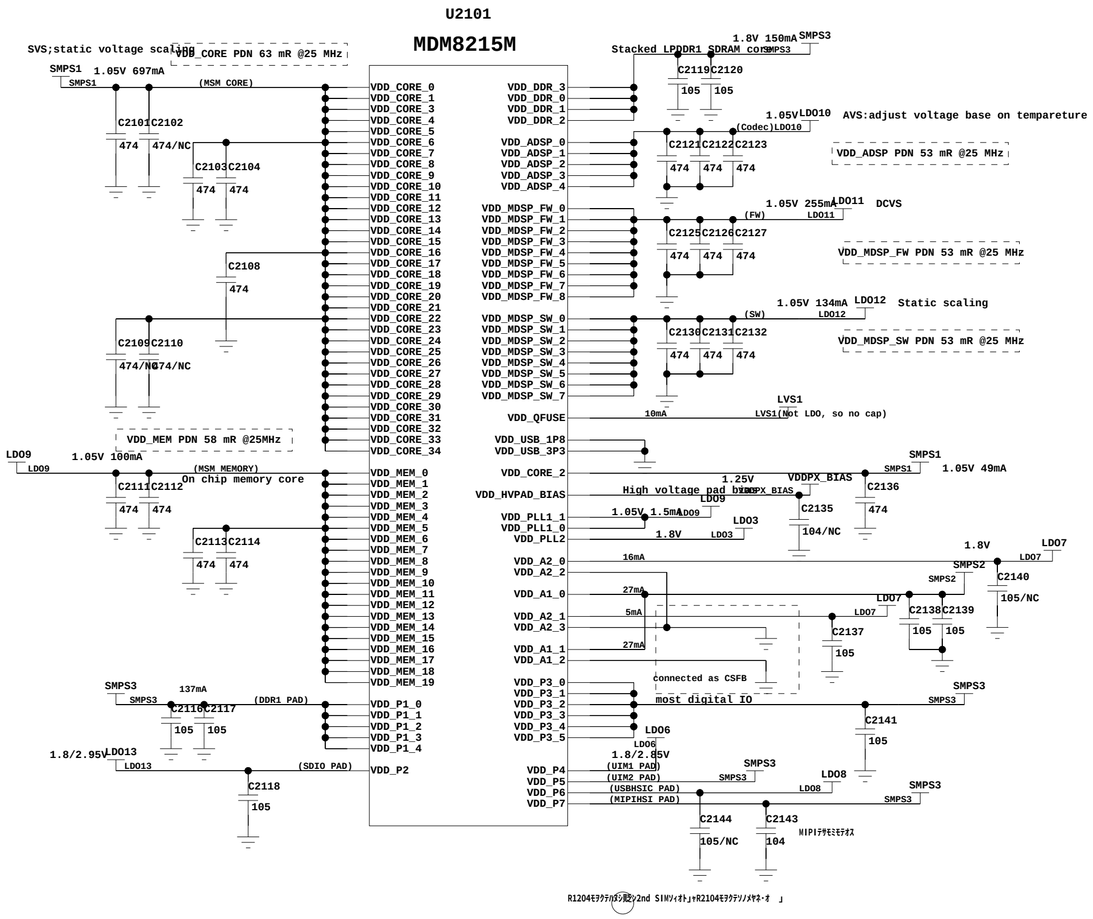
PM8018 REGULATORS

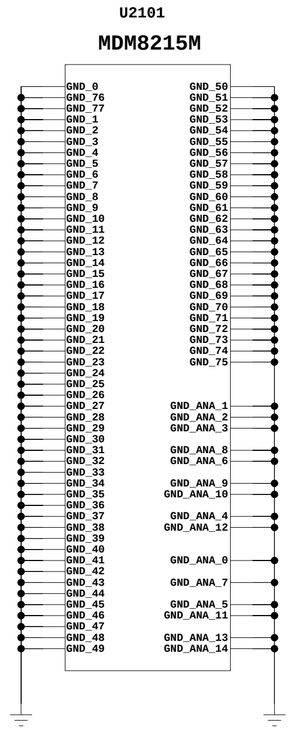


NOTE:
For expected voltages on output regulators S1, S5, L9, L10, L11 and L12, please refer to Section 3.2.2 in 80-N5576-47 document (the voltages are not static and are subject to voltage scaling).

	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 10 of 10 Ver:
Standard By			
Approved By			

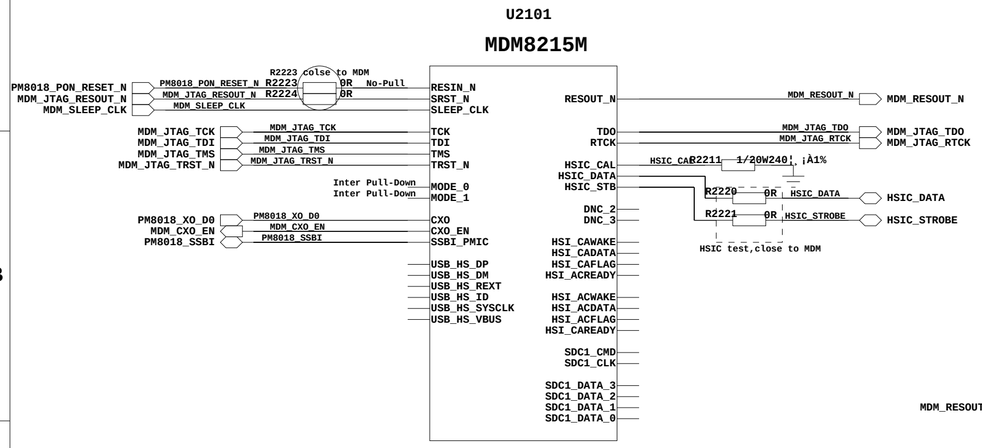
MDM8215M : POWER AND GND





	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 6 of 6 Ver:
Standard By			
Approved By			

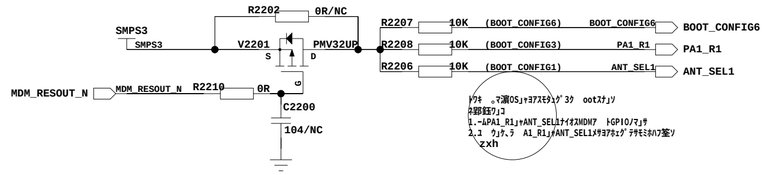
MDM8215M: DIGITAL



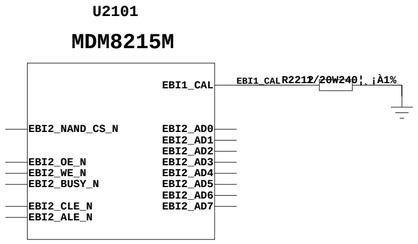
BOOT_CONFIG[5:0]	BOOT_CONFIG[6] = 1 = fast boot
0x000000	Emergency boot-try NAND then HS-USB
0x000001	Boot NAND option
0x000010	Boot HSIC option
0x000011	Boot USB option
0x001010	Enable Sahara protocol

BOOT_CONFIG_6=1:Fast boot
BOOT_CONFIG(5:0)=001010:Sahara prootcol

BOOT_CONFIG

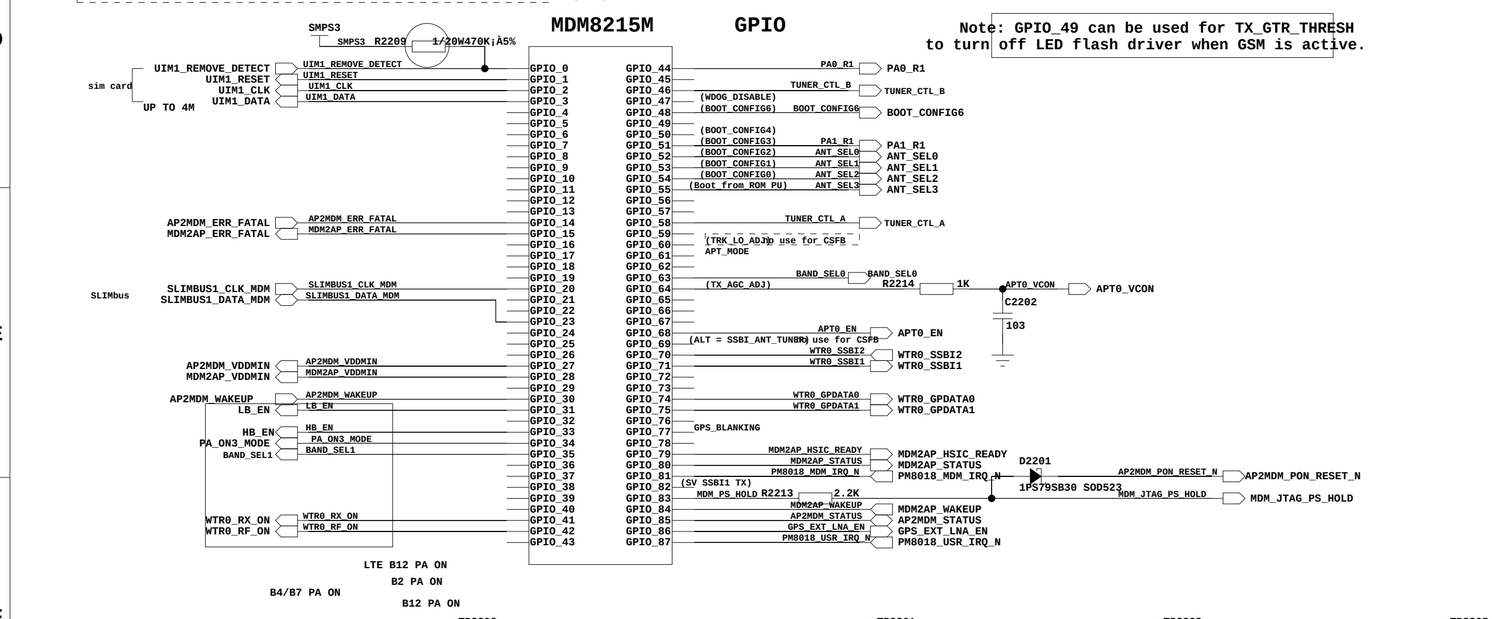


MDM8215M : MEMORY

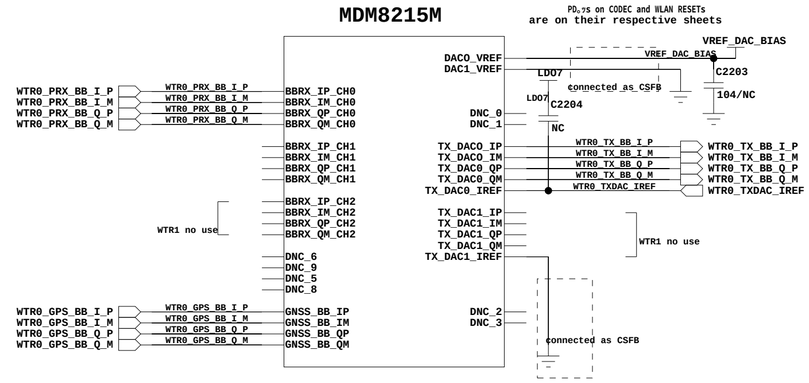


MDM8215M : GPIO & ANALOG IO

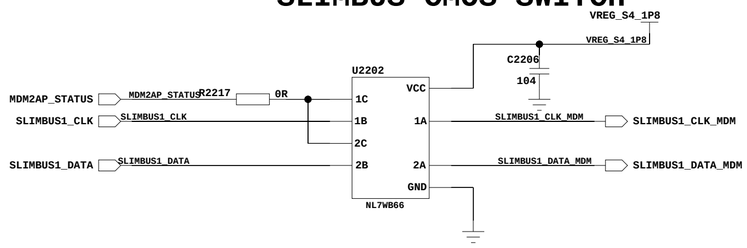
NOTE¡J
To wake up the MDM when there is UIM removal during sleep, a 20 K pullup to SMPS3 is needed¡£
There is less leakage when R is 470 K than when R2209 is 20 k,If UIM removal detection during sleep is not required



ANALOG IO



SLIMBUS CMOS SWITCH



S	Voltage	select
0	< 0.3 V	channel 1
1	> 1.15 V	channel 2

	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 7 of 7 Ver:
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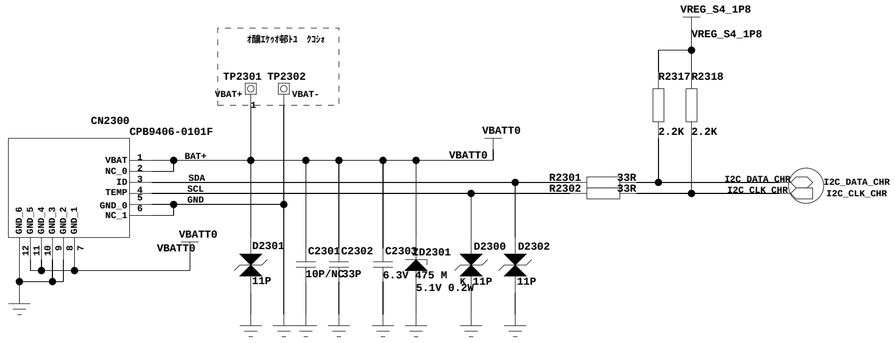
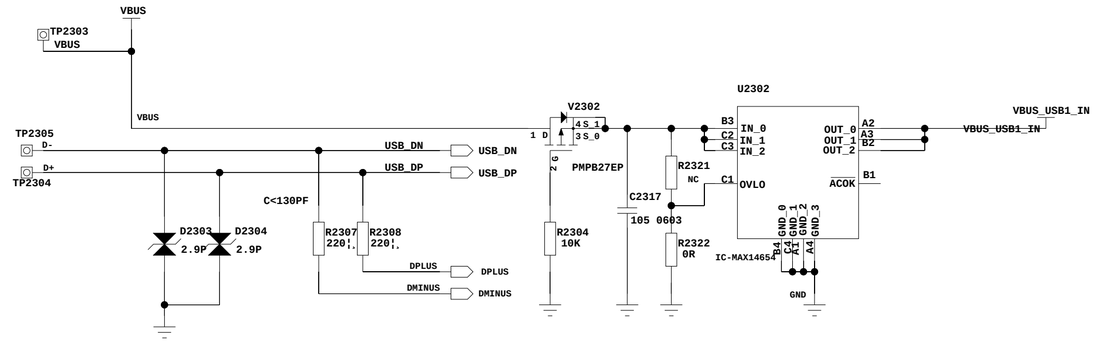
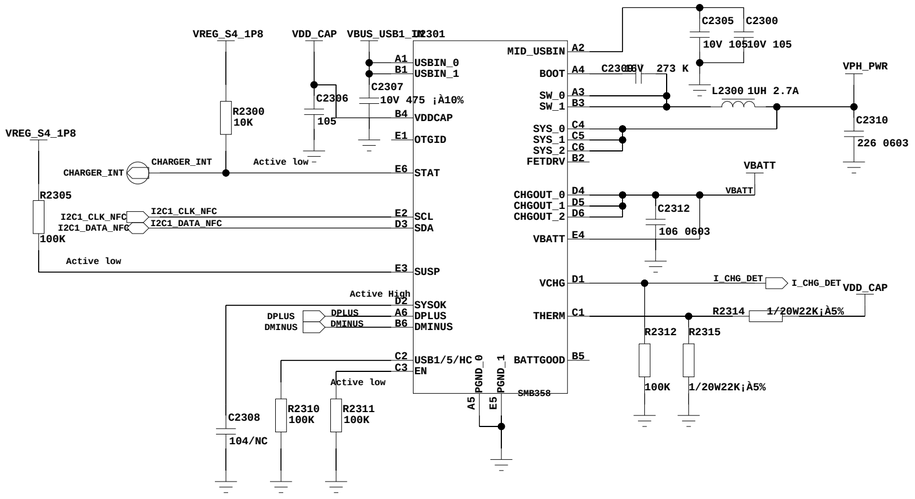
Battery Connector

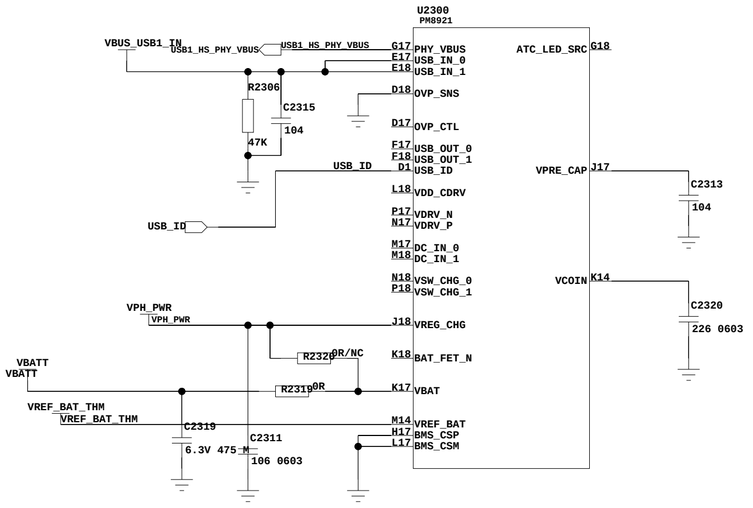


USB Connector



Circuit of Charge





	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 20 of 20 Ver:
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Approved By			

PLACE THE BULK CAPS IN CORNERS TO PROVIDE GENERAL FILL SUPPORT

S1 HF 1.5A 6.4M 1UH
S2 HF 1.5A 6.4M 2.2UH
S3 HF 1.5A 6.4M 0.5UH
S4 HF 1.5A 6.4M 2.2UH
S5 HF 1.5A 6.4M 1UH
S6 FT 2A 2.74M 1UH
S7 FT 2A 2.74M 1UH
S8 HF 1.5A 6.4M NC

VPH_PWR
C2401 226
C2402 226
C2403 6.3V 475 M
C2404 6.3V 475 M
C2405 106 0603
C2407 6.3V 475 M
C2408 6.3V 475 M
C2410 106 0603
C2411 6.3V 475 M

U2300
VDD_S1 A6
VDD_S2 A12
VDD_S3 A11
VDD_S4 V12
VDD_S5_0 A15
VDD_S5_1 A16
VDD_S6_1 V16
VDD_S6_0 V15
VDD_S7 V6
VDD_S8 V11
VIN_LVS1_3_6 T3
VIN_LVS2 M5
VIN_LVS4_5_7 N4
VDD_NCP U1
VIN_5VS F2

VREG_S4_1P8
VREG_S1_1P225
VREG_S7_1P15
VPH_PWR
ΣŧŧΣVPH_PWR

L2401 1UH ¡À20%
Rate 1.5A
VREG_S1_1P225
Power for L24\L25\LV$ΣΣ?ν:=
C2414 226 0603
L2402 2.2UH 1.9A
Rate 1.5A
VREG_S2_1P3
VREG_S2_1P8
power for VDD_FM_1P3\VDD_WLAN_1P3\VDD_BT_1P3\VDDA_WLAN
C2415 226
L2403 0.47UH ¡À20% 2.9A
Rate 2A
VREG_S3_1P05
power for VDD_CORE\VDDA_PCIE?ν:=
C2416 226
C2462 226
Rev.H ΣŧΣ226ŧ ŧ446,ϕ ∘VREG_S3_1P05ŧΣΣ?ν:=
L2404 2.2UH 1.9A
Rate 1.5A
VREG_S4_1P8
power for most of 1P8 voltage?ν:=
C2461 226 0603
C2421 0603
VREF_LPDDR2
power for LPDDR
KR0_SENSE
L2405 1UH 2.7A
Rate 2A
VREG_S5_1P05_KR0
power for CPU0
KR1_SENSE
L2406 1UH 2.7A
VREG_S6_1P05_KR1
C2419 226 0603
C2459 226 0603
C2422 226 0603
C2460 226 0603
power for CPU1
Rate 2A
Note: L2405 and L2406 are changed to higher current rating parts for the APQ8064 V2.0.
L2407 1UH ¡À20%
Rate 1.5A
VREG_S7_1P15
power for L26\L27\L28
C2423 226 0603

VREG_S1 B6
VSW_S1_0 A7
VSW_S1_1 B7
VREG_S2 B14
VSW_S2_0 A13
VSW_S2_1 B13
VREF_LPDDR2 K15
VREG_S3 B9
VSW_S3_0 A10
VSW_S3_1 B10
VREG_S4 U14
VSW_S4_0 U13
VSW_S4_1 V13
VREG_S5 B16
VSW_S5_0 A17
VSW_S5_1 A18
VSW_S5_2 B17
VREG_S6 U16
VSW_S6_0 U17
VSW_S6_1 V17
VSW_S6_2 V18
VREG_S7 U6
VSW_S7_0 U7
VSW_S7_1 V7
VREG_S8 U11
VSW_S8_0 U10
VSW_S8_1 V10

VOUT_LVS1 P4 100mA VREG_LVS1_1P8 VREG_LVS1_1P8 WCN3660
VOUT_LVS2 N5
VOUT_LVS3 R4 100mA VREG_LVS3 VREG_LVS3 APQ8064
VOUT_LVS4 P6 100mA VREG_LVS4_1P8 VREG_LVS4_1P8 Sensor
VOUT_LVS5 P5 100mA VREG_LVS5_1P8 VREG_LVS5_1P8 front and back camera
VOUT_LVS6 U4 100mA VREG_LVS6_1P8 VREG_LVS6_1P8 APQ8064
VOUT_LVS7 R5 100mA VREG_LVS7_1P8 VREG_LVS7_1P8 APQ8064

NCP_CTC1 U3
NCP_CTC2 V3
VREG_NCP V2
NCP_FB T2
LEAVE FLOATING

VOUT_5VS_OTG E1 Rate 500mA
VOUT_5VS_HMDI E2 Rate 62mA
VREG_XO H5
VREG_RF_CLK J5
Linear regulator output for XO circuits; internal use only??
VREG_XO
VREG_XO ν:=
Power for internel RF clock buffer
C2426 105
C2424 105
C2425 105
ROUTE THE GND FROM C2424 AND C2425 TO PIN H8 AND L8 OF U4 (PM8921)

PM8921

VREG_S4_1P8
VPH_PWR
U2300
VDD_L1_2_12_18 F4
VDD_L3_15_17 G1
VDD_L4_L14_SPLDO K5
VDD_L5_8_16 K1
VDD_L6_7 N2
VDD_L9_11 M2
VDD_L10_22 B2
VDD_L21_23_29 J2
VDD_L24 B5
VDD_L25 B4
VDD_L26 P2
VDD_L27 U5
VDD_L28 R2

VREG_L1 D4 Rate 150mA VREG_L1_1P05 VREG_L1_1P05 APQ8064¡JVDD_PXO ν:=
VREG_L2 E4 Rate 150mA VREG_L2_1P2 VREG_L2_1P2 APQ8064¡JVDD_LVDS_PLL
VREG_L3 G5 Rate 150mA VREG_L3_3P075 VREG_L3_3P075 APQ8064¡JVDD_USBPHY1_3P3¡FU¡J74LVC1G3157GW ν:=
VREG_L4 L5 Rate 50mA VREG_L4_1P8 VREG_L4_1P8 APQ8064/WCN3660/PM8921 internet circuit ν:=
VREG_L5 H1 Rate 300mA VREG_L5_2P95 VREG_L5_2P95 EMMC ν:=
VREG_L6 N1 Rate 600mA VREG_L6_2P95 VREG_L6_2P95 TF/ ν:=
VREG_L7 M4 Rate 150mA VREG_L7_2P95 VREG_L7_2P95 APQ8064:VDD_P2 ν:=
VREG_L8 J1 Rate 300mA VREG_L8_2P8 VREG_L8_2P8 front and back camera
VREG_L9 M1 Rate 300mA VREG_L9_2P95 VREG_L9_2P95 sensor
VREG_L10 C1 Rate 600mA VREG_L10_3P0 VREG_L10_3P0 WCN3660
VREG_L11 L4 Rate 150mA VREG_L11_2P7 VREG_L11_2P7 LCD
VREG_L12 F5 Rate 150mA VREG_L12_1P2 VREG_L12_1P2
VREG_L14 M15 Rate 50mA VREG_L14_1P8 VREG_L14_1P8 PM8921 internel circuit
VREG_L15 G4 Rate 150mA VREG_L15_HS HP MIC BIAS_BACKUP
VREG_L16 L1 Rate 300mA VREG_L16_2P8 VREG_L16_2P8 TP
VREG_L17 F1 Rate 150mA VREG_L17_1P8 VREG_L17_1P8
VREG_L18 E5 Rate 150mA
VREG_L21 H4 Rate 150mA VREG_L21_1P8 VREG_L21_1P8 LCD
VREG_L22 B3 Rate 150mA VREG_L22_1P8 VREG_L22_1P8 WCD9310
VREG_L23 K4 Rate 150mA VREG_L23_1P8 VREG_L23_1P8 APQ8064:VDD_PLL1ν:=
VREG_L24 A5 Rate 120mA VREG_L24_1P05 VREG_L24_1P05
VREG_L25 A4 Rate 120mA VREG_L25_1P225 VREG_L25_1P225 WCD9310/APQ8064 ν:=
VREG_L26 P1 Rate 120mA 0.75-1.25V VREG_L26_1P05 VREG_L26_1P05 APQ8064:VDD_QDSP6_APP
VREG_L27 V5 Rate 120mA VREG_L27_1P05 VREG_L27_1P05 APQ8064
VREG_L28 R1 Rate 120mA VREG_L28_1P05 VREG_L28_1P05 CAMERA
J4 Rate 150mA

C2432 225
C2433 225
C2434 474
C2435 105
C2436 105
C2437 474
C2438 105
C2439 225
C2440 474
C2441 474
C2442 225
C2443 474
C2444 474
C2445 474
C2446 474
C2447 225
C2448 474
C2449 474
C2450 474
C2451 475
C2452 475
C2453 475
C2454 475
C2455 475
C2456 474
C2457 474
6.3V 475 M

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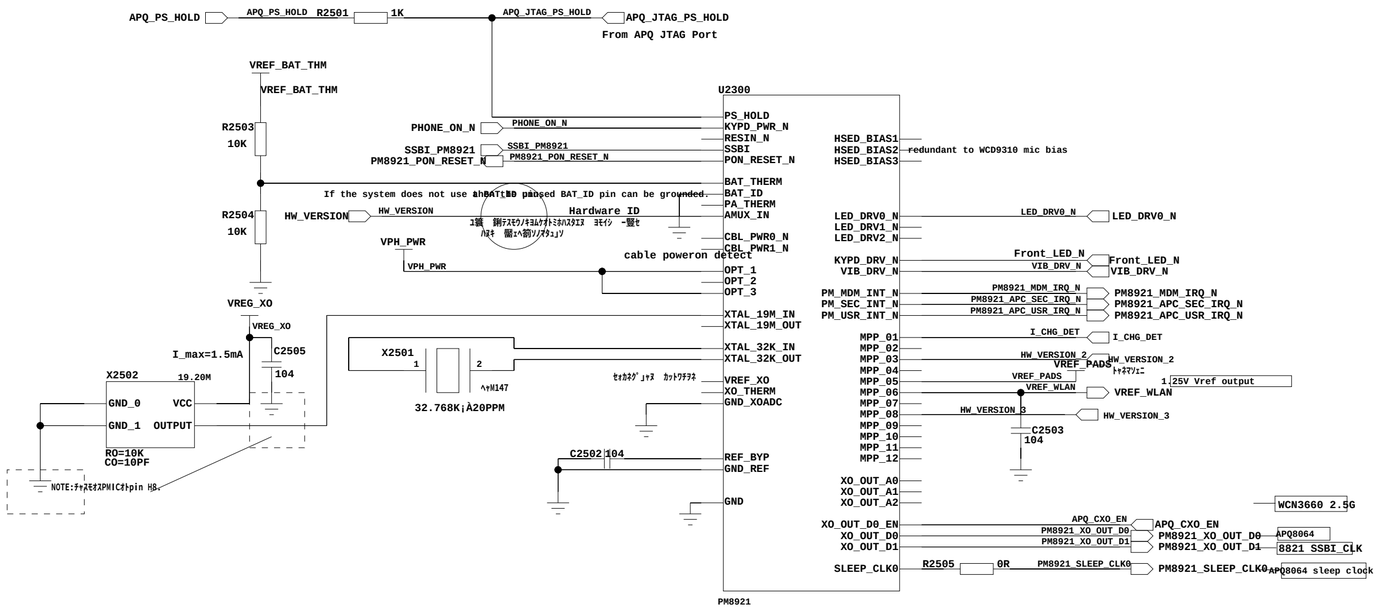
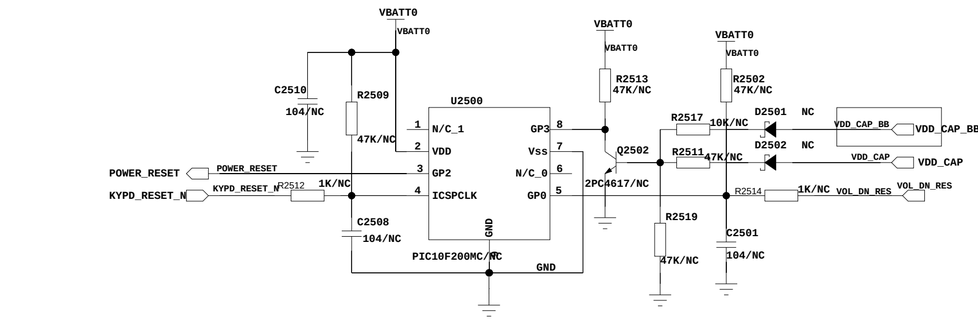
Standard By			
Approved By			

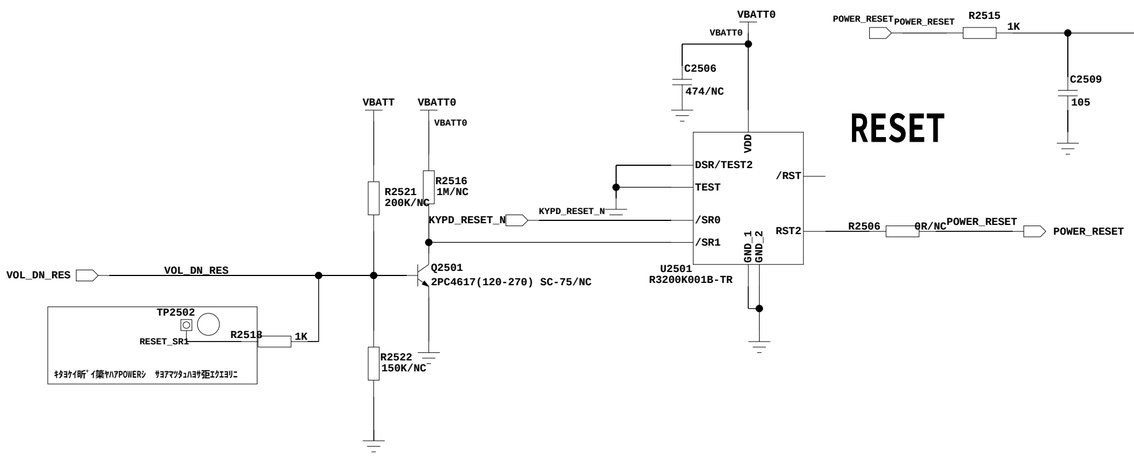
oppo

PM8921 : AMUX, CLK AND MPPS

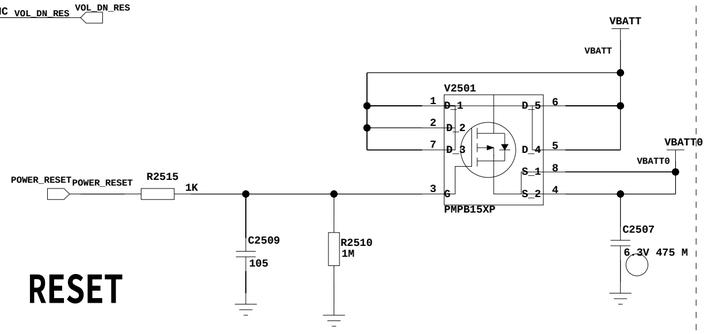


RESET



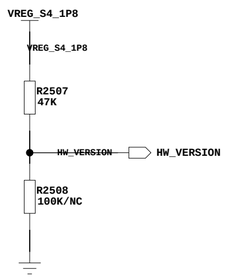


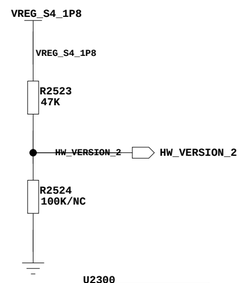
RESET

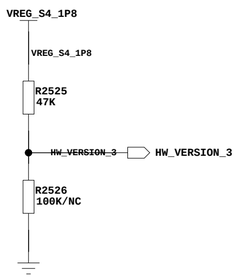


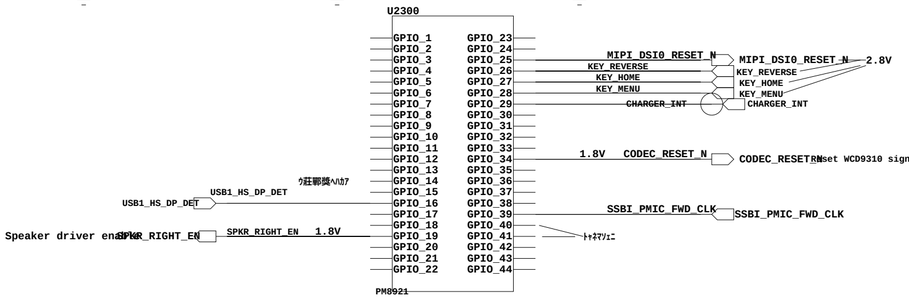
ﾓｲｼ -豎ｾﾇ ﾖ」ｺ

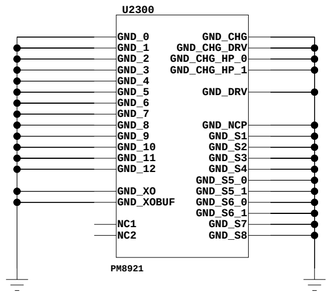
	EVB	EVT	DVT	PVT
ﾉﾏﾀｭｵ釋	24K	47K	100K	150K
ﾏｯﾀｭｵ釋	100K	100K	100K	100K
ｷﾖﾑｹﾖｵ	1.452V	1.224V	0.9V	0.72V











	Sign	Date	Type:
Drawn By			Draw No: Schematic1
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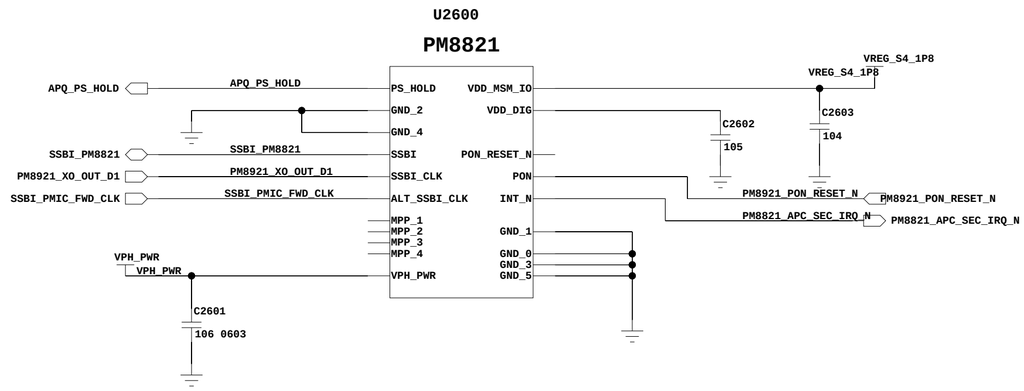
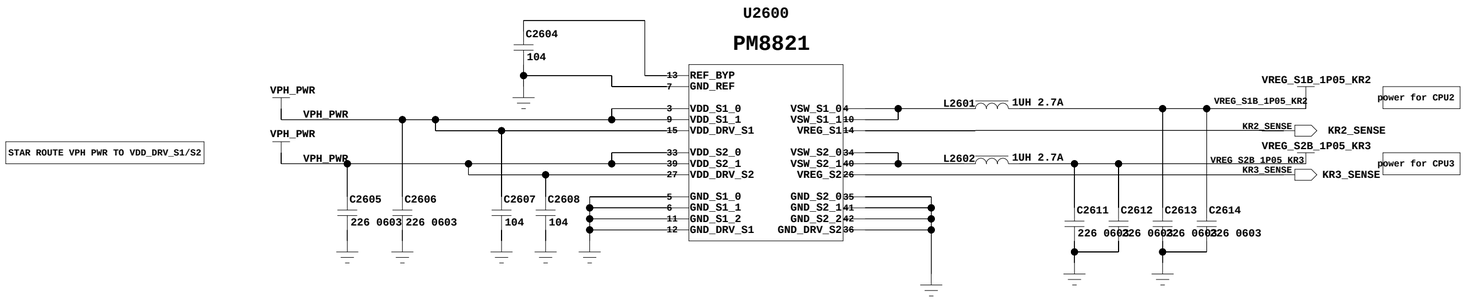
Approved By			





STAR ROUTE VPH PWR TO VDD_DRV_S1/S2

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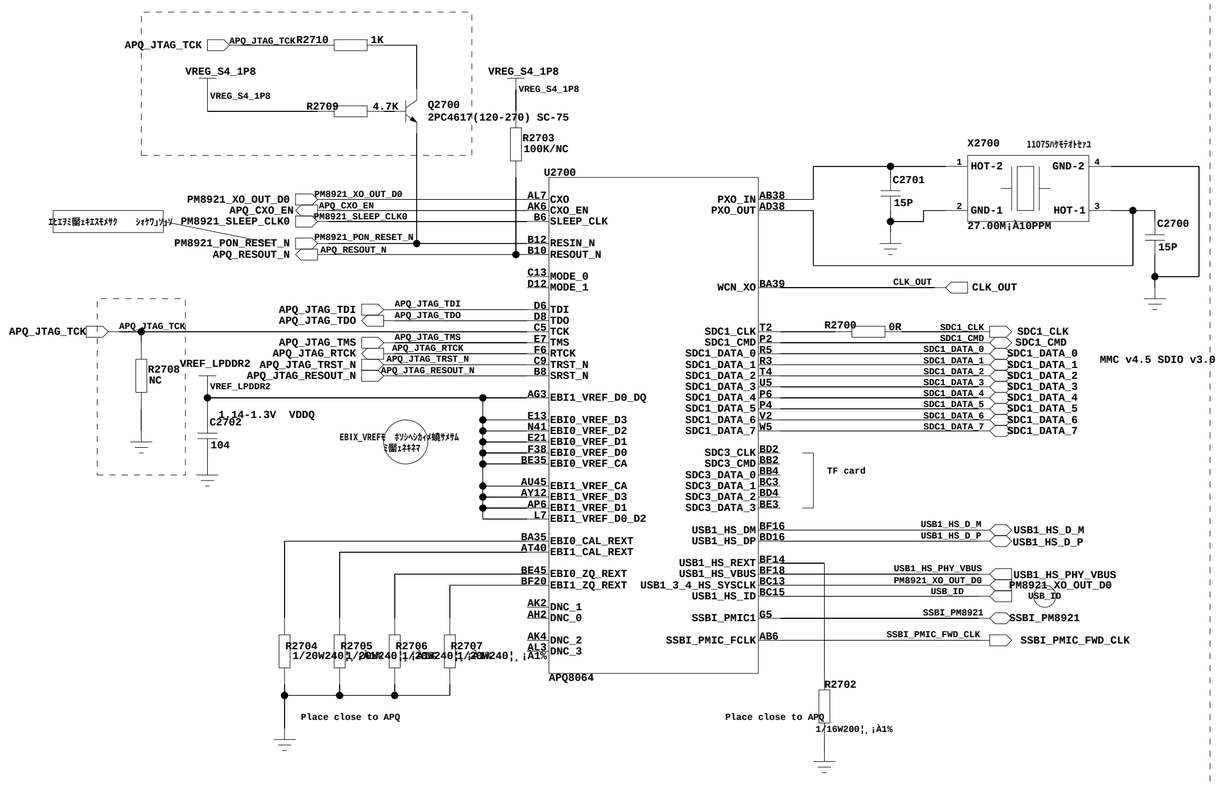
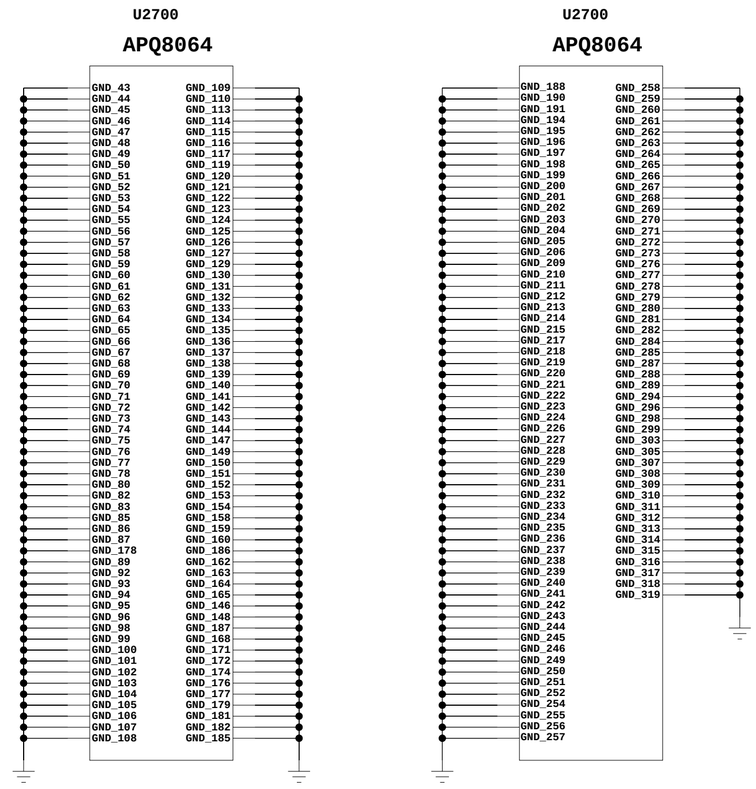
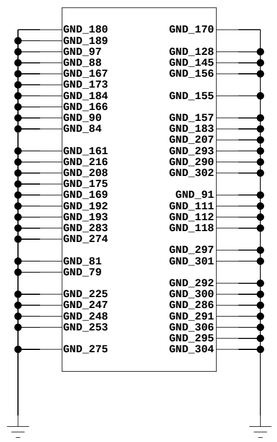
Approved By			

APQ8064 : CONTROL



APQ8064 : GND





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Drawn By			Draw No: Schematic1
Checked By			Sheet 16 of 16 Ver:
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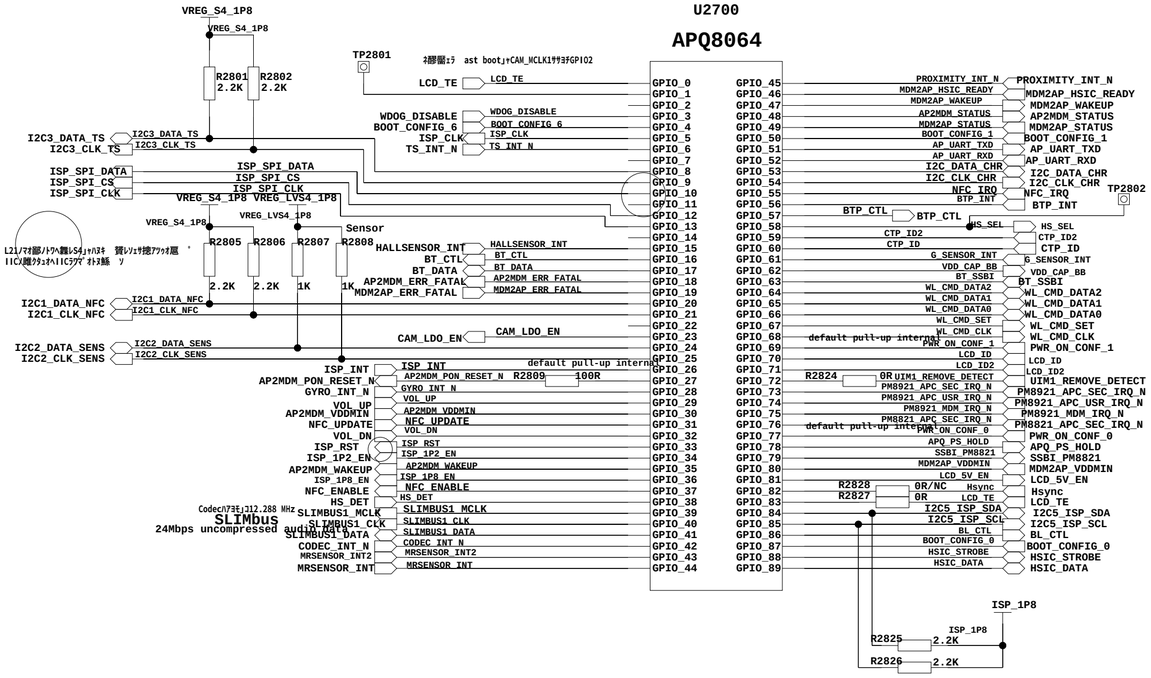
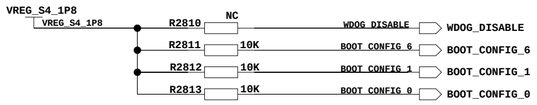
Approved By			

APQ8064 : GPIOS

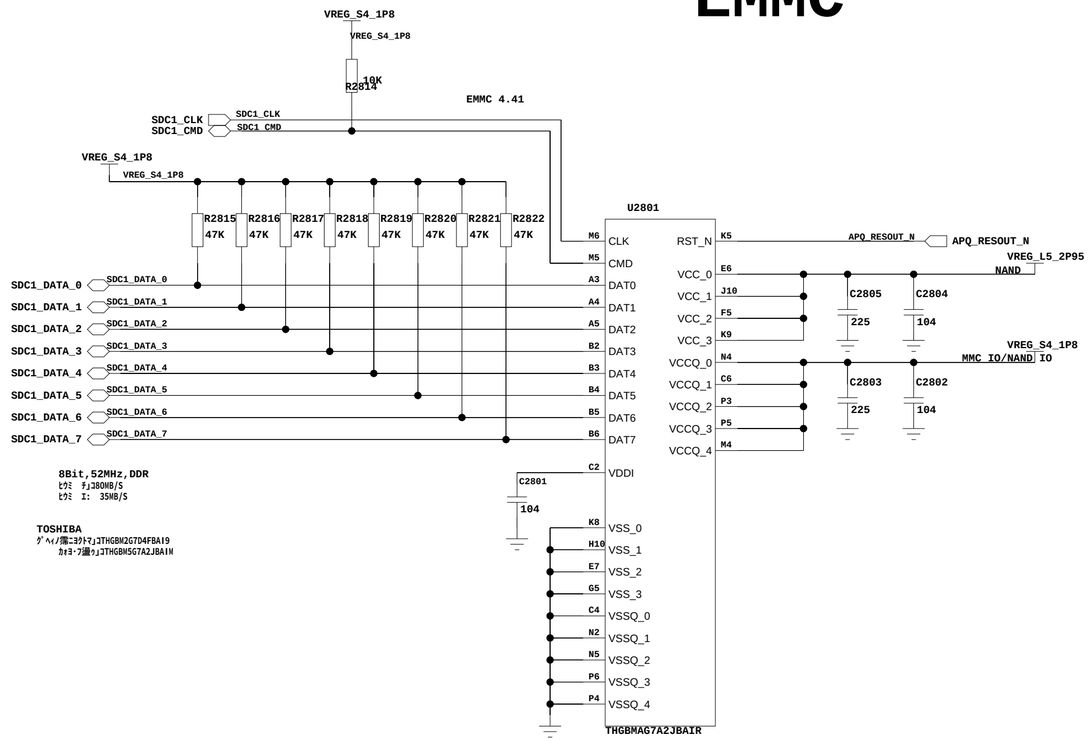


If fast boot is required, external PU on BOOT_CONFIG[6] should be installed. Since BOOT_CONFIG[6] GPIO_4 is also used for CAM_MCLK1 and depending on the camera sensor there is a possibility the sensor is in an undefined state and can sink current from CAM_MCLK1 when FET is ON. This will bring down the voltage on BOOT_CONFIG[6] which could potentially cause boot failure. To avoid this problem, GPIO_2 can be used for CAM_MCLK1 instead.

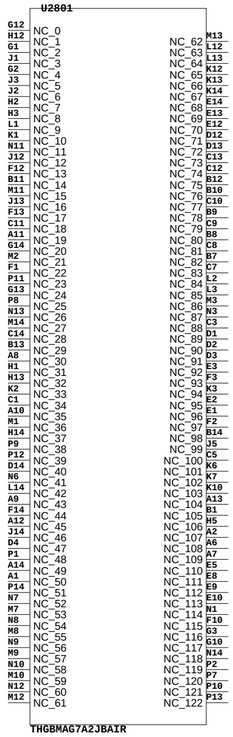
BOOT_CONFIG[6]	0=Secure Boot 1=Fast Boot
BOOT_CONFIG[5:0]=000011 for eMMC boot,000010 for SDC3 followed by SDC2	



EMMC



and the chip should has no special requirement on 1.8V/2.95V power on sequence (which is fixed by our pmic, some eMMC has special requirement on it, most has no requirement on it)



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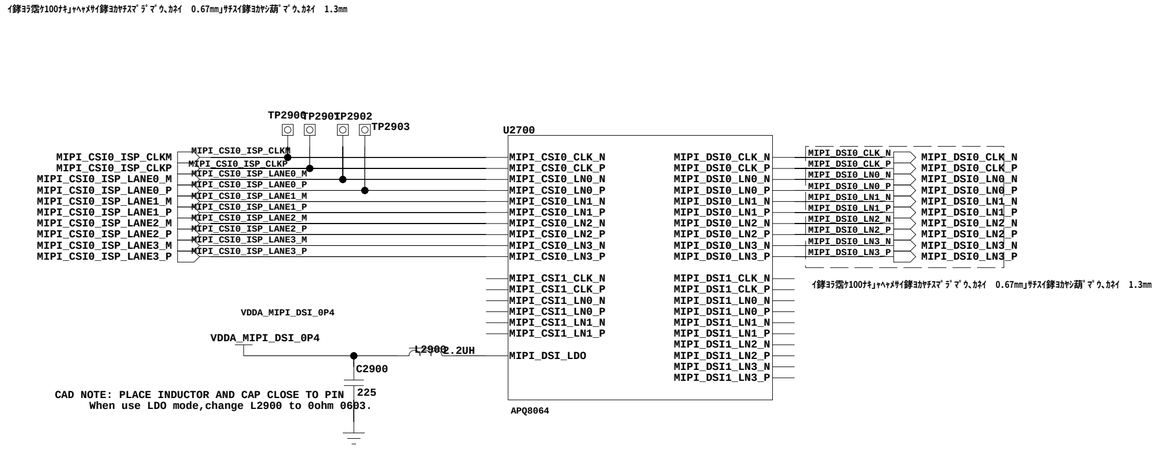
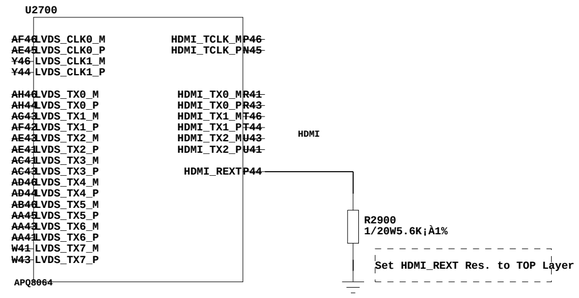
Drawn By			Draw No: A2SHEET
Checked By			Sheet 1 of 2 Ver:
Standard By			
Approved By			

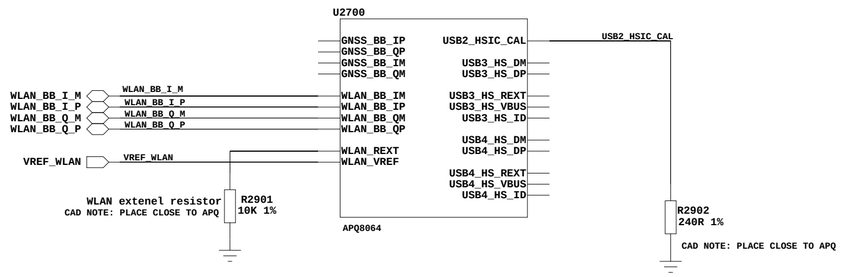
APQ8064: MIPI



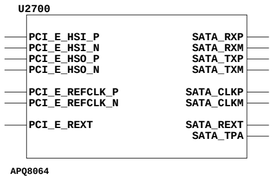
APQ8064: LVDS, HDMI



APQ8064 : USB, GPS AND WLAN



APQ8064 : PCIE AND SATA



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Approved By			

APQ8064 : POWER 1

U2700

APQ8064

VREG_S4_1P8
VREG_S4_1P8
Core1 for POP DDR
1.7-1.95V
POP DDR:ELPIDA-EDBA164B1PF-1D-F
VREG_L25_1P225
VREG_L25_1P225
Core2 for POP DDR
1.14-1.3V
VREG_L26_1P05
VREG_L26_1P05
PDN 65 mR@25MHz
KR0_SENSE
KR1_SENSE
KR2_SENSE
KR3_SENSE
VREG_L1_1P05
VREG_L1_1P05
VREG_LVS3
VREG_LVS3
VREG_S3_1P05
VREG_S3_1P05
VREG_L24_1P05
VREG_L24_1P05
Low voltage PLL
VREG_LVS7_1P8
VREG_LVS7_1P8
high voltage PLL
VREG_LVS7_1P8
CAD NOTE: STAR ALL THE PLL POWER
VREG_S3_1P05
VREG_S3_1P05
Platform crystal oscillotr
VDD_DDR_C1_0
VDD_DDR_C1_1
VDD_DDR_C1_2
VDD_DDR_C1_3
VDD_DDR_C1_4
VDD_DDR_C1_5
VDD_DDR_C1_6
VDD_DDR_C2_0
VDD_DDR_C2_1
VDD_DDR_C2_2
VDD_DDR_C2_3
VDD_DDR_C2_4
VDD_DDR_C2_5
VDD_DDR_C2_6
VDD_DDR_C2_7
VDD_DDR_C2_8
VDD_DDR_C2_9
VDD_DDR_C2_10
VDD_QDSP6_APP_0
VDD_QDSP6_APP_1
VDD_QDSP6_APP_2
VDD_QDSP6_APP_3
VDD_KR0_SNS
VDD_KR1_SNS
VDD_KR2_SNS
VDD_KR3_SNS
VDD_PXO
VDD_QFUSE_PRG
VDD_CORE_17
VDD_CORE_97
VDD_PLL1_0
VDD_PLL1_2
VDD_PLL1_1
VDD_PLL2_5
VDD_PLL2_6
VDD_PLL2_4
VDD_PLL2_1
VDD_PLL2_2
VDD_PLL2_3
VDD_PLL2_0
VDD_CORE_100
VDD_CORE_98
VDD_CORE_99
VDD_MIPI_4
VDD_MIPI_1
VDD_MIPI_3
MIPI_DSI0_CAL
MIPI_DSI1_CAL
VDD_MIPI_0
VDD_MIPI_2
VDD_HDMI_0
VDD_HDMI_1
VDD_LVDS_PLL
VDD_LVDS_0
VDD_LVDS_1
VDD_SATA_0
VDD_SATA_1
VDD_PCIE_0
VDD_PCIE_1
VDD_A2
VDDA_WLAN
VDDA_GPS
VREF_SDC
VDD_USBPHY1_1P8
VDD_USBPHY1_3P3
VDD_USBPHY3_1P8
VDD_USBPHY3_3P3
VDD_USBPHY4_1P8
VDD_USBPHY4_3P3
VDD_MEM_0
VDD_MEM_14
VDD_MEM_1
VDD_MEM_5
VDD_MEM_49
VDD_MEM_43
VDD_MEM_47
VDD_MEM_2
VDD_MEM_41
VDD_MEM_11
VREG_L2_1P2
VREG_L2_1P2
VDDA_MIPI_DSI_0P4
VDDA_MIPI_DSI_0P4
VREG_LVS7_1P8
VREG_LVS7_1P8
VREG_L2_1P2
VREG_L2_1P2
VREG_LVS7_1P8
VREG_LVS7_1P8
VREG_LVS7_1P8
VREG_S3_1P05
VREG_S3_1P05
VREG_LVS6_1P8
VREG_LVS6_1P8
VREG_S2_1P3
VREG_S2_1P3
VREF_PADS
VREF_PADS
Refrence voltage for SD controller
VREG_L4_1P8
VREG_L4_1P8
VREG_L3_3P075
VREG_L3_3P075
VREG_L24_1P05
VREG_L24_1P05

APQ8064 : DECOUPLING CAPS

VREG_S4_1P8
VREG_S4_1P8
DDR_C1,P1
C3001 C3002 C3003 C3004 C3005 C3006
105 105 105 105 105 105

VREG_L25_1P225
VREG_L25_1P225
DDR_C2,P1
C3007 C3008 C3009 C3010 C3011 C3012 C3013 C3014
105 105 105 105 105 105 105 105

VREG_L26_1P05
VREG_L26_1P05(AB36)(AB35)(AB37)
QDSP
PDN 65 mR@25MHz
C3015 C3016 C3017 C3046
474 474 474 474
OPPO ADD

VREG_L1_1P05
VREG_L1_1P05 (AA37)
C3018
105

VREG_LVS3
VREG_LVS3
(AW7)
C3019
105

VREG_S3_1P05
VREG_S3_1P05(B7) (BA5)
VDD_CORE
PDN 25 mR@25MHz
C3020 C3021
474/NC 474

VREG_L24_1P05
VREG_L24_1P05(V18)(AE10)(AB34)
PLL1,MEM
PDN 30 mR@25MHz
C3022 C3023 C3024
474 474/NC 474

VREG_LVS7_1P8
VREG_LVS7_1P8(AV32) (AC7)
C3025
105

VREG_LVS7_1P8
VREG_LVS7_1P8(AB30)(K28) (W19)(AB19) (H8)
PLL2,HDMI
C3026 C3027 C3028 C3029 C3030
105 105 105 105 105

VREG_S3_1P05
VREG_S3_1P05(BA19, BA15)(BA9)
C3031 C3032
105 105

VREG_L2_1P2
VREG_L2_1P2(AW40) (AK38,AM38,AP38) (AV38)
C3033 C3034 C3035
105 105 105

VREG_LVS7_1P8
VREG_LVS7_1P8(P38) (P42)
C3036
105

VREG_L2_1P2
VREG_L2_1P2(AG41)
MIPI
C3037
105

VREG_LVS7_1P8
VREG_LVS7_1P8(AF38)(AD40)
C3038
105

VREG_LVS7_1P8
VREG_LVS7_1P8(L41)(M44)
C3039
105

VREG_S3_1P05
VREG_S3_1P05(F44,G43)
C3040
105

VREG_LVS6_1P8
VREG_LVS6_1P8(F42)
A2
C3041
105

VREG_S2_1P3
VREG_S2_1P3(BA23)
WLAN
C3042
105

VREF_PADS
VREF_PADS (BC5)
C3043
105

VREG_L4_1P8
VREG_L4_1P8(BB18)
WLAN XO,USB_PHY
C3044
105

VREG_L3_3P075
VREG_L3_3P075(BA17)
C3045
105

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oppo

APQ8064 : POWER 2

U2700

APQ8064

VREG_L24_1P05

PDN 30 mR@25 MHz

to 0.75V

VDD_MEM_3 VDD_MEM_4 VDD_MEM_6 VDD_MEM_7 VDD_MEM_8 VDD_MEM_9 VDD_MEM_10 VDD_MEM_12 VDD_MEM_13 VDD_MEM_15 VDD_MEM_16 VDD_MEM_17 VDD_MEM_18 VDD_MEM_19 VDD_MEM_20 VDD_MEM_21 VDD_MEM_22 VDD_MEM_23 VDD_MEM_24 VDD_MEM_25 VDD_MEM_26 VDD_MEM_27 VDD_MEM_28 VDD_MEM_29 VDD_MEM_30 VDD_MEM_31 VDD_MEM_32 VDD_MEM_33 VDD_MEM_34 VDD_MEM_35 VDD_MEM_36 VDD_MEM_37 VDD_MEM_38 VDD_MEM_39 VDD_MEM_40 VDD_MEM_42 VDD_MEM_44 VDD_MEM_45 VDD_MEM_46 VDD_MEM_48

VDD_P1_0 VDD_P1_1 VDD_P1_2 VDD_P1_3 VDD_P1_4 VDD_P1_5 VDD_P1_6 VDD_P1_7 VDD_P1_8 VDD_P1_9 VDD_P1_10 VDD_P1_11 VDD_P1_12 VDD_P1_13

VDD_P1_14 VDD_P1_15 VDD_P1_16 VDD_P1_17 VDD_P1_18 VDD_P1_19 VDD_P1_20 VDD_P1_21 VDD_P1_22 VDD_P1_23 VDD_P1_24 VDD_P1_25 VDD_P1_26 VDD_P1_27 VDD_P1_28 VDD_P1_29 VDD_P1_30 VDD_P1_31 VDD_P1_32 VDD_P1_33 VDD_P1_34 VDD_P1_35 VDD_P1_36 VDD_P1_37 VDD_P1_38 VDD_P1_39 VDD_P1_40 VDD_P1_41

VREG_L25_1P225

EBI0,EBI1

VREG_L7_2P95

SDC3

VDD_P2

VREG_S4_1P8

most 1A

VDD_P3_0 VDD_P3_1 VDD_P3_2 VDD_P3_3 VDD_P3_4 VDD_P3_5 VDD_P3_6 VDD_P3_7 VDD_P3_8 VDD_P3_9 VDD_P3_10 VDD_P3_11 VDD_P3_12 VDD_P3_13 VDD_P3_14 VDD_P3_15 VDD_P3_16 VDD_P3_17 VDD_P3_18 VDD_P3_19 VDD_P3_20 VDD_P3_21 VDD_P3_22 VDD_P3_23

VDD_P4

HSIC PAD

C3139

105

Shorted VREG_L27 of PM8921 to VREG_S3_1P05 at VDD_CORE pins to supply additional current

VREG_L27_1P05

R3100

0R

to 0.5V

VREG_S3_1P05

PDN 25 mR @25 MHz

U2700

APQ8064

VDD_CORE_0 VDD_CORE_1 VDD_CORE_2 VDD_CORE_3 VDD_CORE_4 VDD_CORE_5 VDD_CORE_6 VDD_CORE_7 VDD_CORE_8 VDD_CORE_9 VDD_CORE_10 VDD_CORE_11 VDD_CORE_12 VDD_CORE_13 VDD_CORE_14 VDD_CORE_15 VDD_CORE_16 VDD_CORE_18 VDD_CORE_19 VDD_CORE_20 VDD_CORE_21 VDD_CORE_22 VDD_CORE_23 VDD_CORE_24 VDD_CORE_25 VDD_CORE_26 VDD_CORE_27 VDD_CORE_28 VDD_CORE_29 VDD_CORE_30 VDD_CORE_31 VDD_CORE_32 VDD_CORE_33 VDD_CORE_34 VDD_CORE_35 VDD_CORE_36 VDD_CORE_37 VDD_CORE_38 VDD_CORE_39 VDD_CORE_40 VDD_CORE_41 VDD_CORE_42 VDD_CORE_43 VDD_CORE_44 VDD_CORE_45 VDD_CORE_46 VDD_CORE_47 VDD_CORE_48 VDD_CORE_49 VDD_CORE_50 VDD_CORE_51 VDD_CORE_52 VDD_CORE_53 VDD_CORE_54

VDD_CORE_55 VDD_CORE_56 VDD_CORE_57 VDD_CORE_58 VDD_CORE_59 VDD_CORE_60 VDD_CORE_61 VDD_CORE_62 VDD_CORE_63 VDD_CORE_64 VDD_CORE_65 VDD_CORE_66 VDD_CORE_67 VDD_CORE_68 VDD_CORE_69 VDD_CORE_70 VDD_CORE_71 VDD_CORE_72 VDD_CORE_73 VDD_CORE_74 VDD_CORE_75 VDD_CORE_76 VDD_CORE_77 VDD_CORE_78 VDD_CORE_79 VDD_CORE_80 VDD_CORE_81 VDD_CORE_82 VDD_CORE_83 VDD_CORE_84 VDD_CORE_85 VDD_CORE_86 VDD_CORE_87 VDD_CORE_88 VDD_CORE_89 VDD_CORE_90 VDD_CORE_91 VDD_CORE_92 VDD_CORE_93 VDD_CORE_94 VDD_CORE_95 VDD_CORE_96

デバッグ raitモニタ aps

PDN 25 mR @25 MHz

U2700

APQ8064

VREG_S5_1P05_KR0

VDD_KR0_2 VDD_KR0_3 VDD_KR0_4 VDD_KR0_5 VDD_KR0_6 VDD_KR0_0 VDD_KR0_1

VREG_S6_1P05_KR1

VDD_KR1_2 VDD_KR1_3 VDD_KR1_4 VDD_KR1_5 VDD_KR1_6 VDD_KR1_0 VDD_KR1_1

VDD_KR2_1 VDD_KR2_2 VDD_KR2_3 VDD_KR2_4 VDD_KR2_0 VDD_KR2_5 VDD_KR2_6

VREG_S1B_1P05_KR2

VDD_KR3_3 VDD_KR3_4 VDD_KR3_5 VDD_KR3_6 VDD_KR3_1 VDD_KR3_0 VDD_KR3_2

VREG_S2B_1P05_KR3

APQ8064 : DECOUPLING CAPS

VDD_CORE

PDN 25 mR @25 MHz

VREG_S3_1P05

C3101 C3102 C3103 C3104 C3105 C3106 C3107 C3108 C3109 C3110 C3111 C3112 C3113

474 474 474/NC 474 474/NC 474 474 474/NC 474/NC 474/NC 474/NC 474/NC 474

VDD_MEM,PLL1

PDN 30 mR@25 MHz

VREG_L24_1P05

C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3124 C3125 C3126

474/NC 474 474 474 474 474/NC 474/NC 474 474/NC 474 474/NC 474

VREG_L25_1P225

VDD_P1

C3127 C3128 C3129 C3130 C3131 C3132 C3133 C3134 C3135 C3136 C3137 C3138

105 105 105 105 105 105 105 105 105 105 105 105

VDD_P2

VREG_L7_2P95 (AY8)

C3140

105

VREG_S4_1P8

VDD_P3

C3141 C3142 C3143 C3144 C3145 C3146 C3147 C3148 C3149 C3150 C3151 C3152

105 105 105 105 105 105 105 105 105 105 105 105

PDN 25 mR @25 MHz

VREG_S5_1P05_KR0

C3160 C3161 C3162 C3163 C3164 C3165 C3166

474/NC 474/NC 474/NC 474/NC 474 474/NC 474

PDN 25 mR @25 MHz

VREG_S6_1P05_KR1

C3153 C3154 C3155 C3156 C3157 C3158 C3159

474 474/NC 474 474/NC 474 474/NC 474/NC

PDN 25 mR @25 MHz

VREG_S1B_1P05_KR2

C3174 C3175 C3176 C3177 C3178 C3179 C3180

474/NC 474 474 474/NC 474/NC 474/NC 474/NC

PDN 25 mR @25 MHz

VREG_S2B_1P05_KR3

C3167 C3168 C3169 C3170 C3171 C3172 C3173

474 474/NC 474/NC 474 474/NC 474 474/NC

	Sign	Date	Type:
Drawn By			Draw No: Schematic1
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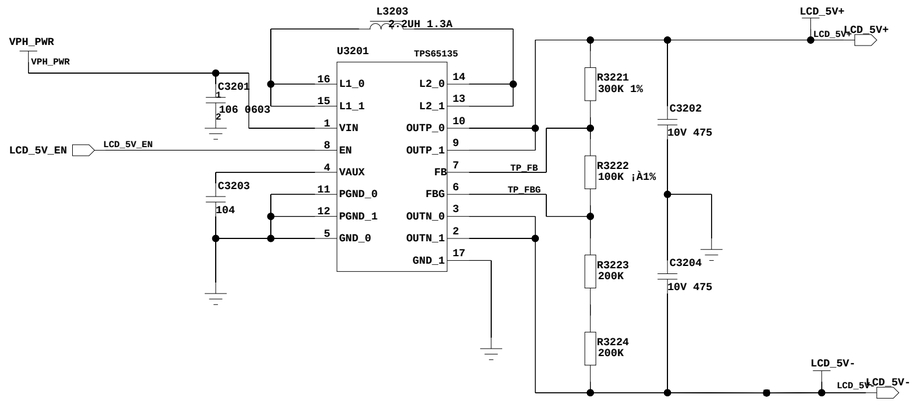
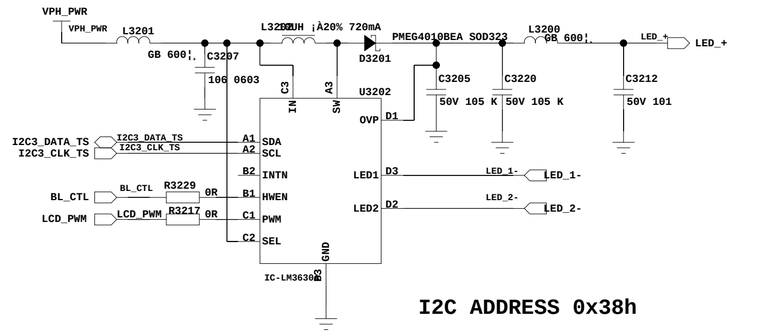
Standard By			
Approved By			

oppo

LCD ¡À5V

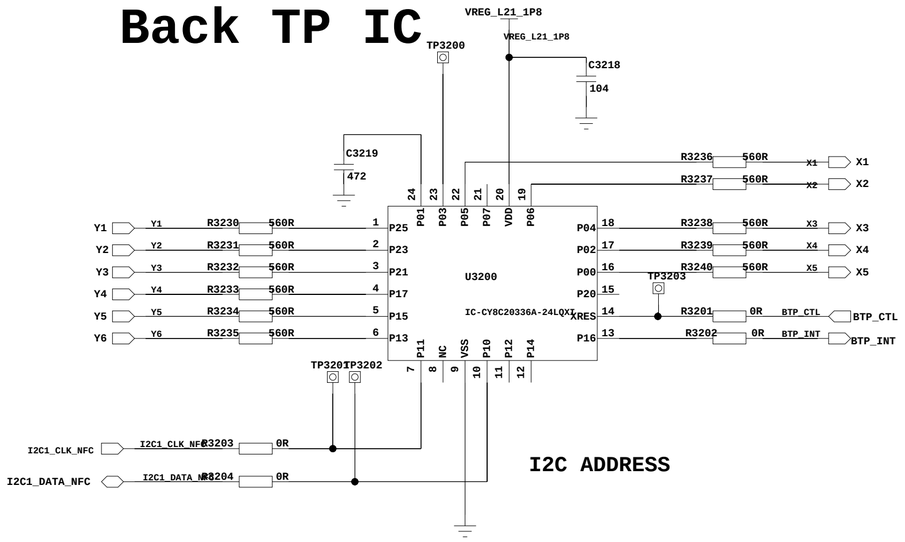


LCD BL



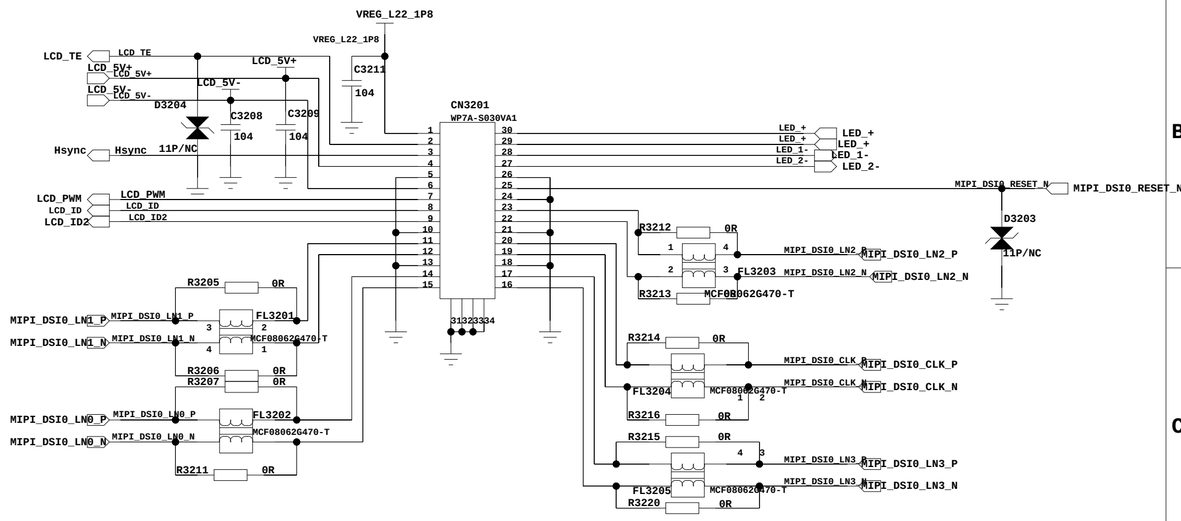
I2C ADDRESS 0x38h

Back TP IC

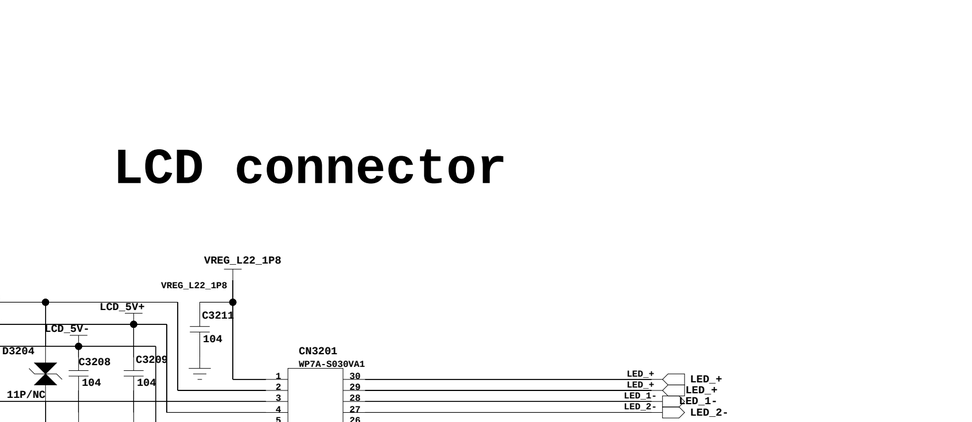


I2C ADDRESS

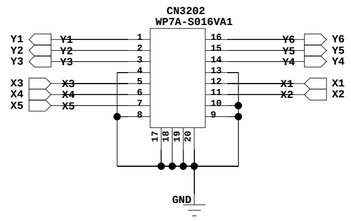
LCD connector



Sub board connector



Back TP connector



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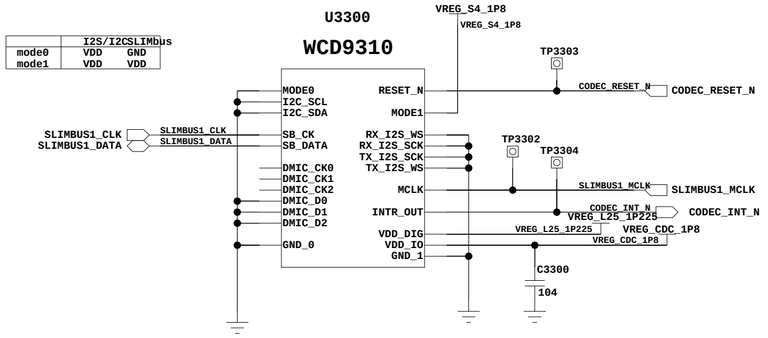
WCD9310 POWER OPTIONS

U3300

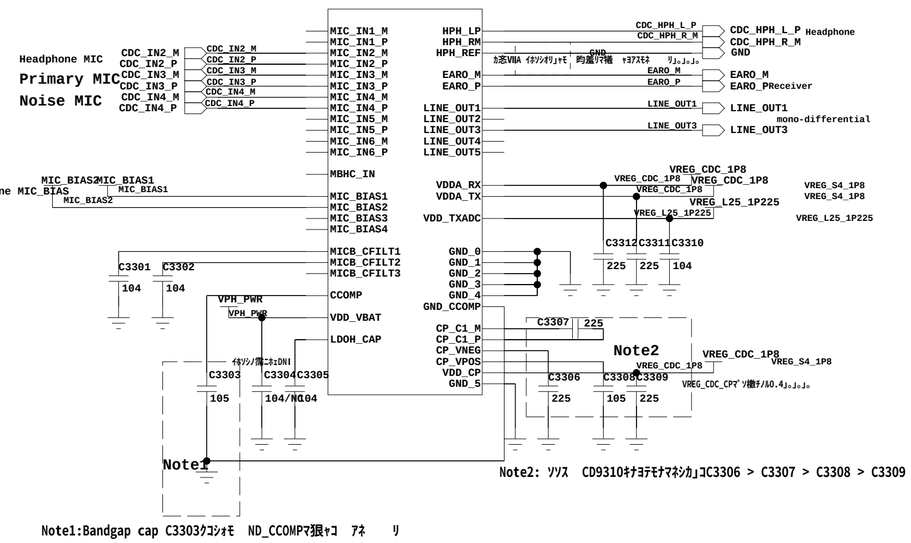
WCD9310

	I2S/I2CSLIMbus
mode0	VDD GND
mode1	VDD VDD



U3300

WCD9310



Note1:Bandgap cap C3303ｶｺﾝｼｮﾓ ND_CCOMPﾏﾃ狽ｷｬｺ ｱﾈ ﾘ

Note2: ｿｿｽ CD9310ﾈﾅｺﾃﾓﾅﾏﾏﾈｼｶ」ｺC3306 > C3307 > C3308 > C3309

WCD3660 Power Tree

VDD_BAT(Pin 63)	VPH_PWR
VDD_TXADC(Pin 41) VDD_DIG(Pin 26)	VREG_L25_1P225
VDD_CP(Pin3) VDD_IO(Pin33) VDDA_RX(Pin30) VDDA_TX(Pin64)	VREG_S4_1P8

WCD3660 Frequency Table

Name	Clock Source	Frequency(MHz)
	Active Mode	
System Clock	GPIO_39(APQ8064)	12.288
MBHC	MCLK	12.288
TxADC	MCLK/2	6.144
RxDAC	MCLK/2	6.144
SLIMBus Clock	MSM LPASS	24.576
	Standby Mode	
System Clock	RC oscillator	12.288
MBHC	RC oscillator	12.288
AUX_PGA	RC oscillator	12.288
Charge Pump	RC oscillator	12.288

WCD3660 Power Consumption

Scenario	Test Conditions	Typical Current(uA)						
		VBAT(3.8V)	VDD_TXADC(1.2V)	VDD_DIG(1.2	VDD_CP(1.8V)	VDD_IO(1.8V)	VDD_RX and VDD_TX(1.8V)	Total Current
Reset	WCD in reset (reset pin held high), MCLK off	1.8	0.45	2.86	0.05	0.04	0.16	5.36
Standby (idle)	WCD taken out of reset, MCLK off	1.8	0.44	2.86	0.05	0.04	0.16	5.35
Stereo playback to HPH	48 kHz,24 bits,16 R load quiescent	1.4	6.80	988.60	812.40	24.40	726.60	2560.2
mono-differential line out	48kHz, 24 bits, 10 k? load	4.00	3.00	640.00	4.00	40.00	1445.00	2136.00
Handset voice call	8 kHz sample rate, 16 bits	258.00	325.00	1210.00	644.00	110.00	920.00	3467
Headset voice call	stereo HPH 16R 8 kHz	568.00	159	10	783	10	981	2511
Speaker phone mode	Mono analog mic,8 kHz,16 bits	218	162	810	4	30	1695	2919
Stereo recording	Dual analog mics capless,16 bits,48 kHz	20	324	720	3	70	523	1660

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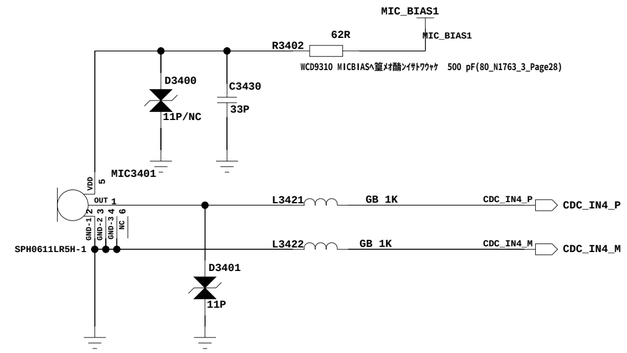
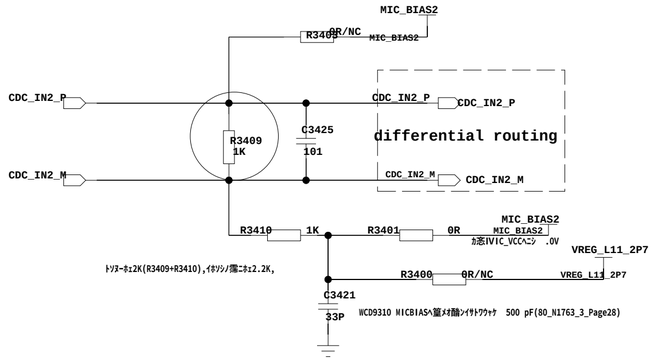
Approved By			oppo

Noise MIC



BOT

Headphone MIC



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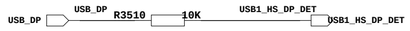
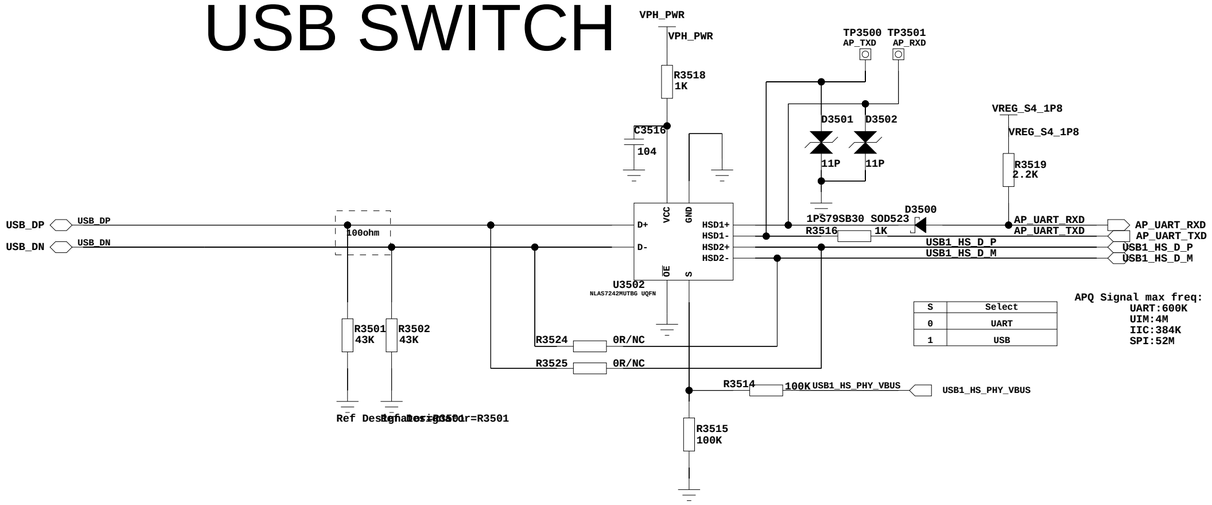
Checked By			Sheet of Ver:
Standard By			24_MIC_HP2SPK_EAR
Approved By			oppo

ｸﾞﾍｨﾔｭﾀ槙ｼ(Rev.H)ｸ　ﾂﾊｱｼ膣ep.29

ｿｿｽ　SBﾗ　ﾅﾖﾃ



USB SWITCH



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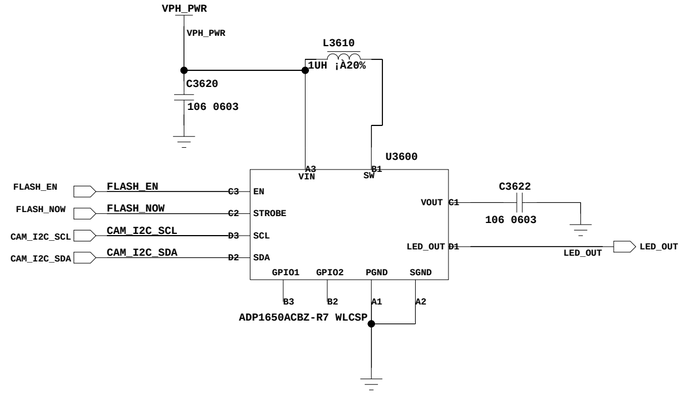
Flash LED Driver



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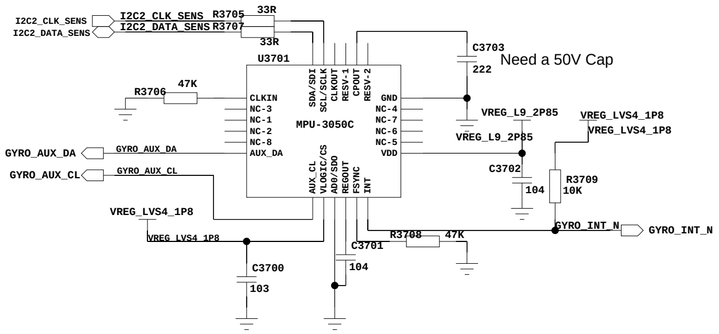
Approved By			

Gyro



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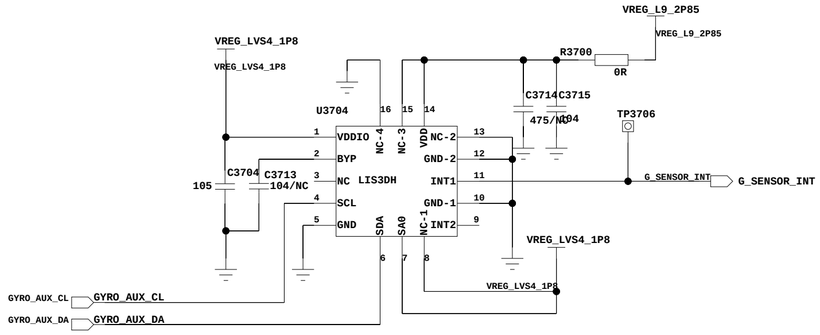
G-Sensor



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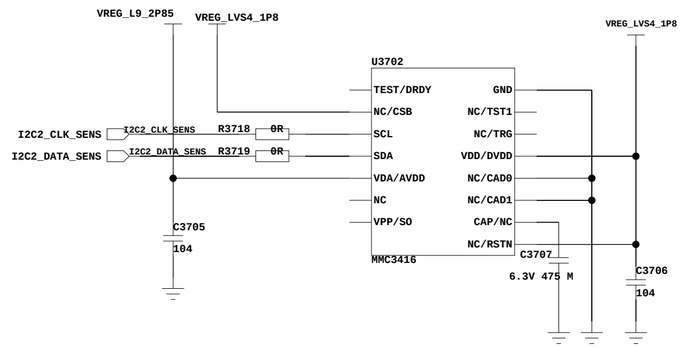
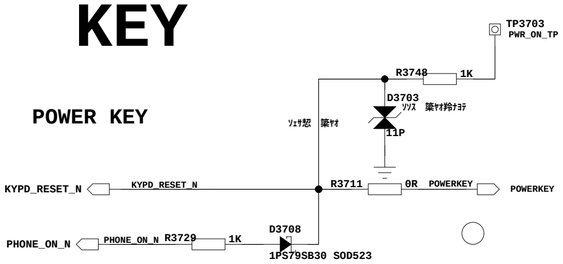
M-Sensor



I2C ADDRESS 0x30

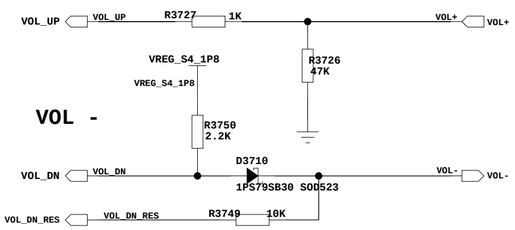
KEY

POWER KEY



VOL +

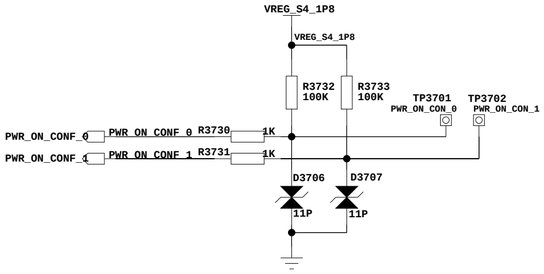
VOL -



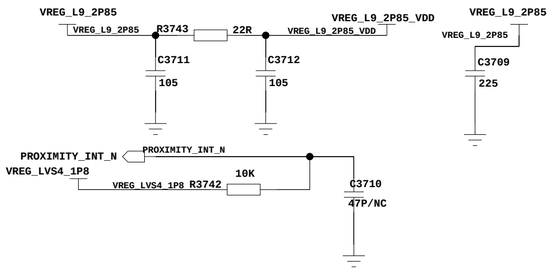
Test Confige

BOOT MODE

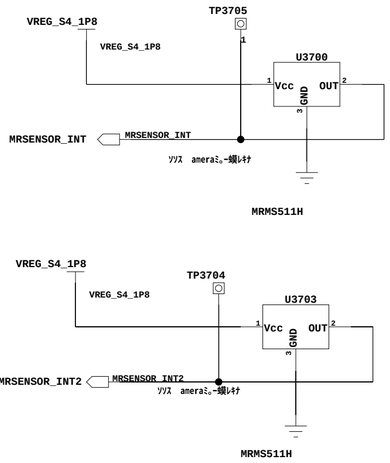
CONF_0	CONF_1	Mode
0	0	Factory Mode
0	1	WLAN Final Test
1	0	RF mode
1	1	Ordinary Power On



ALS+PS



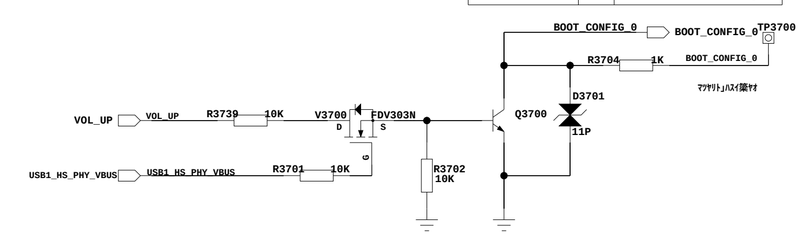
MR sensor



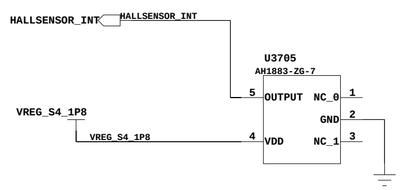
UPDATE

UPDATE

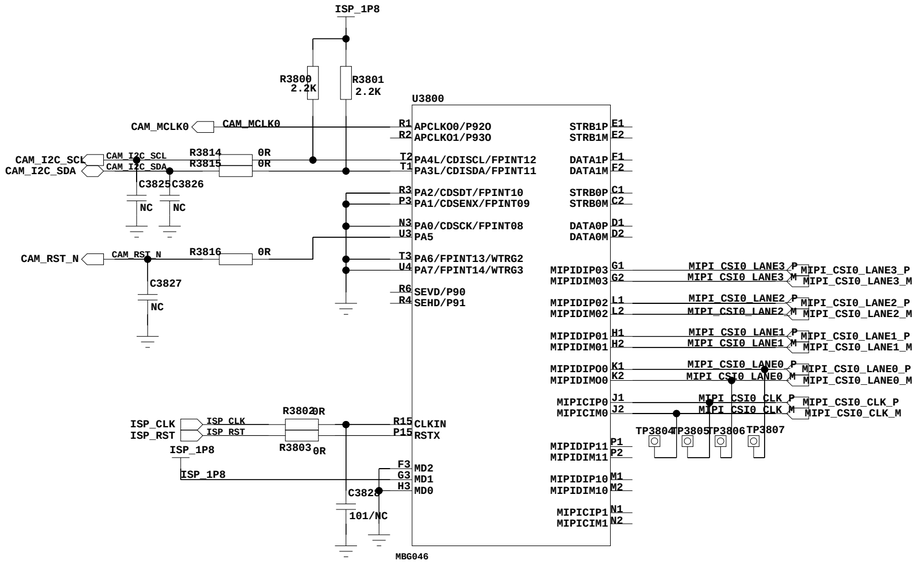
BOOT_CONFIG_0	0	Boot from eMMC
	1	Boot from SDC3 followed by SDC2

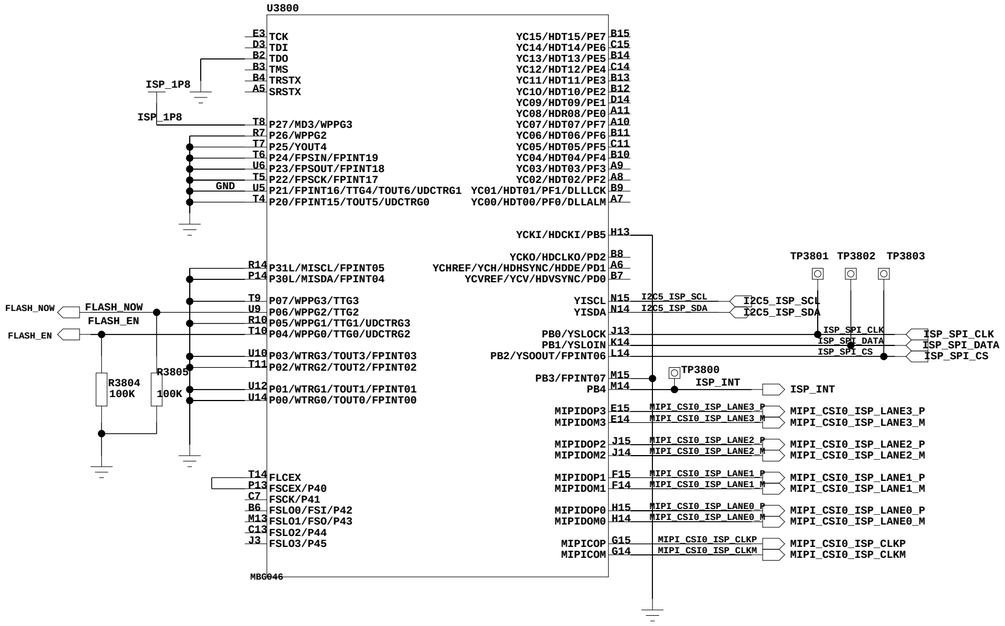


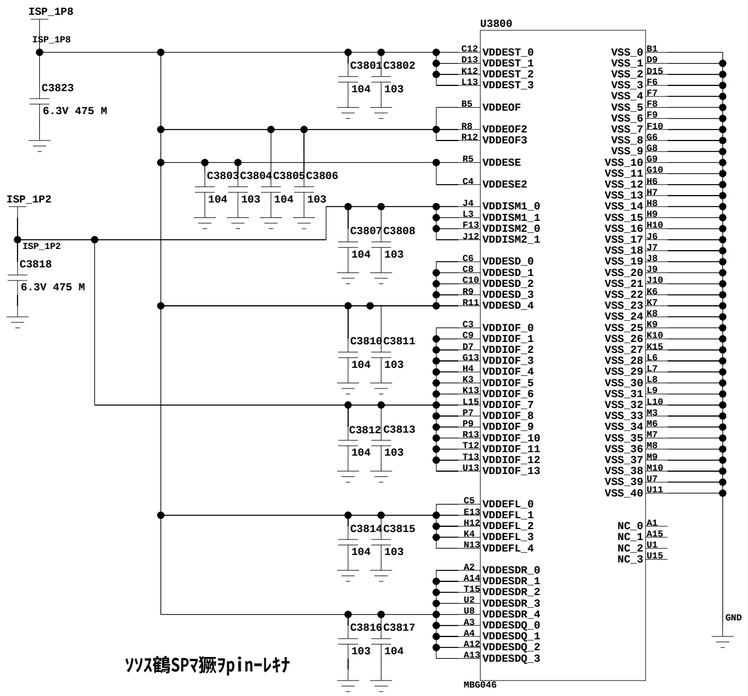
Hall sensor



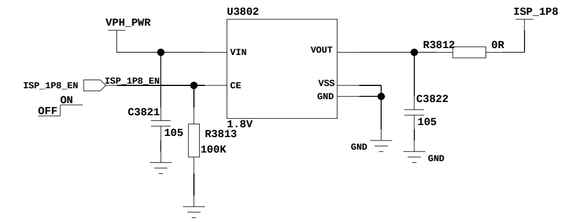
	Sign	Date	Type:
Drawn By			Draw No: 213005
Checked By			Sheet 27 of 27 Ver:
Standard By			
Approved By			

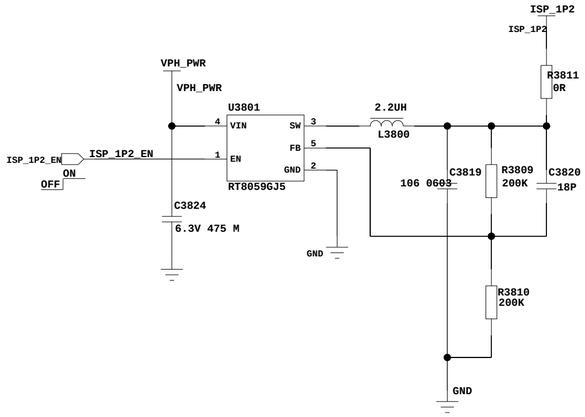






ソソス鶴SPマ豚ヲpin-レキナ





	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet of 3 Ver:
Standard By			
Approved By			

oppo

Blcok diagram

Primary Antenna

SWITCH SKY13404-466LF

Control

Control

SAW
B1 B2 B4
B5 B8
GSM850 900
DCS1800
PCS1900

PA
SKY77619
2G 3G

RF Transceiver
WTR1605

Analog baseband interfaces

Status & Control

128M LPDDR1
(Stacked Die)

MODEM Base-band Processor

MDM8215M

HSIC

IPC

SLIMbus

I2C2(GSBI2)

Ambient light Proximity sensor TMD27713

Gyro_sensor MPU6050

M-Sensor AK8975

SPEAKER
RECEIVE
Headphone

MIC1
MIC2
HP-MIC

AUDIO CODEC
WCD9310

2GB LPDDR2
(POP)

Applications Processor

APQ8064

BT_CTL

BT_DATA

BT_SSBI

BT

BT+WIFI
WCN3660

WIFI

WIFI+BT Antenna

WLAN command bus Interface

WLAN Analog Baseband IQ

NFC Antenna

I2C1(GSBI1)

NFC
PN650

I2C1(GSBI1)

SM358

I2C1(GSBI1)

BTP

SDC1

EMMC
THGBMAG7A2JBAIR P-VFBGA

USB

UART

SWITCH

USB/UART

USB
Micro 5P

ISP
MBG046

MIPI_CSI0 4Lanes

MIPI_CSI0 4Lanes

CAM I2C

MAIN CAMERA
SONY IMX135 13M

ISP I2C

CAM I2C

FLASH LED DRIVER
ADP1650

MIPI _DSI0 4 Lanes

I2C3(GSBI3) for TP

JDI 5.9¡± FHD LCD
Cap T.P:S3202

I2C3(GSBI3)

LCD Backlight
LCD ₀ϕ5V

SIM

UIM1

Supply Voltages

Supply Voltages

Supply Voltages

CTL

MDM_PSHOLD

PON_RESET

PM8018

19.2M XO

CTL

Supply Voltages

CTL

Supply Voltages

Supply Voltages

Supply Voltages

PM8821

reset

PM8921

Power_On

Battery

19.2M TCXO

32.768K XO

	Sign	Date	Type:
Drawn By			Draw No: A2SHEET
Checked By			Sheet 1 of 2 Ver:
Standard By			
Approved By			

oppo