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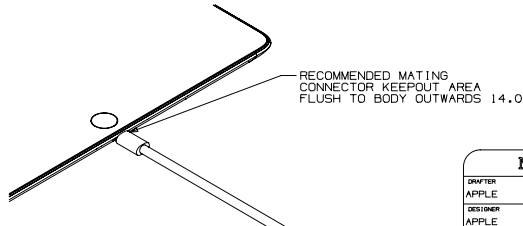
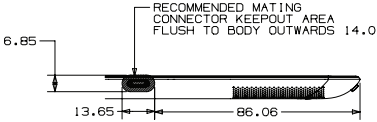
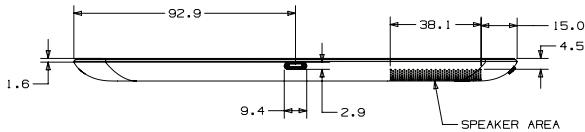
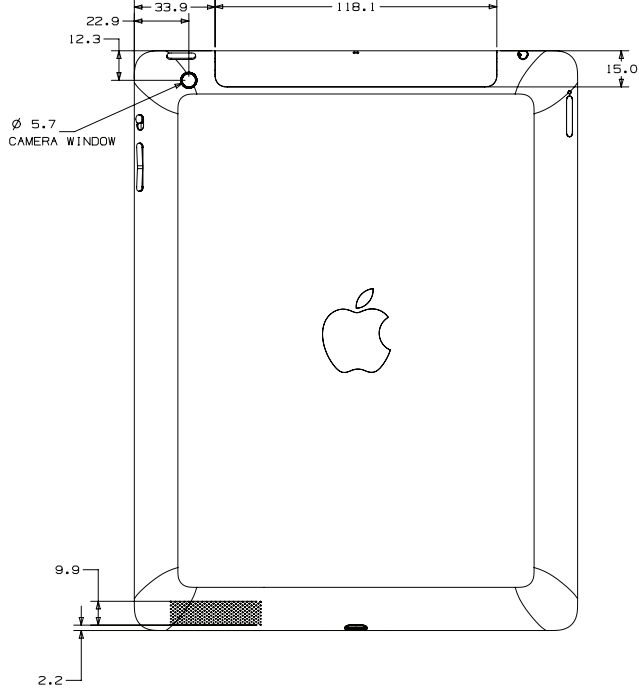
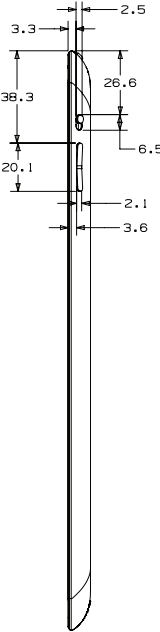
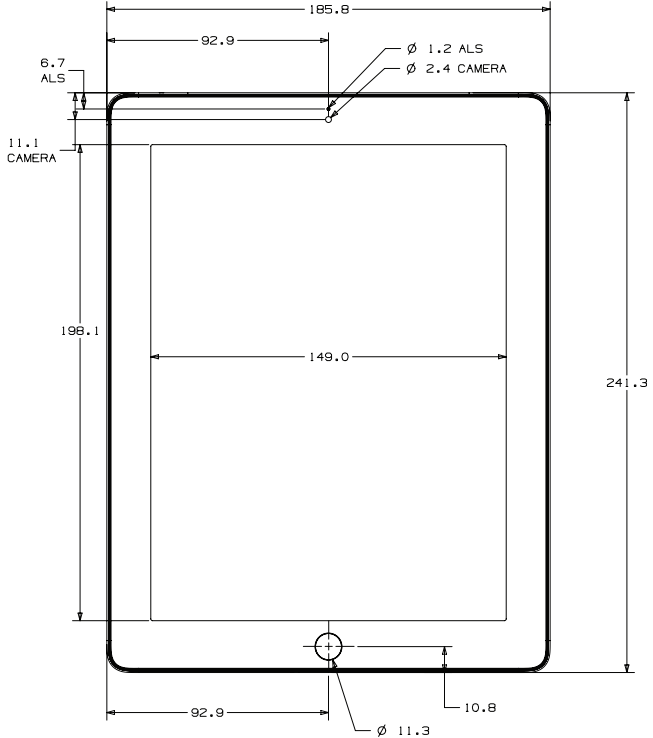
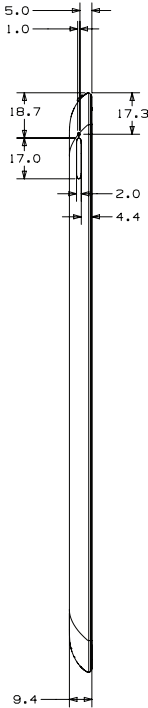
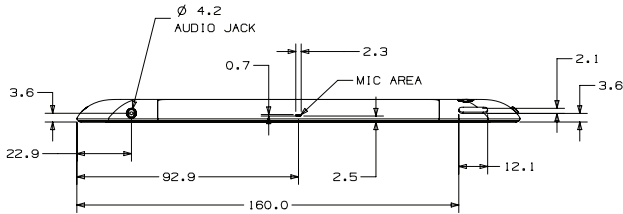
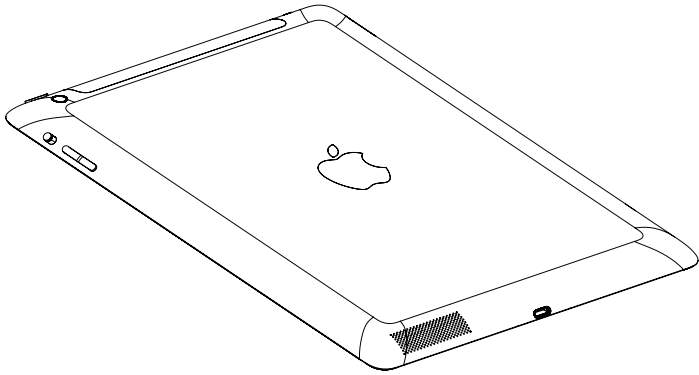
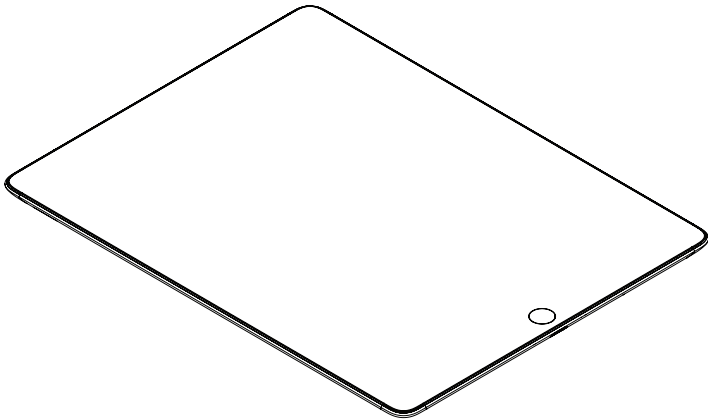
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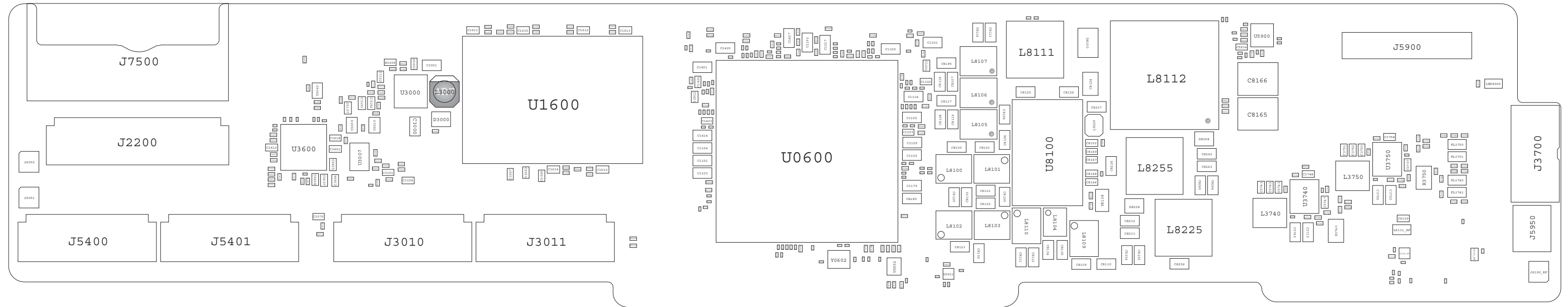
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NOTES (UNLESS OTHERWISE SPECIFIED)

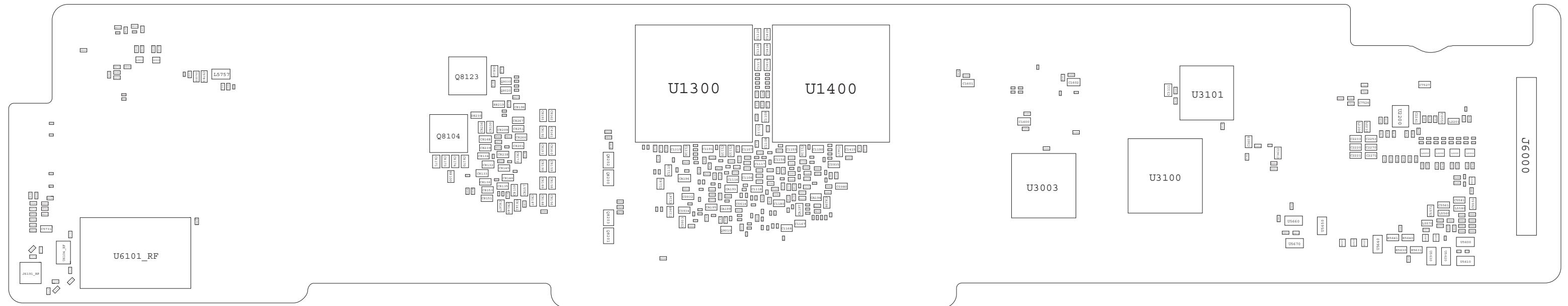


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REV.		REV.	
02		02	
SHEET		SHEET	
1		1	
OF 1		OF 1	

820-3249-TOP MLB



820-3249-BOT MLB



1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0001554595	PRODUCTION RELEASED	2012-07-26

iPad 4th Gen

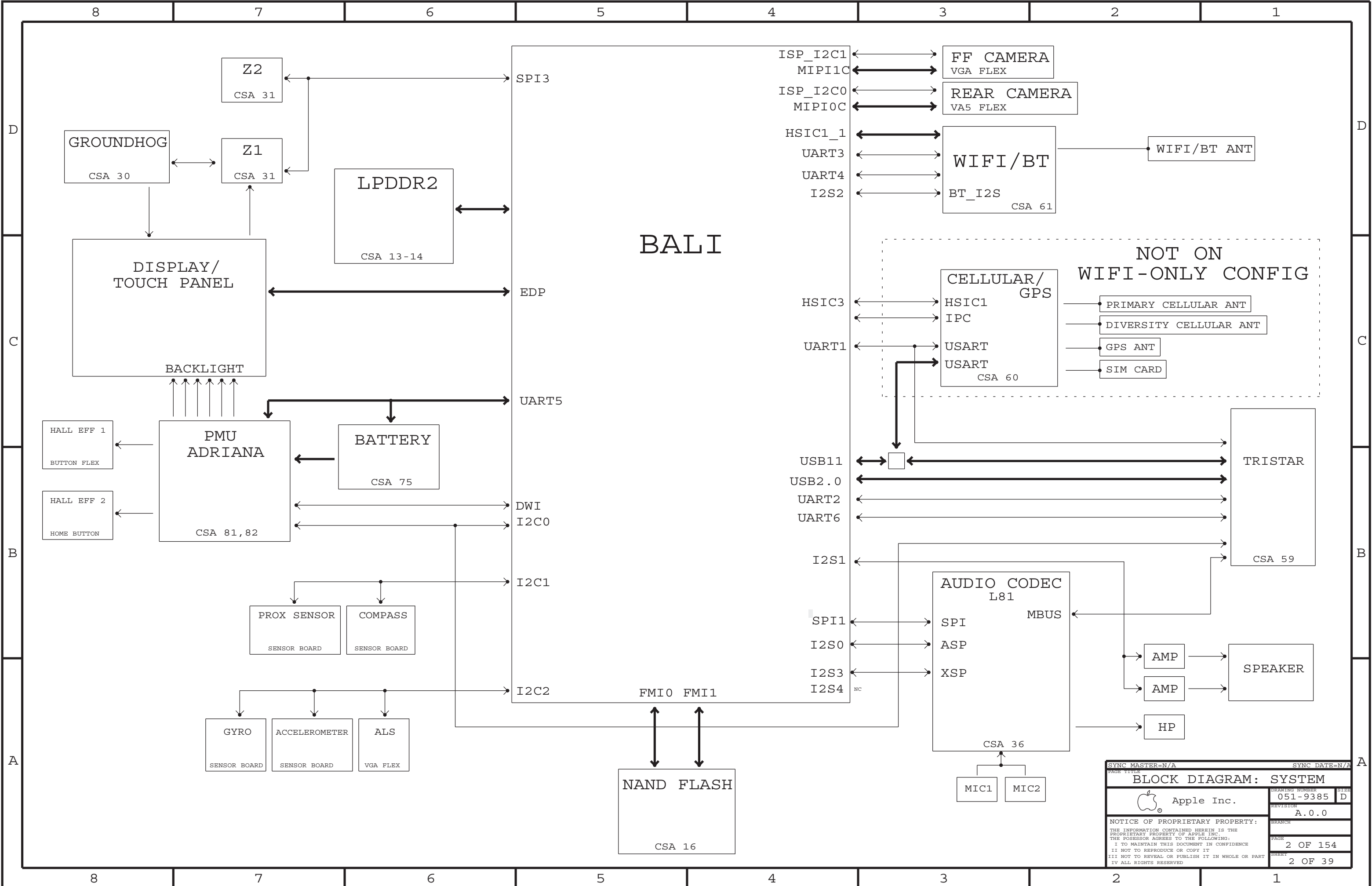
LAST_MODIFIED=Thu Jul 26 10:29:36 2012

PDF	CSA	CONTENTS	SYNC	MASTER	DATE	(SYSTEM DRI
1	1	Table of Contents	N/A	N/A		(AMANDA)
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A		(AMANDA)
3	4	BOM TABLES	N/A	N/A		(AMANDA)
4	6	AP: MAIN	N/A	N/A		(TERRY)
5	7	AP: I/Os	N/A	N/A		(AMANDA)
6	8	AP: NAND	N/A	N/A		(TERRY)
7	9	AP: TV,DP,MIPI	N/A	N/A		(TERRY)
8	10	AP: DDR	N/A	N/A		(TERRY)
9	11	AP: POWER	N/A	N/A		(TERRY)
10	12	AP: MISC & ALIASES	N/A	N/A		(TERRY)
11	13	DDR 0 AND 1	N/A	N/A		(TERRY)
12	14	DDR 2 AND 3	N/A	N/A		(TERRY)
13	16	NAND	N/A	N/A		(AMANDA)
14	21	ALIASES	N/A	N/A		(AMANDA)
15	22	VIDEO: EDP CONNECTOR	N/A	N/A		(JOE)
16	30	GRAPE: GROUNDHOG, CONN, BOOST	N/A	N/A		(AMANDA)
17	31	GRAPE: Z1, Z2	N/A	N/A		(AMANDA)
18	36	AUDIO: L81 CODEC	N/A	N/A		(TERRY)
19	37	AUDIO: SPEAKER AMP	N/A	N/A		(TERRY)
20	54	SENSOR FLEX CONN	N/A	N/A		(MARK)
21	55	SENSOR CONN FILTERS 1	N/A	N/A		(MARK)
22	56	SENSOR CONN FILTERS 2	N/A	N/A		(MARK)
23	57	E75 DOCK SUPPORT	N/A	N/A		(JOE)
24	58	IO FLEX CONN	N/A	N/A		(JOE)
25	59	TRISTAR	N/A	N/A		(JOE)
26	60	CONNECTOR: CELLULAR	N/A	N/A		(AMANDA)
27	61	WIFI/BT	N/A	N/A		(MATT)
28	75	POWER: BATTERY CONNECTOR	MADHAVI	12/06/2011		(MADHAVI)
29	81	PMU: ADRIANA PAGE 1	MADHAVI	12/06/2011		(MADHAVI)
30	82	PMU: ADRIANA PAGE 2	MADHAVI	12/06/2011		(MADHAVI)

PDF	CSA	CONTENTS	SYNC MASTER	DATE	(SYSTEM DRI
31	83	PMU: ADRIANA PAGE 3	MADHAVI	12/06/2011	(MADHAVI)
32	90	DEBUG/MISC.	MLB	11/09/2011	(AMANDA)
33	93	TEST/HOLES/FIDUCUALS	N/A	N/A	(AMANDA)
34	121	POWER ALIASES	N/A	N/A	(MADHAVI)
35	150	CONSTRAINTS: MLB RULES	MIKE	11/30/2011	(AMANDA)
36	151	CONSTRAINTS: LOW SPEED BUS	MIKE	11/30/2011	(AMANDA)
37	152	CONSTRAINTS: DISPLAY/AUDIO	MIKE	11/30/2011	(AMANDA)
38	153	CONSTRAINTS: DDR/FMI	MIKE	11/30/2011	(AMANDA)
39	154	CONSTRAINTS: POWER / GND	MIKE	11/30/2011	(AMANDA)

DRAWING
MLB
DRAWING

DRAWING TITLE		DRAWING NUMBER		SIZE
X140 MLB		051-9385		D
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

BOM OPTIONS

```
COMMON
ALTERNATE

16GB PROD: 16GB CONFIG
32GB-PROD: 32GB CONFIG
64GB-PROD: 64 GB CONFIG
DEV:-DEV BOARD ONLY
```

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MLB: MLB BOARD ONLY
MLB A: WIFI ONLY CONFIG
MLB B: CELLULAR CONFIG
MLB C: CELLULAR CONFIG
MLB D: LEGACY CELLULAR CONFIG
MLB E: LEGACY CELLULAR CONFIG
```

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

MECHANICAL PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
NAND	806-4195	1	FENCE,NAND, TOP,MLB,X140	PD_FENCE_NAND	CRITICAL	
SOC/PMU	806-3493	1	FENCE,LARGE, TOP,MLB,X140	PD_FENCE_LARGE	CRITICAL	
AUDIO	806-3956	1	FENCE,AMP,MLB,X140	PD_FENCE_AMP	CRITICAL	
GRAPE	806-4196	1	FENCE,1,BTM,MLB,X140	PD_FENCE_BTMT1	CRITICAL	
MEMORY	806-3492	1	FENCE,2,BTM,MLB,X140	PD_FENCE_BTMT2	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7838	1	EEEE FOR 639-3736 (MLB A 16G)	EEEE_F1WD	CRITICAL	EEEE_MLB_A_16G
825-7838	1	EEEE FOR 639-3737 (MLB A 32G)	EEEE_F1WH	CRITICAL	EEEE_MLB_A_32G
825-7838	1	EEEE FOR 639-3738 (MLB A 64G)	EEEE_F1W8	CRITICAL	EEEE_MLB_A_64G
825-7838	1	EEEE FOR 639-4176 (MLB A 128G)	EEEE_F8Q	CRITICAL	EEEE_MLB_A_128G
825-7838	1	EEEE FOR 639-3263 (MLB B 16G)	EEEE_DWGG	CRITICAL	EEEE_MLB_B_16G
825-7838	1	EEEE FOR 639-3739 (MLB B 32G)	EEEE_F1W7	CRITICAL	EEEE_MLB_B_32G
825-7838	1	EEEE FOR 639-3740 (MLB B 64G)	EEEE_F1WC	CRITICAL	EEEE_MLB_B_64G
825-7838	1	EEEE FOR 639-4177 (MLB B 128G)	EEEE_F8P	CRITICAL	EEEE_MLB_B_128G
825-7838	1	EEEE FOR 639-3741 (MLB C 16G)	EEEE_F1WG	CRITICAL	EEEE_MLB_C_16G
825-7838	1	EEEE FOR 639-3742 (MLB C 32G)	EEEE_F1WF	CRITICAL	EEEE_MLB_C_32G
825-7838	1	EEEE FOR 639-3743 (MLB C 64G)	EEEE_F1W9	CRITICAL	EEEE_MLB_C_64G
825-7838	1	EEEE FOR 639-4178 (MLB C 128G)	EEEE_F8OR	CRITICAL	EEEE_MLB_C_128G

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9385	1	SCH,MLB,X140	SCH1	CRITICAL	
820-3249	1	PCBF,MLB,X140	PCB1	CRITICAL	

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0598	1	IC, SOC, H5G, FCBGA1089, 0.5MM	U0600	CRITICAL	

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0622	1	IC, PMU, ADRIANA, D2018A1, FCBGA	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0636	2	LPDDR2, 533MHZ, 512MB, SAMSUNG, 35NM	U1300, U1400	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0637	333S0636		U1300, U1400	LPDDR2, 533MHZ, HYNIX, 38NM
333S0638	333S0636		U1400, U1400	LPDDR2, 533MHZ, ELPIDA, 38NM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0878	1	TOSHIBA PPN1.5 16GB	U1600	CRITICAL	16GB_PROD

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0879	1	TOSHIBA PPN1.5 32GB	U1600	CRITICAL	32GB_PROD

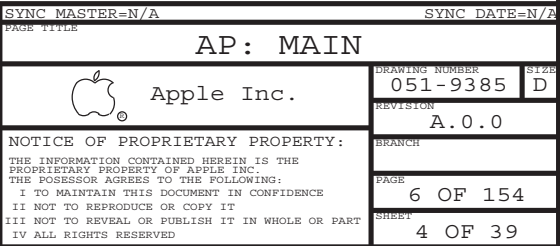
64GB FLASH CONFIGURATIONS

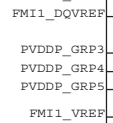
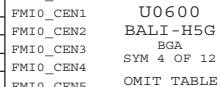
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335S0880	1	TOSHIBA PPN1.5 64GB	U1600	CRITICAL	64GB_PROD

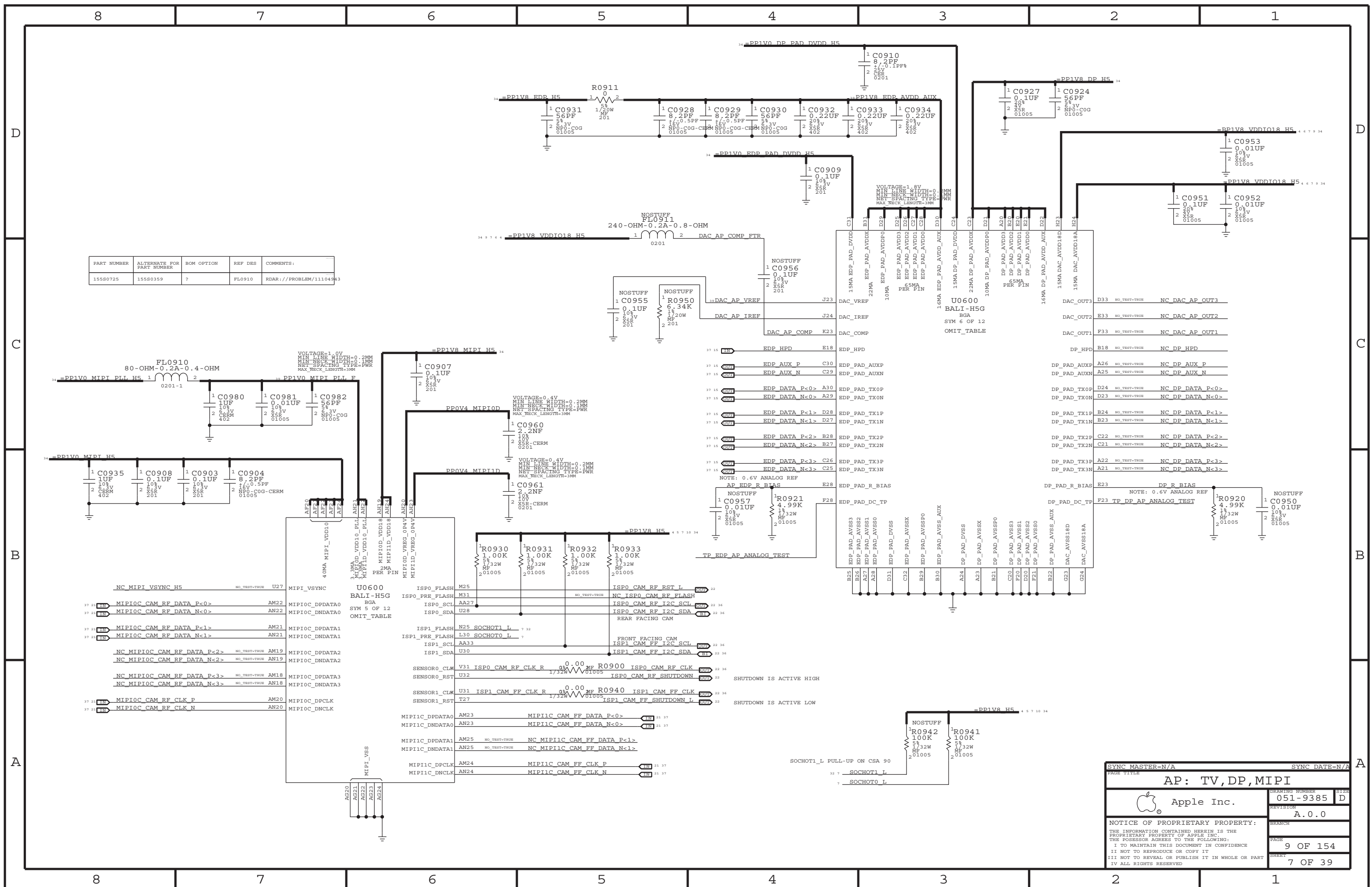
128GB FLASH CONFIGURATIONS

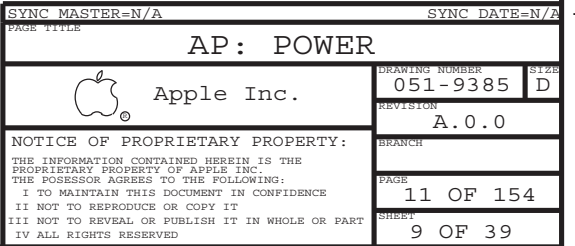
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0912	1	TOSHIBA PPN1.5 128GB	U1600	CRITICAL	128GB_PROD

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BOM TABLES			
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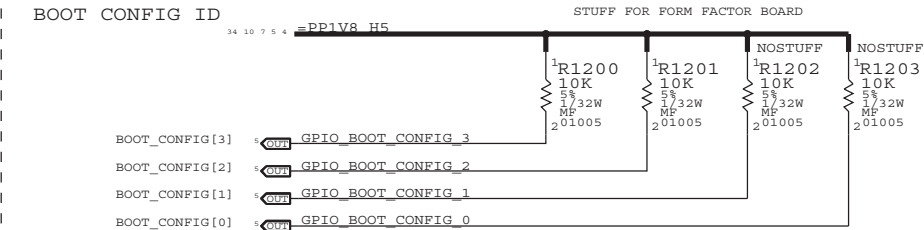
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BOOT_CONFIG[3-0]	S/W READ FLOW
1100 FMIO/1 2/2 CS	1. SET GPIO AS INPUT
1101 FMIO/1 4/4 CS	2. DISABLE PU AND ENABLE PD
1110 FMIO/1 4/4 CS WITH TEST	3. READ

FOR REFERENCE

BOOT_CONFIG[3:0]

0000 SPI0

0001 SPI1

0010 SPI0 W/TEST

0011 SPI1 W/TEST

0100 FMIO 2CS

0101 FMIO 4CS

0110 FMIO 4CS W/TEST

0111 RESERVED

1000 FMIO 2 CS

1001 FMIO 4 CS

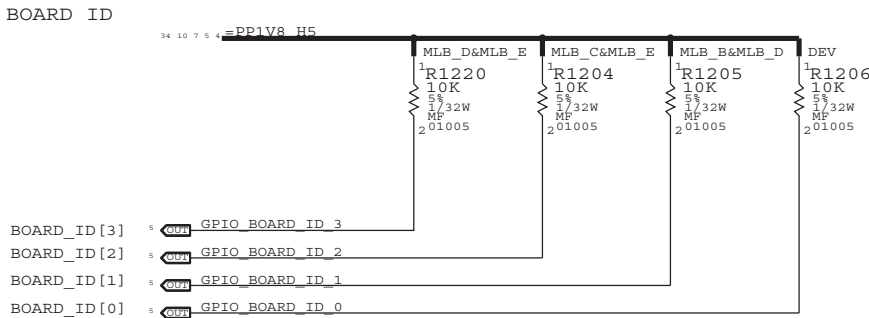
1010 FMIO 4CS W/TEST

1100 FMIO/1 2/2 CS

1101 FMIO/1 4/4 CS

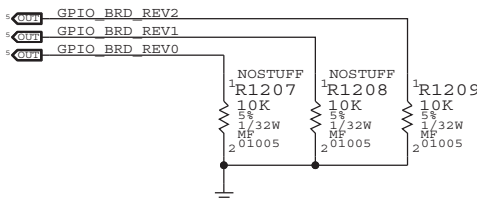
1110 FMIO/1 4/4 CS W/TEST

1111 RESERVED



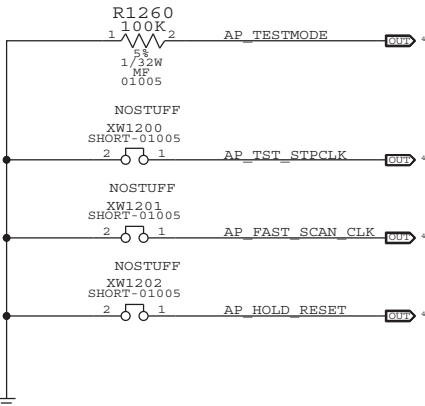
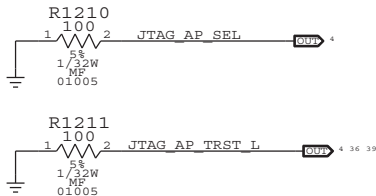
BOARD_ID[3-0]	S/W READ FLOW
0000 X140 AP WLAN (MLB A)	1. SET GPIO AS INPUT
0001 X140 DEV WLAN	2. DISABLE PU AND ENABLE PD
0010 X140 AP BB_41 (MLB B)	3. READ
0011 X140 DEV BB_41	
0100 X140 AP BB_42 (MLB C)	
0101 X140 DEV BB_42	
1010 X140 AP BB_26A (MLB D)	
1011 X140 DEV BB_26A	
1110 X140 AP BB_26 (MLB E)	
1111 X140 DEV BB_26	

BOARD REVISION

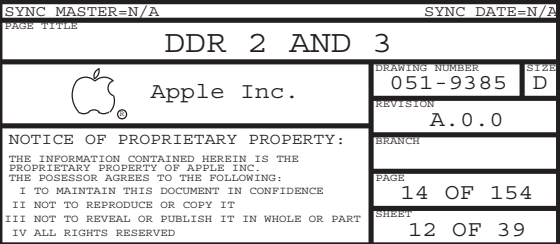


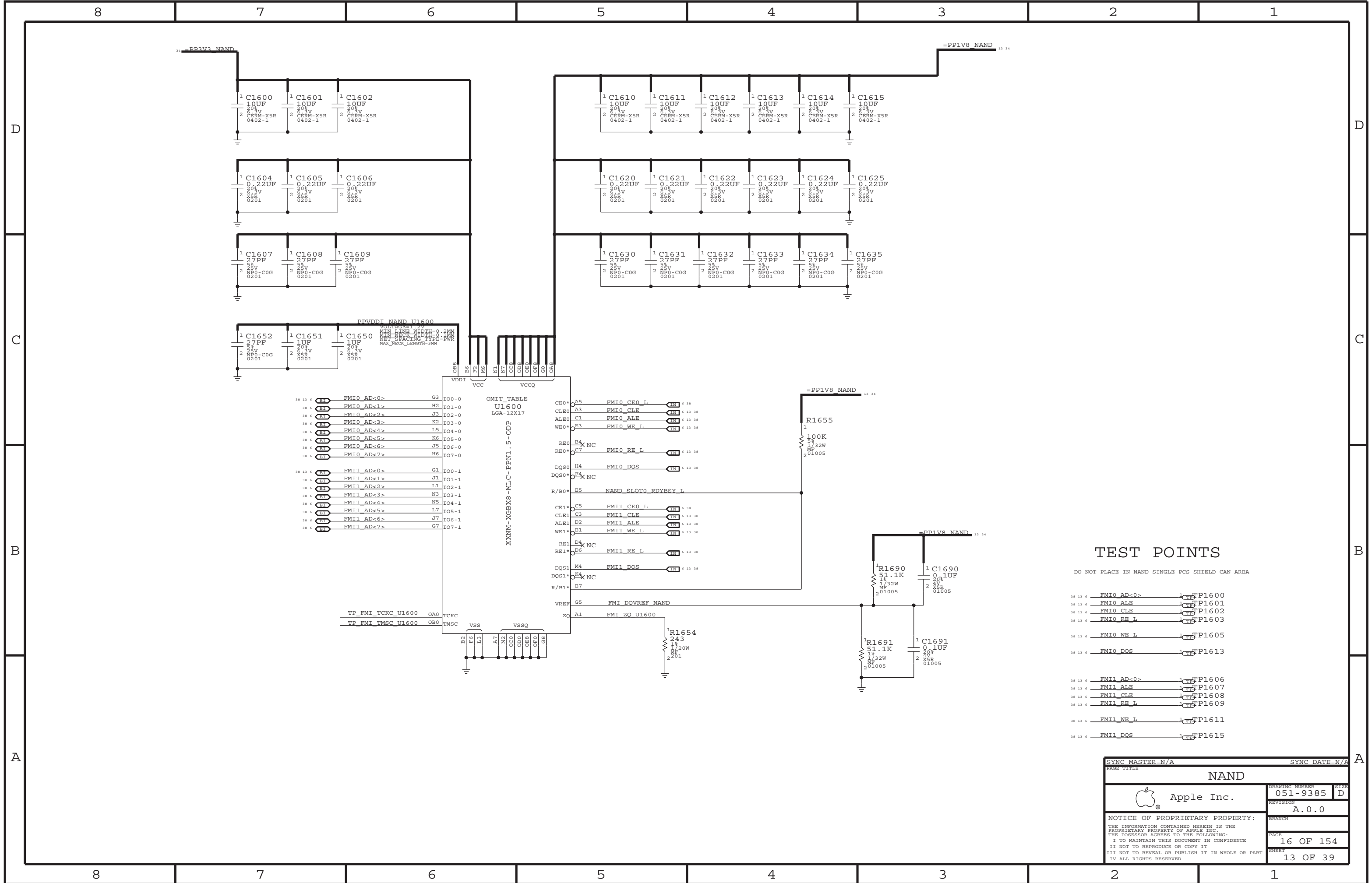
BRD_REV[2-0]	S/W READ FLOW
000 PROTO	1. SET GPIO AS INPUT
001 PROTO 2	2. ENABLE PU AND DISABLE PD
010 EVT	3. READ
011 DVT	

JTAG



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TEST POINTS

DO NOT PLACE IN NAND SINGLE PCS SHIELD CAN AREA

38 13 6	FMIO_AD<0>	1	TP1600
38 13 6	FMIO_ALE	1	TP1601
38 13 6	FMIO_CLE	1	TP1602
38 13 6	FMIO_RE_L	1	TP1603
38 13 6	FMIO_WE_L	1	TP1605
38 13 6	FMIO_DQS	1	TP1613
38 13 6	FMII_AD<0>	1	TP1606
38 13 6	FMII_ALE	1	TP1607
38 13 6	FMII_CLE	1	TP1608
38 13 6	FMII_RE_L	1	TP1609
38 13 6	FMII_WE_L	1	TP1611
38 13 6	FMII_DQS	1	TP1615

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WIFI ALIASES

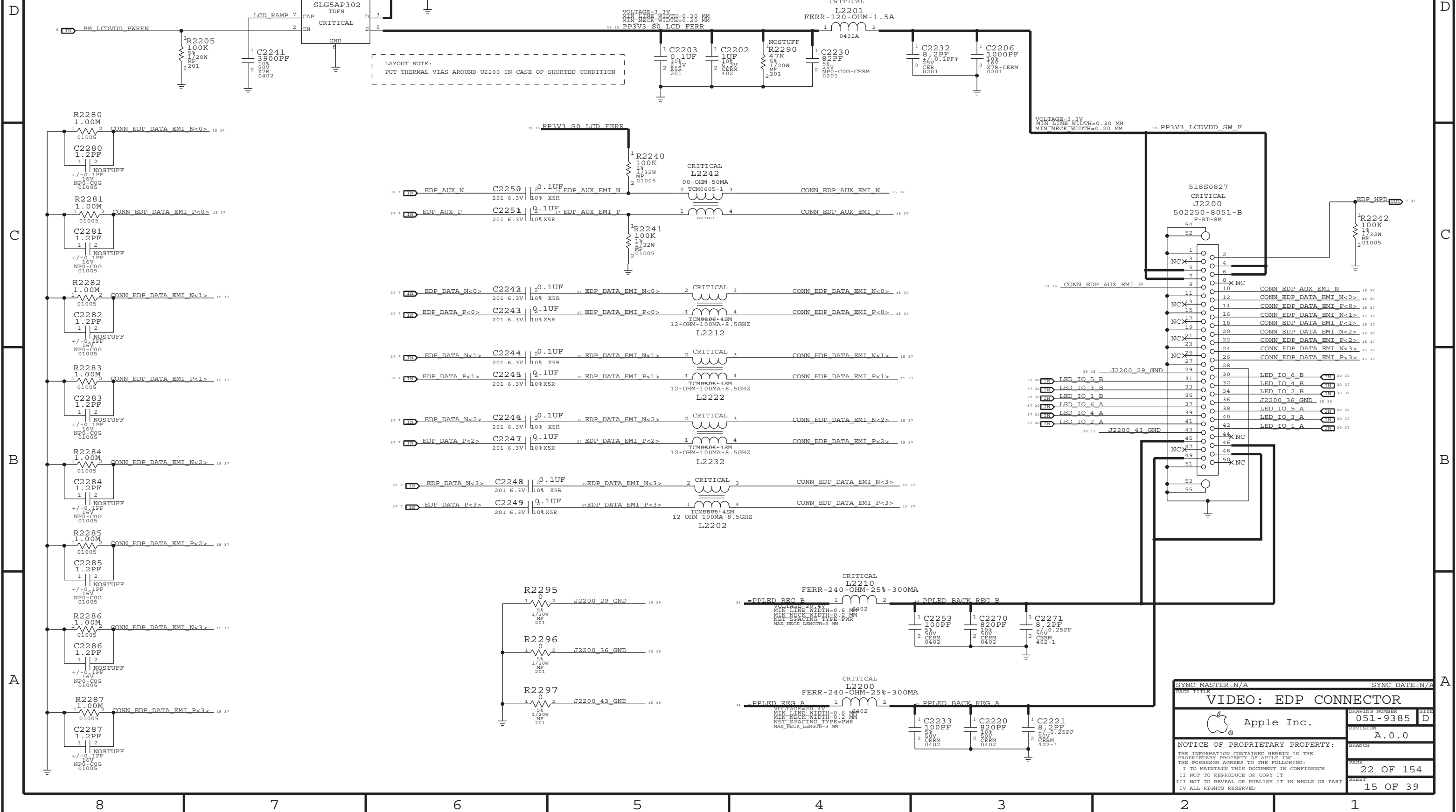
36	4	HSIC1 WLAN_DATA	MAKE_BROG-TX00	50	HSIC WLAN_DATA	27
36	4	HSIC1 WLAN_STB	MAKE_BROG-TX00	50	HSIC WLAN STROBE	27
36	5	GPIO WLAN_HSIC_HOST_RDY	MAKE_BROG-TX00	AP	HSIC3_RDY	27
36	5	GPIO WLAN_HSIC_DEV_RDY	MAKE_BROG-TX00	DEV	HSIC3_RDY	27
30		PMU_GPIO WLAN_REG_ON	MAKE_BROG-TX00	WLAN	REG_ON	27
30		PMU_GPIO WLAN_HOST_WAKE	MAKE_BROG-TX00	HOST	WAKE WLAN	27
30		PMU_GPIO_BT_REG_ON	MAKE_BROG-TX00	BT	REG_ON	27
30		PMU_GPIO_BT_HOST_WAKE	MAKE_BROG-TX00	HOST	WAKE_BT	27
5		GPIO_BT_WAKE	MAKE_BROG-TX00	BT	WAKE	27
36	5	UART3_BT_RXD	MAKE_BROG-TX00	BT	UART_TXD	27
36	5	UART3_BT_TXD	MAKE_BROG-TX00	BT	UART_RXD	27
36	5	UART3_BT_CTS_L	MAKE_BROG-TX00	BT	UART_RTS_L	27
36	5	UART3_BT_RTS_L	MAKE_BROG-TX00	BT	UART_CTS_L	27
36	30	PMU_GPIO_CLK_32K_WLAN	MAKE_BROG-TX00	CLK32K	AP	27
36	5	I2S2_BT_BCLK	MAKE_BROG-TX00	BT	PCM_CLK	27
36	5	I2S2_BT_DOUT	MAKE_BROG-TX00	BT	PCM_IN	27
36	5	I2S2_BT_DIN	MAKE_BROG-TX00	BT	PCM_OUT	27
36	5	I2S2_BT_LRCK	MAKE_BROG-TX00	BT	PCM_SYNC	27
36	5	UART4_WLAN_RXD	MAKE_BROG-TX00	WLAN	UART_TXD	27
36	5	UART4_WLAN_TXD	MAKE_BROG-TX00	WLAN	UART_RXD	27
5		GPIO_WL_HSIC_RESUME	MAKE_BROG-TX00	WLAN	HSIC3_RESUME	27
34		VDDIO_WLAN_BT_1V8	MAKE_BROG-TX00	PP_WL_BT	VDDIO_AP	27

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EDP CONNECTOR

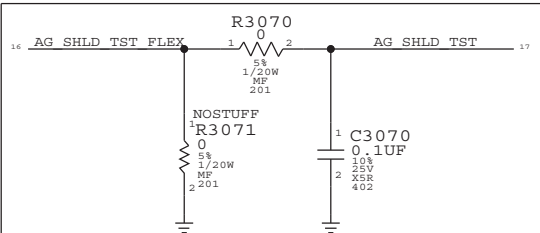
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS :
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155S0625	155S0559	L2202, L2212, L2232	L2222, L2232	RDAR://PROBLEM/901759

RADAR://PROBLEM/9015335



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

CONNECTORS TO GRAPE FLEX



P/N 518S0828

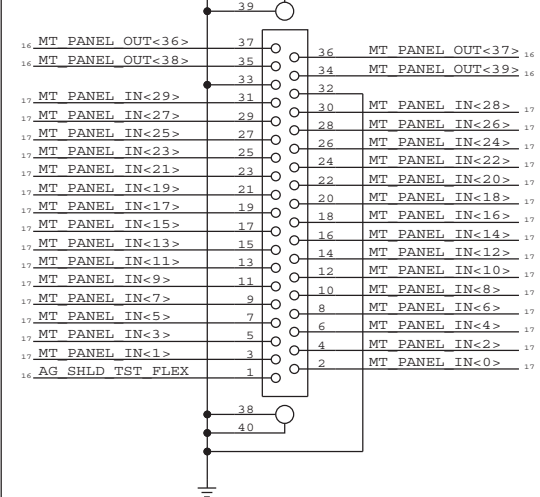
MATES WITH LEFTMOST GRAPE FLEX TAIL

CRITICAL

J3010

502250-8037-B

F-RT-SM



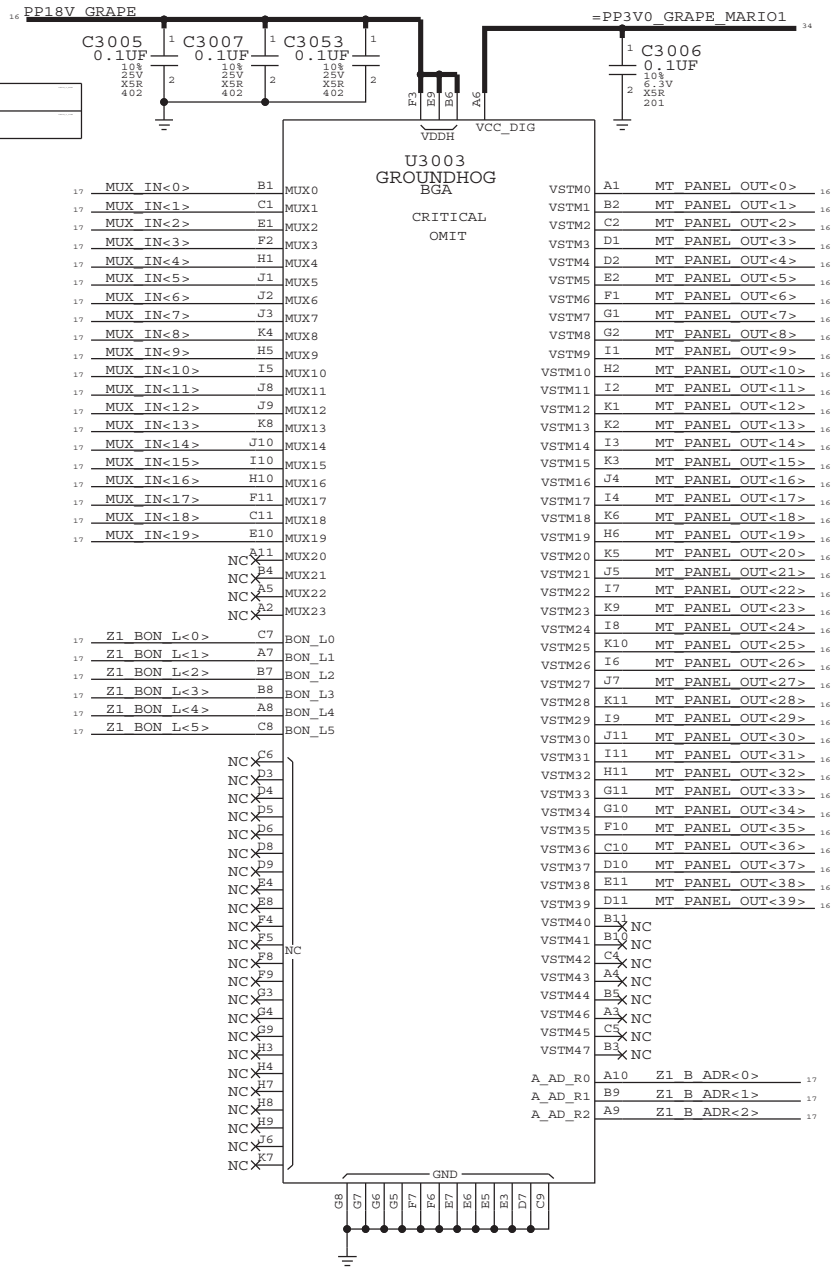
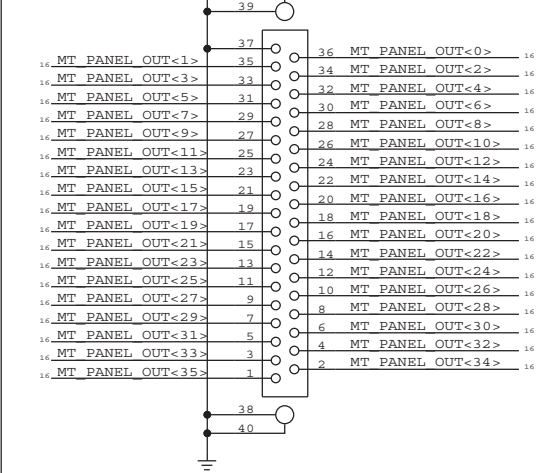
MATES WITH RIGHTMOST GRAPE FLEX TAIL

CRITICAL

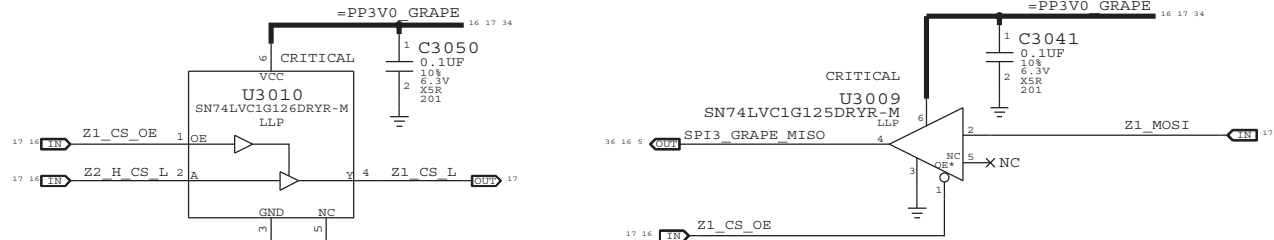
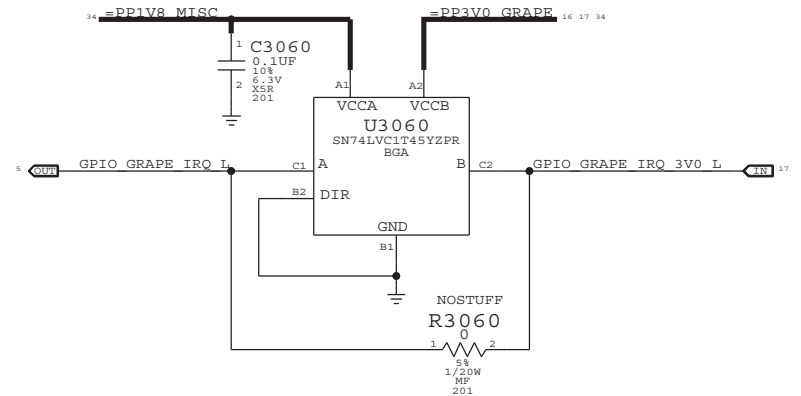
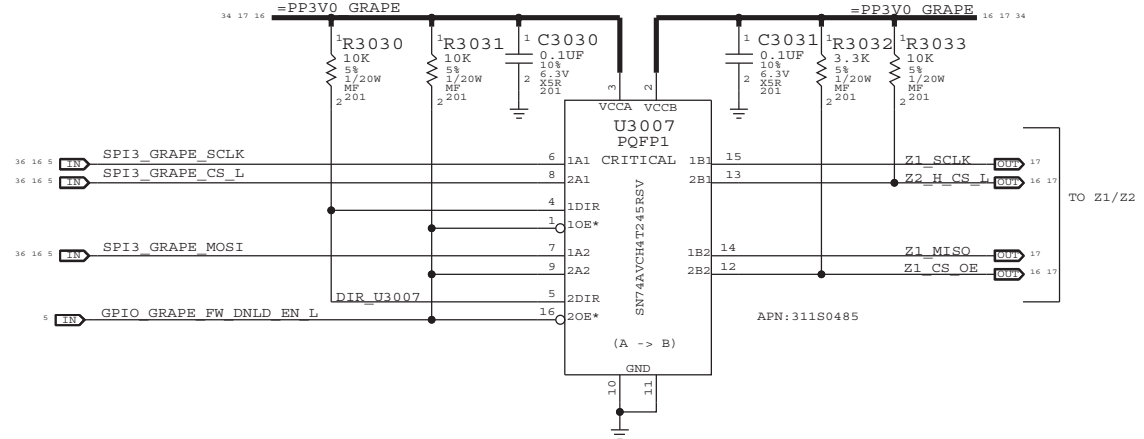
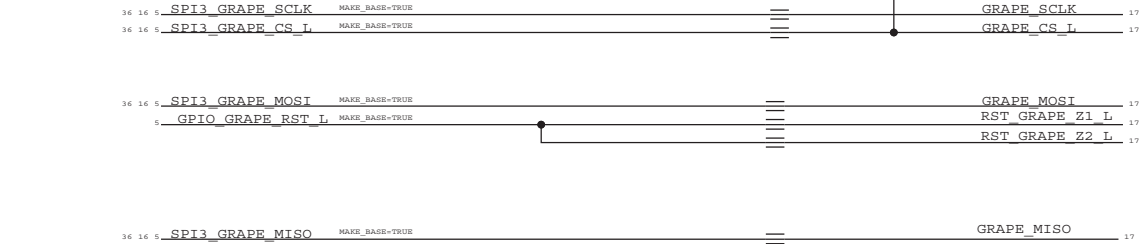
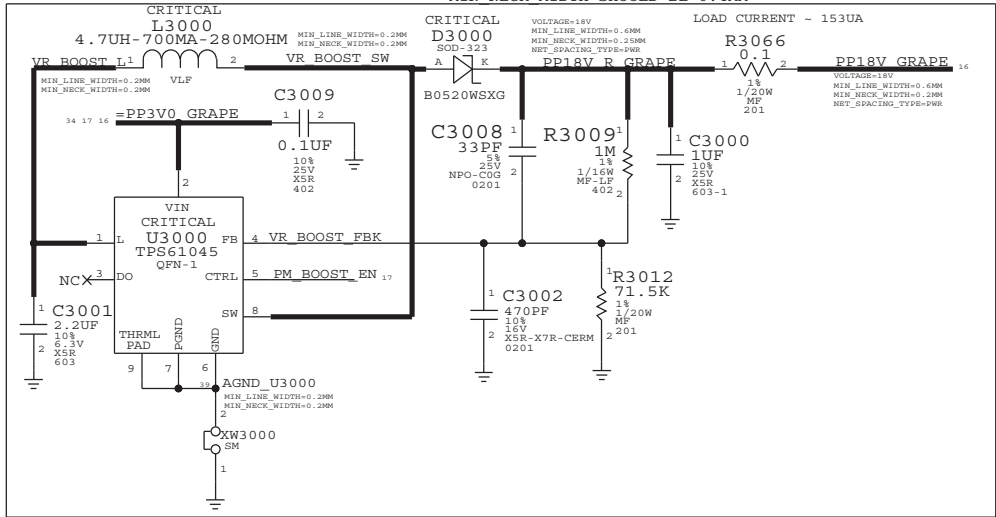
J3011

502250-8037-B

F-RT-SM

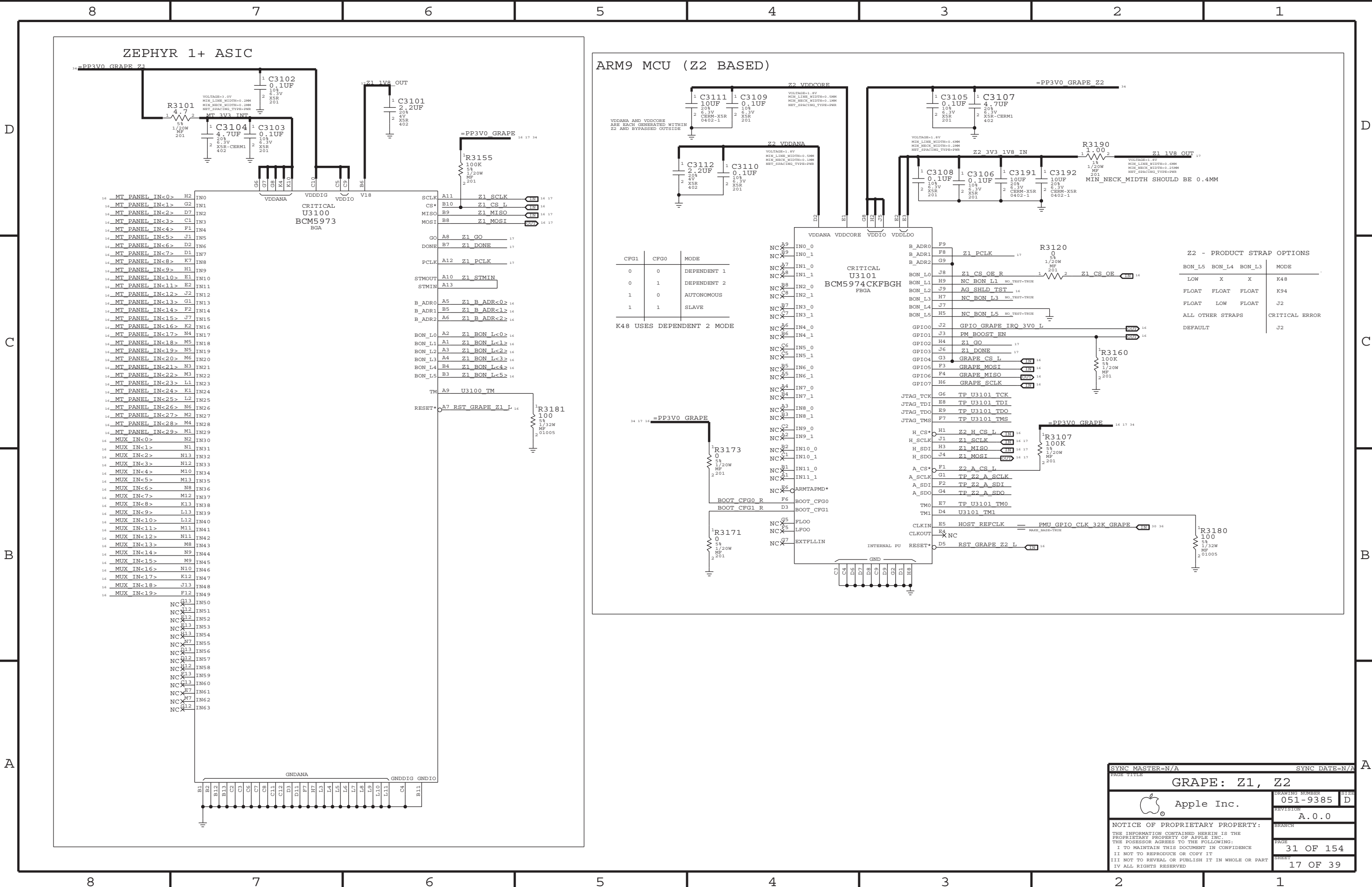


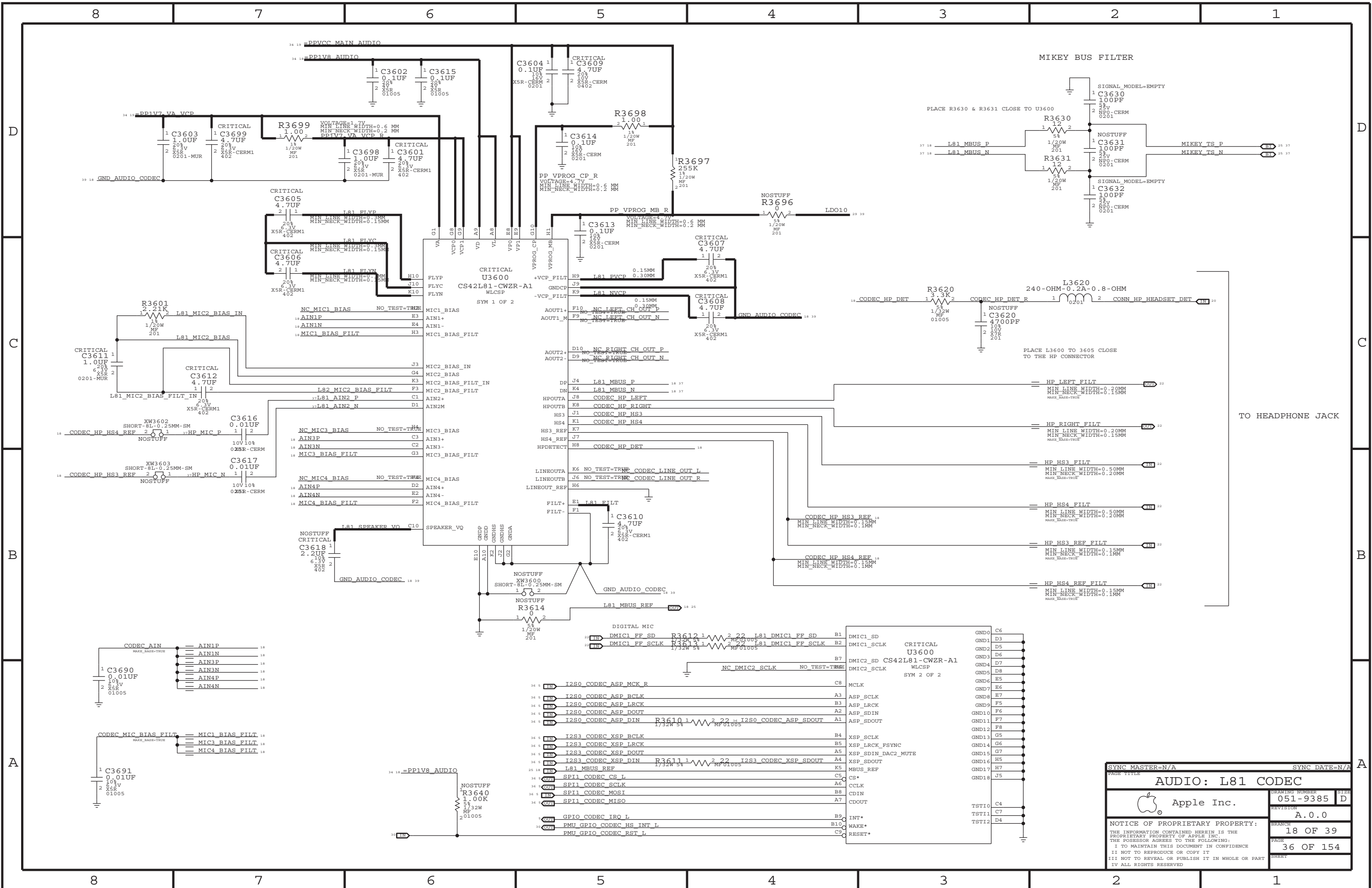
BOOST CONVERTOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

PAGE TITLE		SYNC DATE=N/A	
GRAPE: GROUNDHOG, CONN, BOOST		DRAWING NUMBER	
Apple Inc.		051-9385	
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IV ALL RIGHTS RESERVED		SHEET	
		16 OF 39	

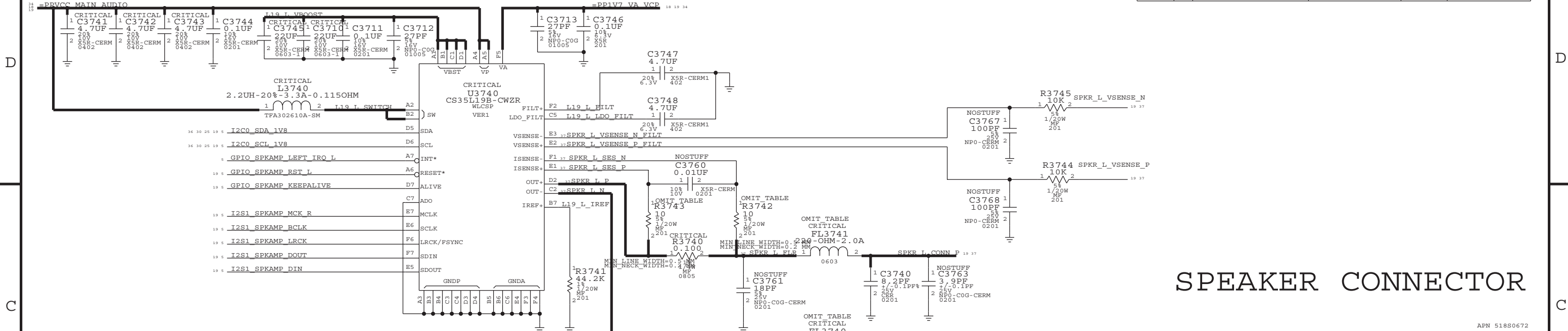




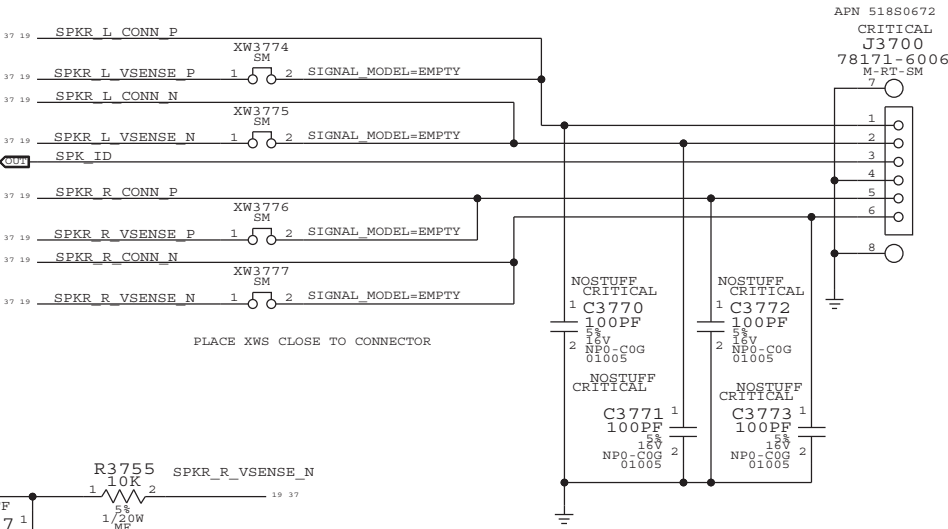
LEFT SPEAKER AMP

I2C ADDRESS: 1000000X

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0002	4	RES,MP,1/20W,0.00HM,5,0201,SMD	R3742,R3743,R3752,R3753	?	?
113S0022	4	RES,MP,1/10W,00HM,5,0603,SMD,LF	FL3740,FL3741,FL3750,FL3751	?	?

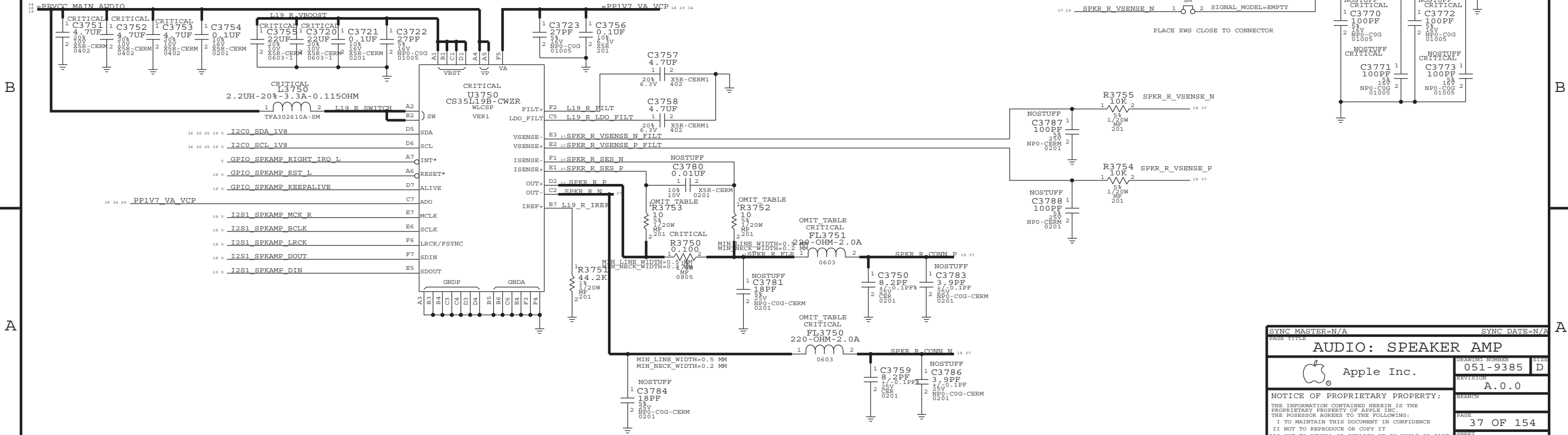


SPEAKER CONNECTOR

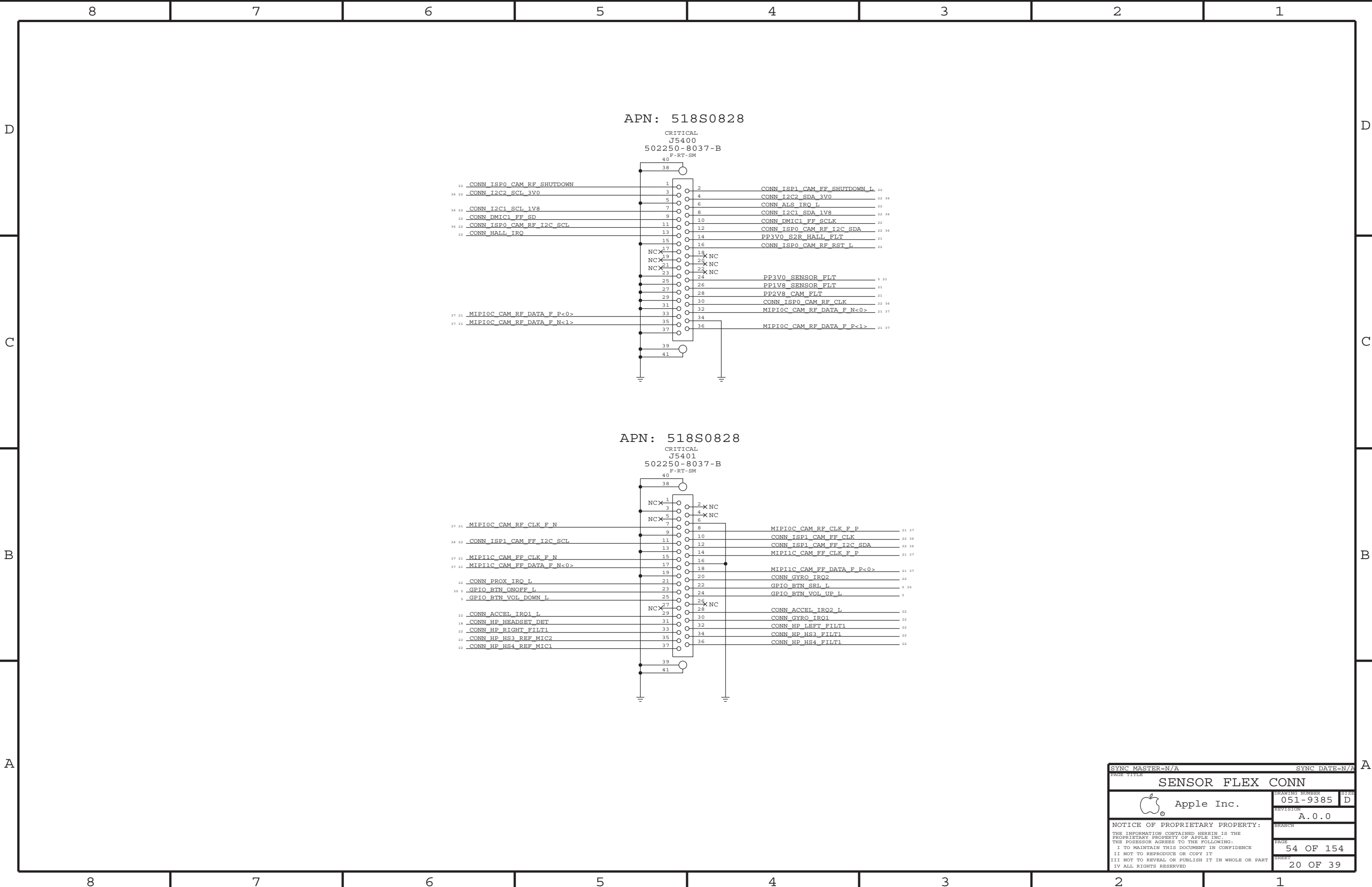


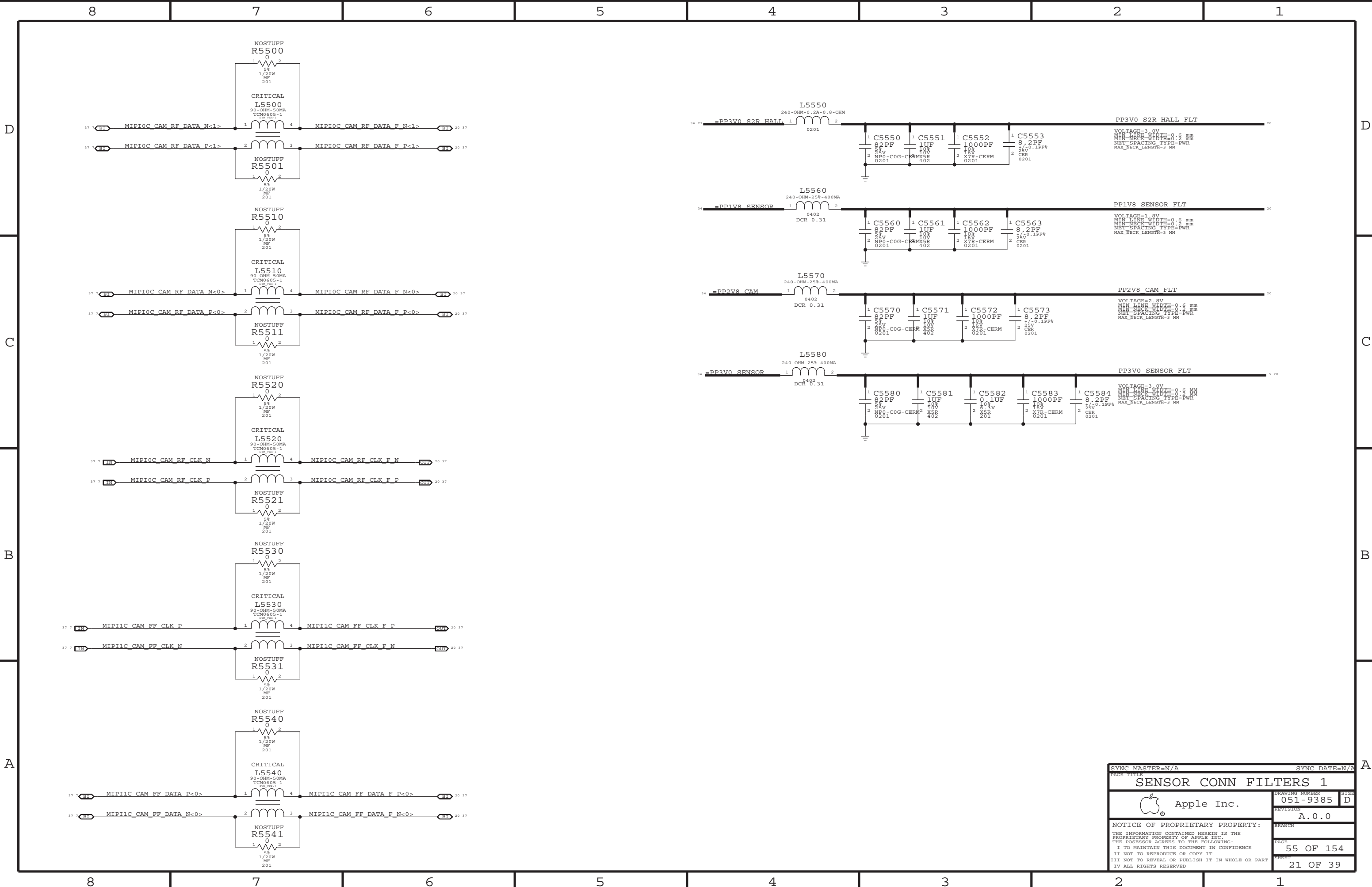
RIGHT SPEAKER AMP

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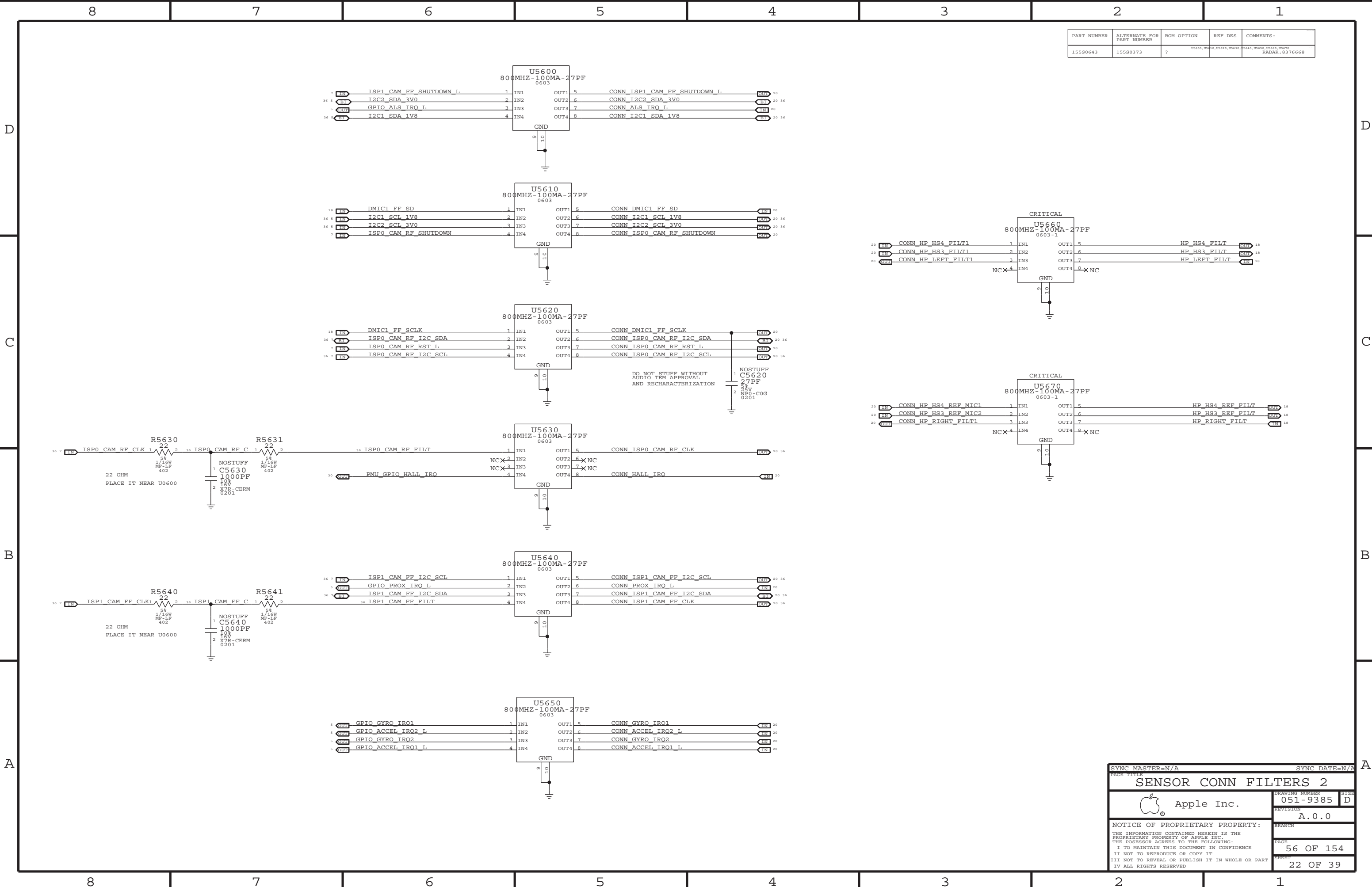


SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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		REVISION	A.0.0
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		PAGE	37 OF 154
		SHEET	19 OF 39





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 Apple Inc.		DRAWING NUMBER	051-9385
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		PAGE	55 OF 154
		SHEET	21 OF 39



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0643	155S0373	?	U5600, U5610, U5620, U5630, U5640, U5650, U5660, U5670	RADAR: 8376668

SYNC MASTER=N/A

SYNC DATE=N/A

SENSOR CONN FILTERS 2

Apple Inc.

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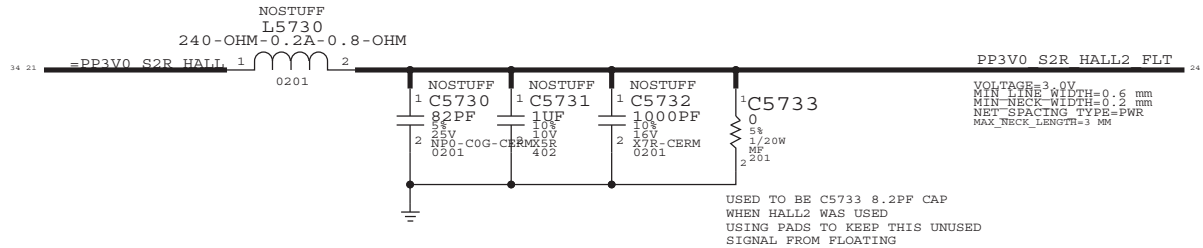
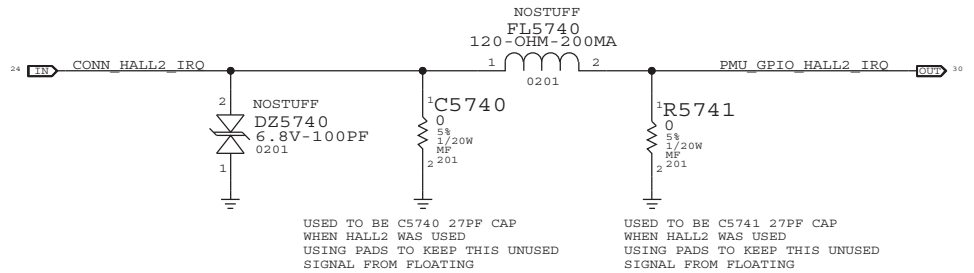
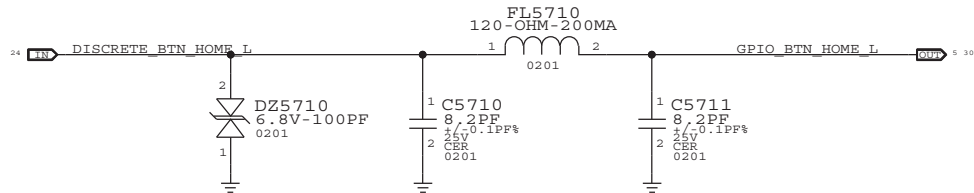
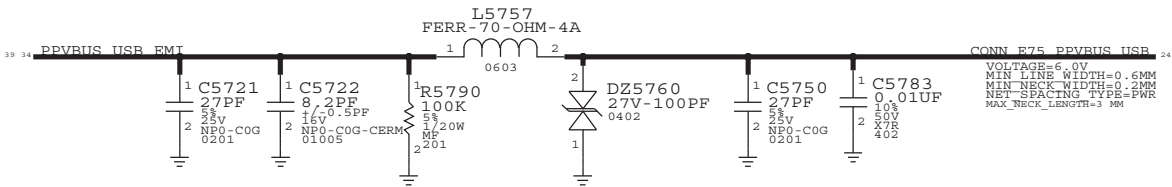
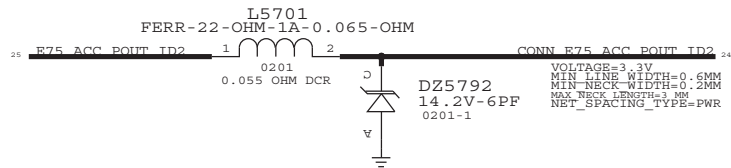
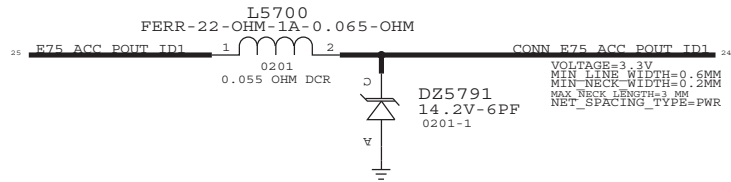
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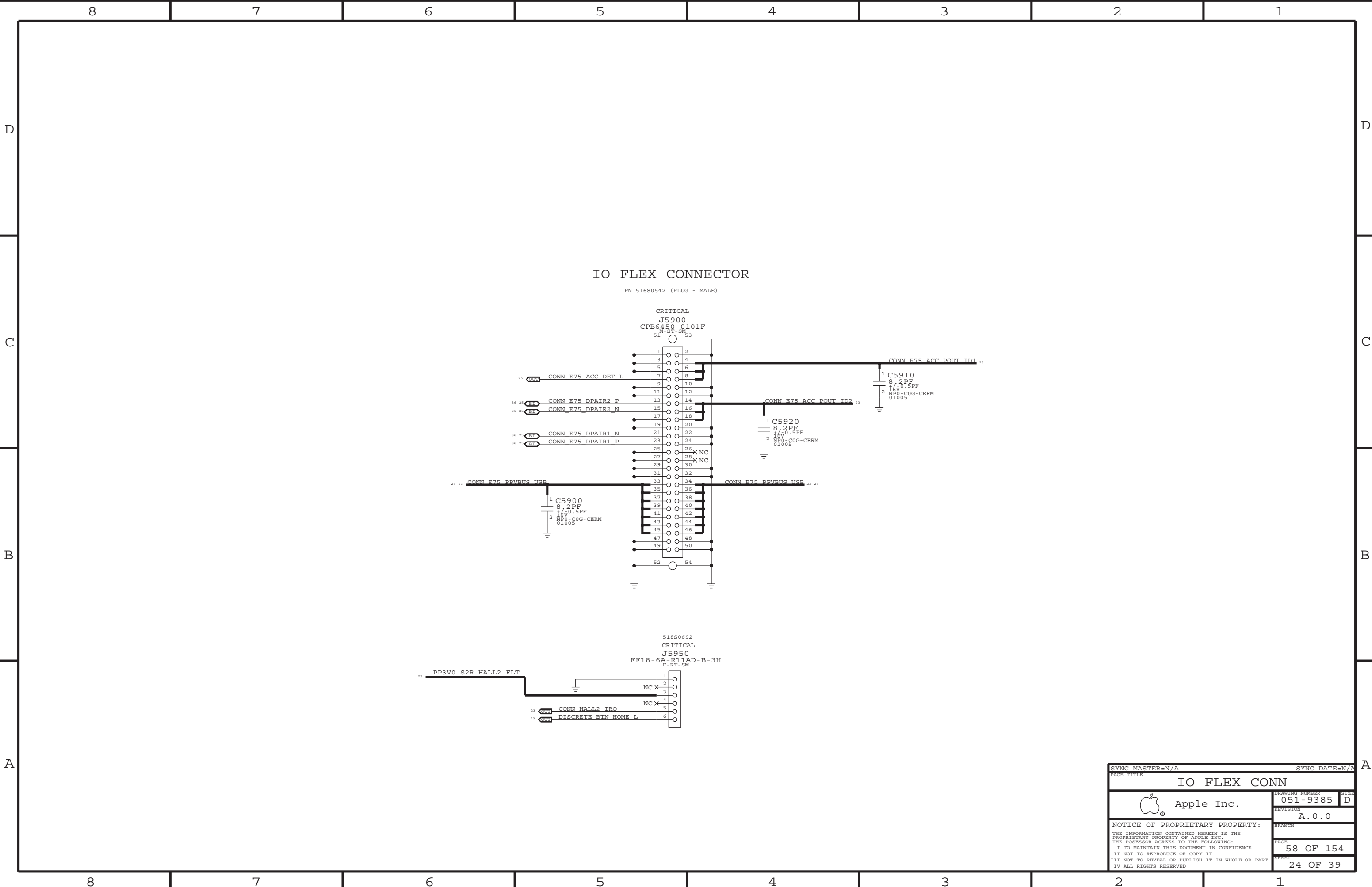
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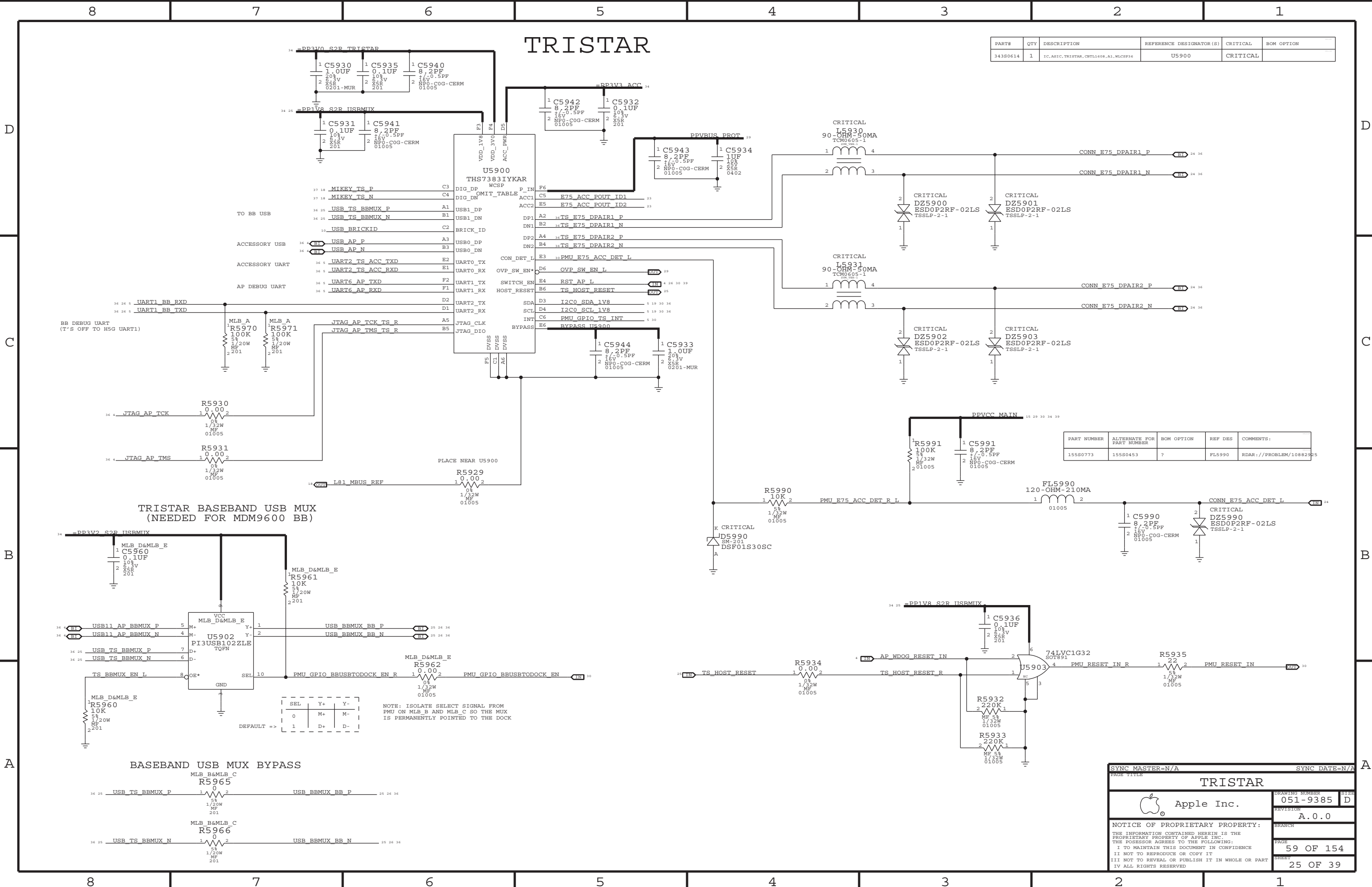
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ5760	RDAR://PROBLEM/8370432
155S0320	155S0513		L5700,L5701	RDAR://PROBLEM/9625601
155S0657	155S0537		FL5710,FL5750	
155S0741	155S0397		L5757	RDAR://PROBLEM/11238841

SYNC MASTER=N/A		SYNC DATE=N/A	
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E75 DOCK SUPPORT			
 Apple Inc.		DRAWING NUMBER	051-9385
		SIZE	D
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		PAGE	57 OF 154
		SHEET	23 OF 39

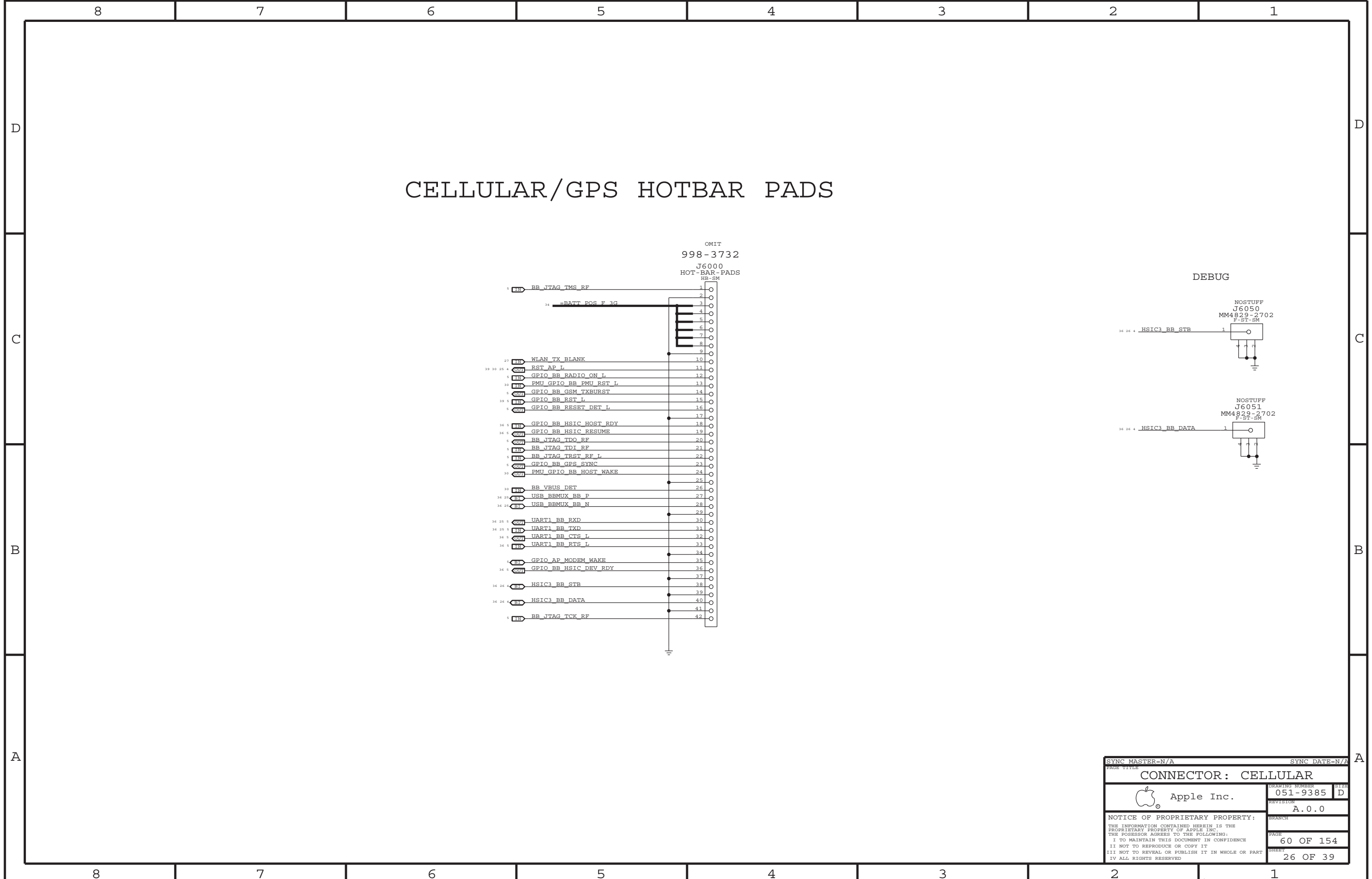




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0614	1	IC, ASIC, TRISTAR, CRTL1608, A1, WLCSP36	U5900	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15550773	15550453	?	FL5990	RDAR://PROBLEM/10882925

PAGE TITLE		SYNC DATE=N/A	
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WLAN/BT

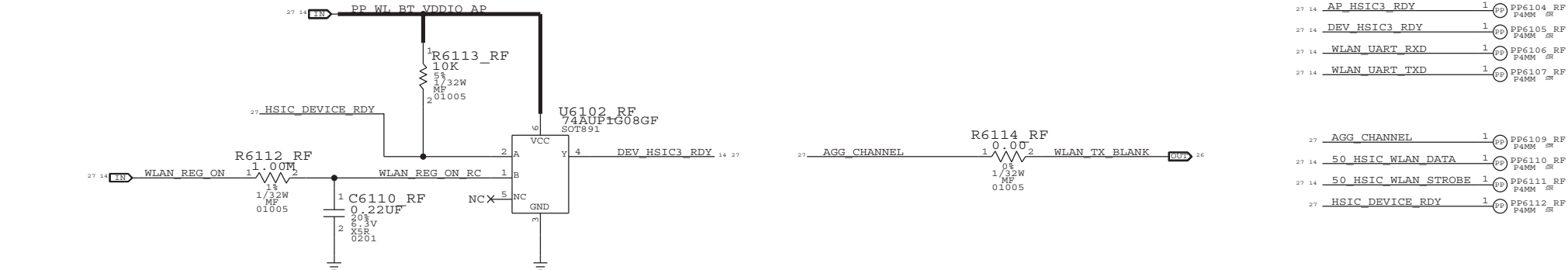
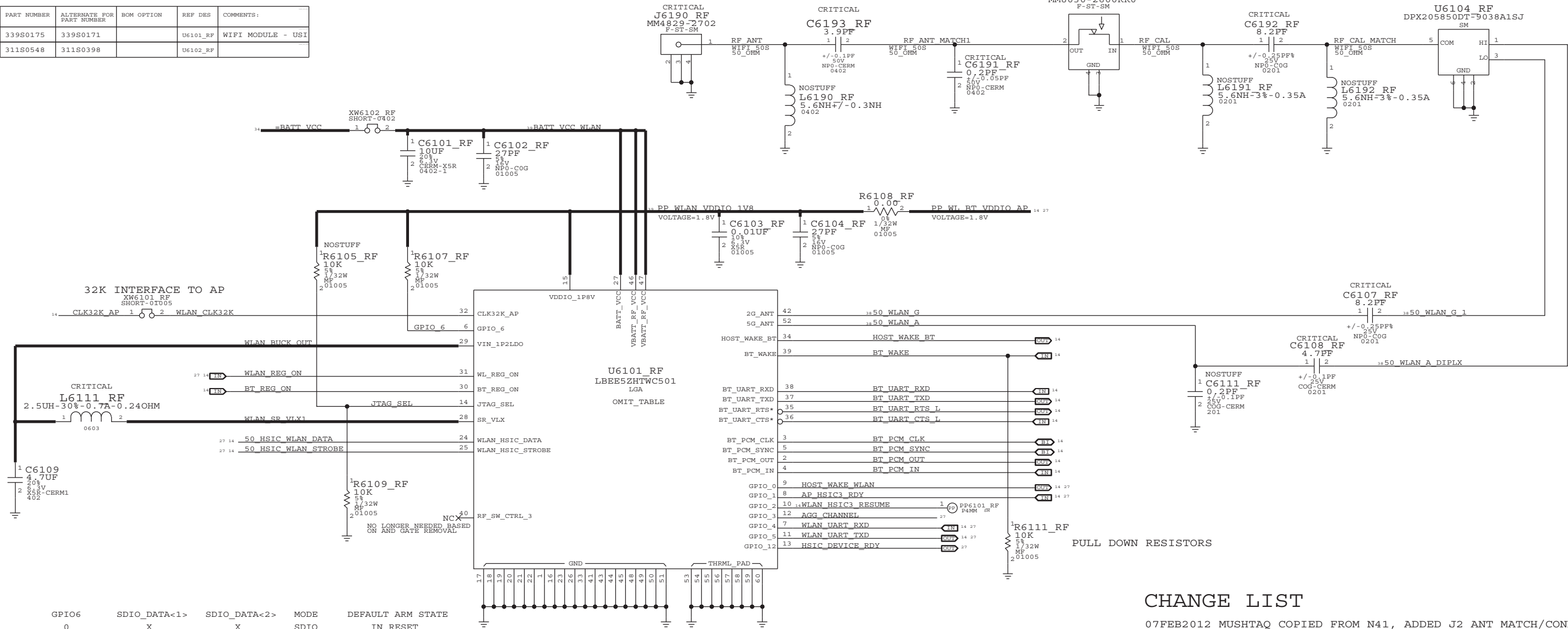
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0171	1	WIFI MODULE - MURATA	U6101_RF	CRITICAL	

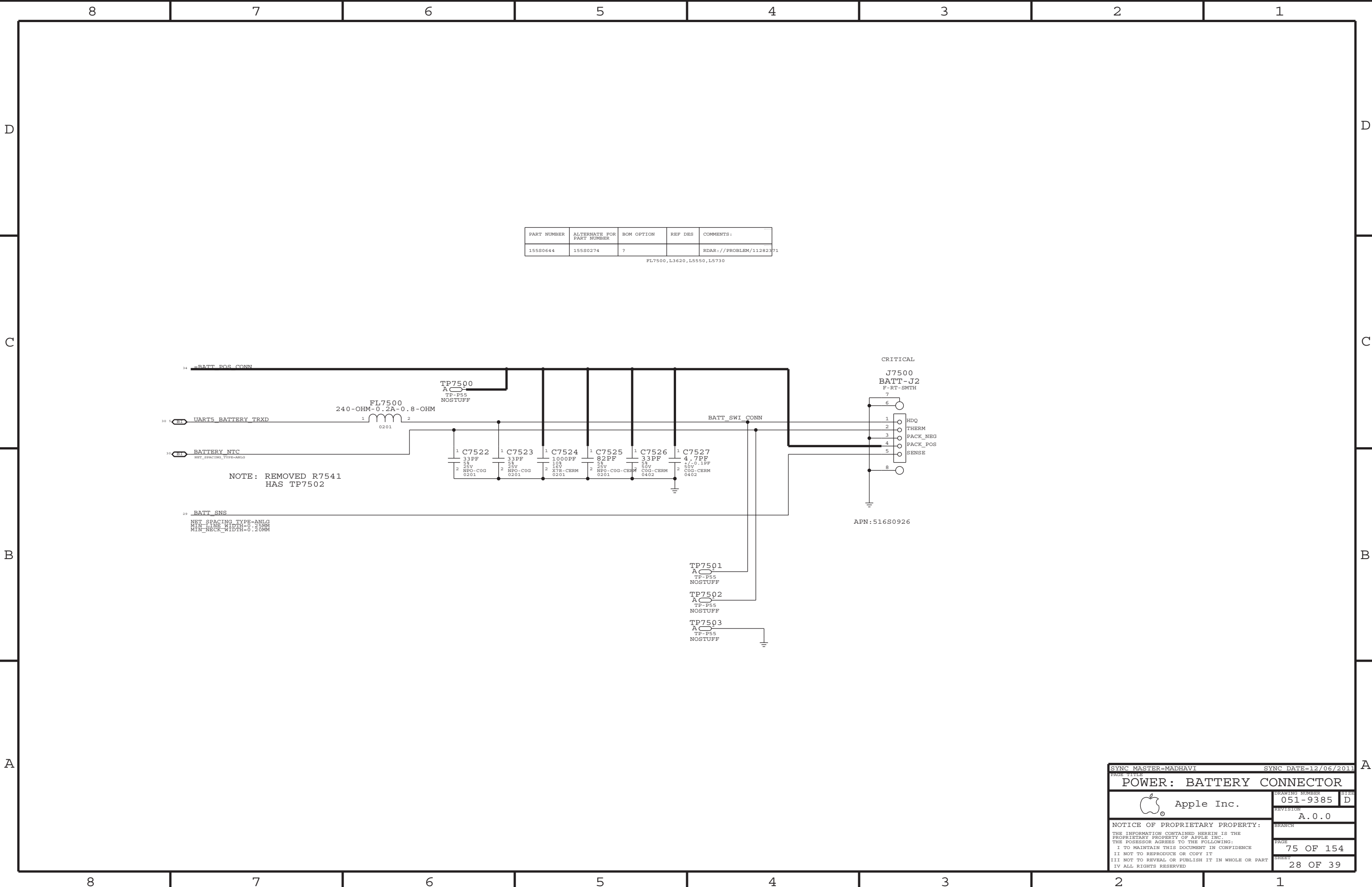
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0175	339S0171		U6101_RF	WIFI MODULE - USI
311S0548	311S0398		U6102_RF	

ANTENNA CONNECTOR

CONDUCTED TEST PORT



SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE		WIFI/BT	
Apple Inc.		DRAWING NUMBER	051-9385
		REVISION	A.0.0
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		PAGE	61 OF 154
		SHEET	27 OF 39
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0274	?		RDAR://PROBLEM/11282371

FL7500, L3620, L5550, L5730

SYNC MASTER=MADHAVI

SYNC DATE=12/06/2011

POWER: BATTERY CONNECTOR

 Apple Inc.

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75 OF 154

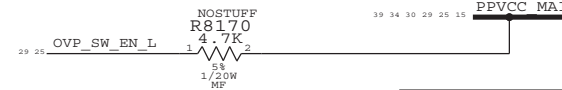
SHEET
28 OF 39

SIZE
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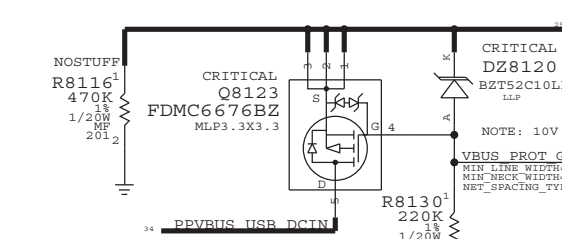
VCC MAIN BYPASS
TOTAL CAPS = ~400UF
PLACE ONE 10UF CAP
AT EACH VDD INPUT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1637	6	IND, 1.0UH, 20%, 59MO, 2.74A	L8100, L8101, L8102, L8103, L8109, L8110	CRITICAL	
152S1638	1	IND, 1.0UH, 20%, 64MO, 2.3A	L8104	CRITICAL	

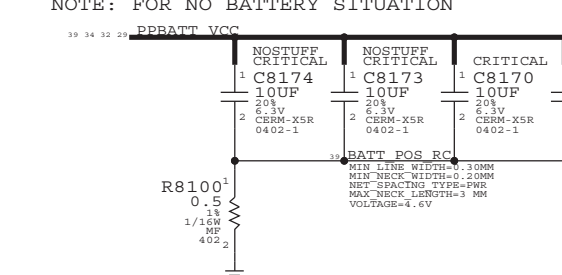
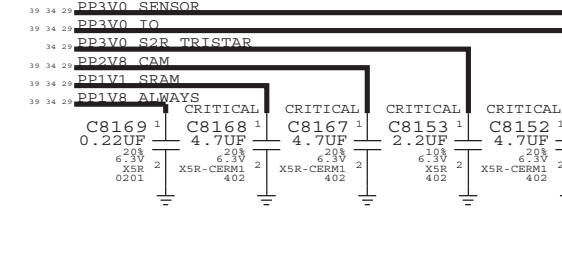
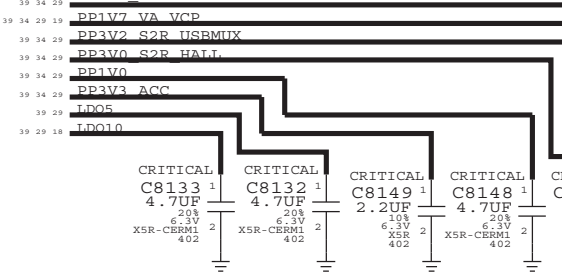
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1452	152S1292	?	L8111	RDAR://PROBLEM/8376462
138S0676	138S0654	?	?	?



MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	2.7 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



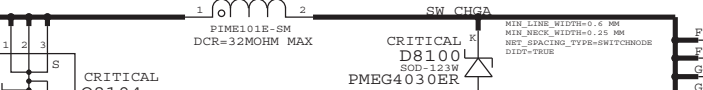
USB REVERSE VOLTAGE PROTECTION
LDO BYPASS



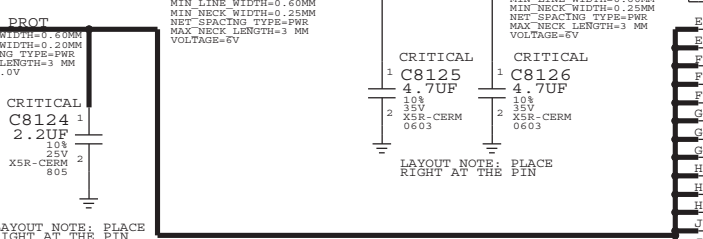
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CRITICAL C8165 150UF
CRITICAL C8154 10UF
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CRITICAL C8162 10UF
CRITICAL C8187 10UF
CRITICAL C8188 10UF
CRITICAL C8193 10UF
CRITICAL C8194 10UF
CRITICAL C8130 10UF
CRITICAL C8131 10UF
CRITICAL C8163 82PF
CRITICAL C8164 8.2PF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1637	6	IND, 1.0UH, 20%, 59MO, 2.74A	L8100, L8101, L8102, L8103, L8109, L8110	CRITICAL	
152S1638	1	IND, 1.0UH, 20%, 64MO, 2.3A	L8104	CRITICAL	

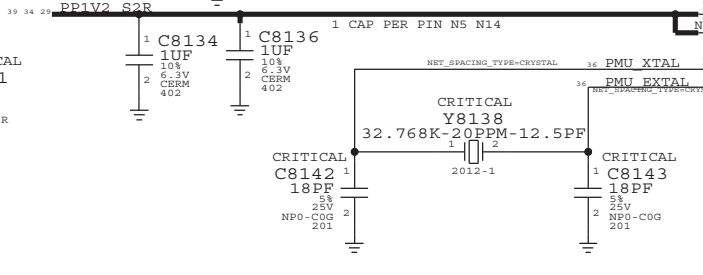
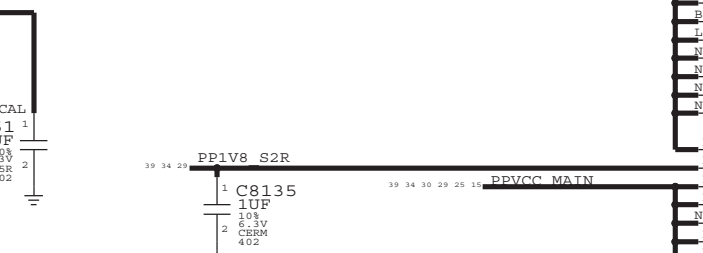
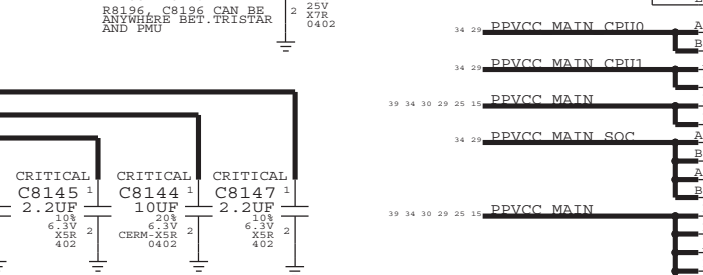
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1452	152S1292	?	L8111	RDAR://PROBLEM/8376462
138S0676	138S0654	?	?	?



MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	2.7 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



USB REVERSE VOLTAGE PROTECTION
LDO BYPASS



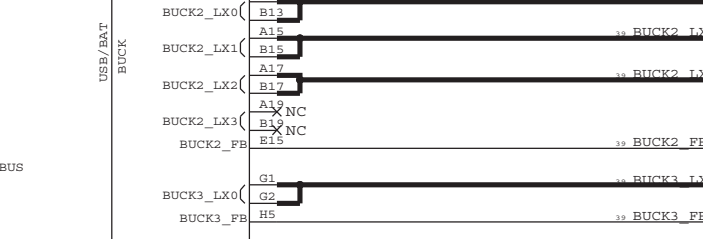
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CRITICAL C8162 10UF
CRITICAL C8187 10UF
CRITICAL C8188 10UF
CRITICAL C8193 10UF
CRITICAL C8194 10UF
CRITICAL C8130 10UF
CRITICAL C8131 10UF
CRITICAL C8163 82PF
CRITICAL C8164 8.2PF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1637	6	IND, 1.0UH, 20%, 59MO, 2.74A	L8100, L8101, L8102, L8103, L8109, L8110	CRITICAL	
152S1638	1	IND, 1.0UH, 20%, 64MO, 2.3A	L8104	CRITICAL	

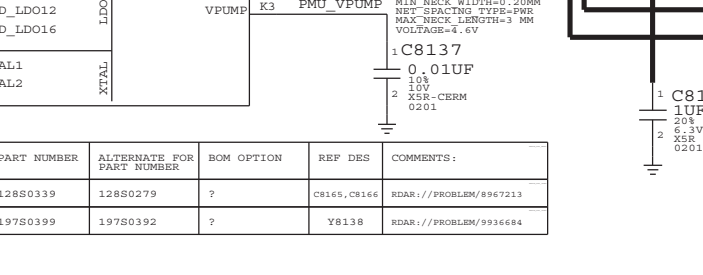
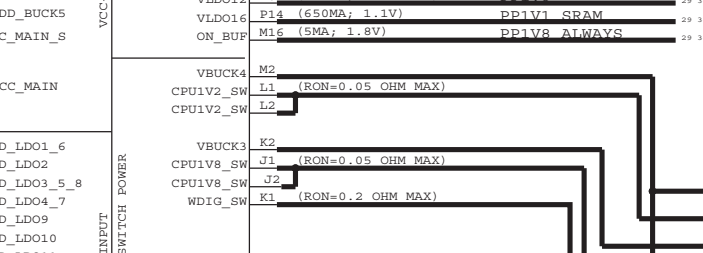
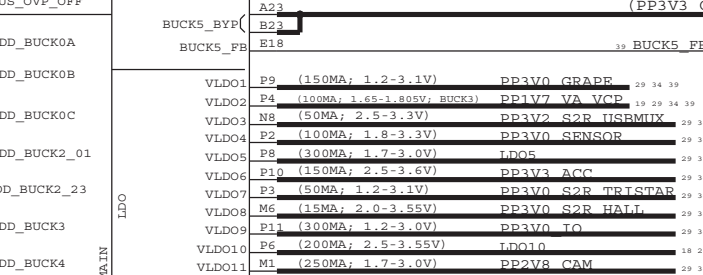
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1452	152S1292	?	L8111	RDAR://PROBLEM/8376462
138S0676	138S0654	?	?	?



MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	2.7 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



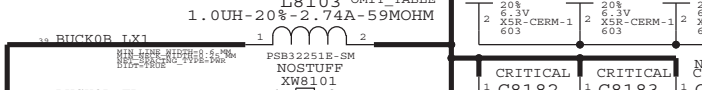
USB REVERSE VOLTAGE PROTECTION
LDO BYPASS



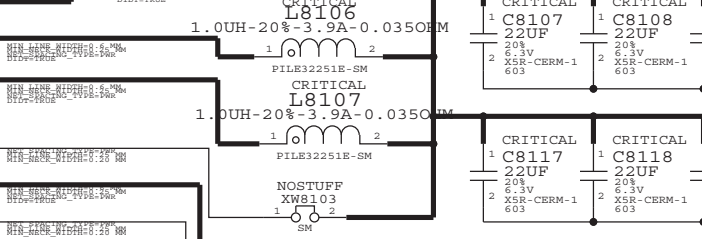
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CRITICAL C8162 10UF
CRITICAL C8187 10UF
CRITICAL C8188 10UF
CRITICAL C8193 10UF
CRITICAL C8194 10UF
CRITICAL C8130 10UF
CRITICAL C8131 10UF
CRITICAL C8163 82PF
CRITICAL C8164 8.2PF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1637	6	IND, 1.0UH, 20%, 59MO, 2.74A	L8100, L8101, L8102, L8103, L8109, L8110	CRITICAL	
152S1638	1	IND, 1.0UH, 20%, 64MO, 2.3A	L8104	CRITICAL	

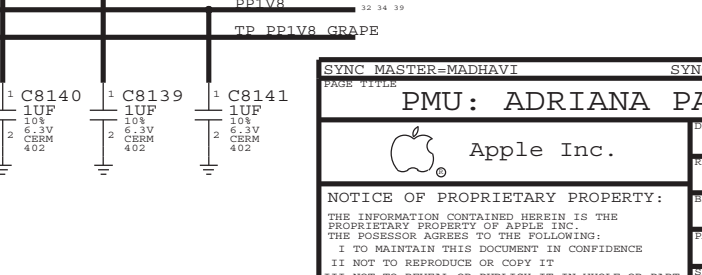
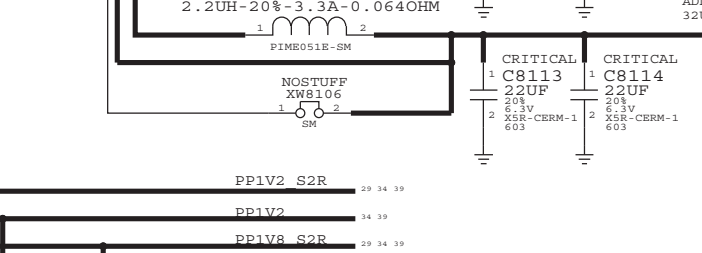
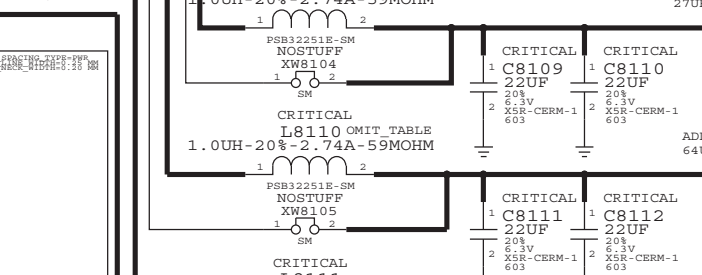
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1452	152S1292	?	L8111	RDAR://PROBLEM/8376462
138S0676	138S0654	?	?	?



MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	2.7 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



USB REVERSE VOLTAGE PROTECTION
LDO BYPASS



VCC MAIN BYPASS
TOTAL CAPS = ~400UF
PLACE ONE 10UF CAP
AT EACH VDD INPUT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1637	6	IND, 1.0UH, 20%, 59MO, 2.74A	L8100, L8101, L8102, L8103, L8109, L8110	CRITICAL	
152S1638	1	IND, 1.0UH, 20%, 64MO, 2.3A	L8104	CRITICAL	

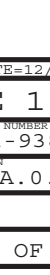
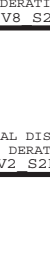
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1452	152S1292	?	L8111	RDAR://PROBLEM/8376462
138S0676	138S0654	?	?	?

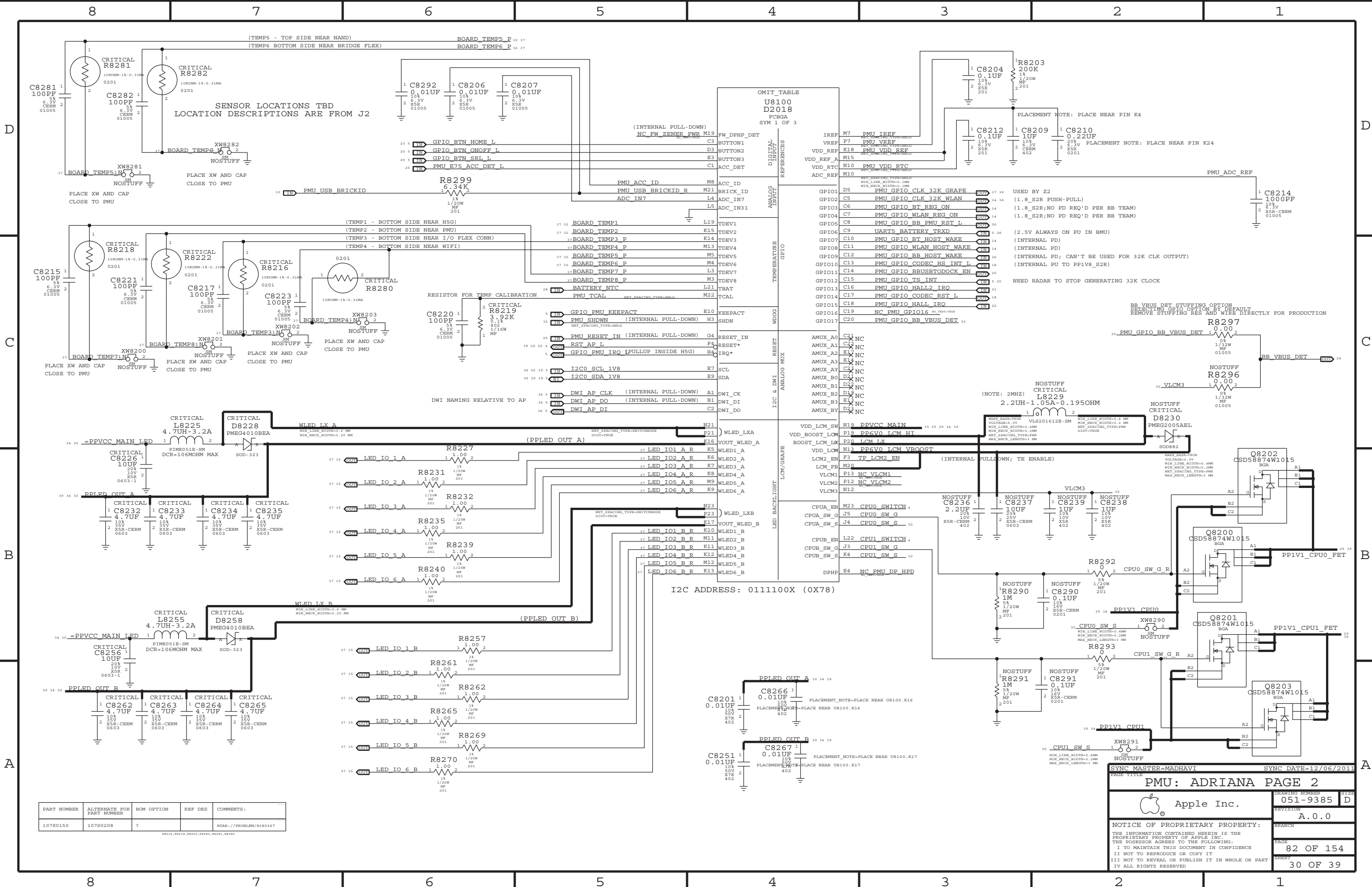


MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	2.7 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



USB REVERSE VOLTAGE PROTECTION
LDO BYPASS





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	?		RDAR://PROBLEM/8380367

SYNC MASTER=MADHAVI

SYNC DATE=12/06/2011

PMU: ADRIANA PAGE 2

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051-9385

REVISION

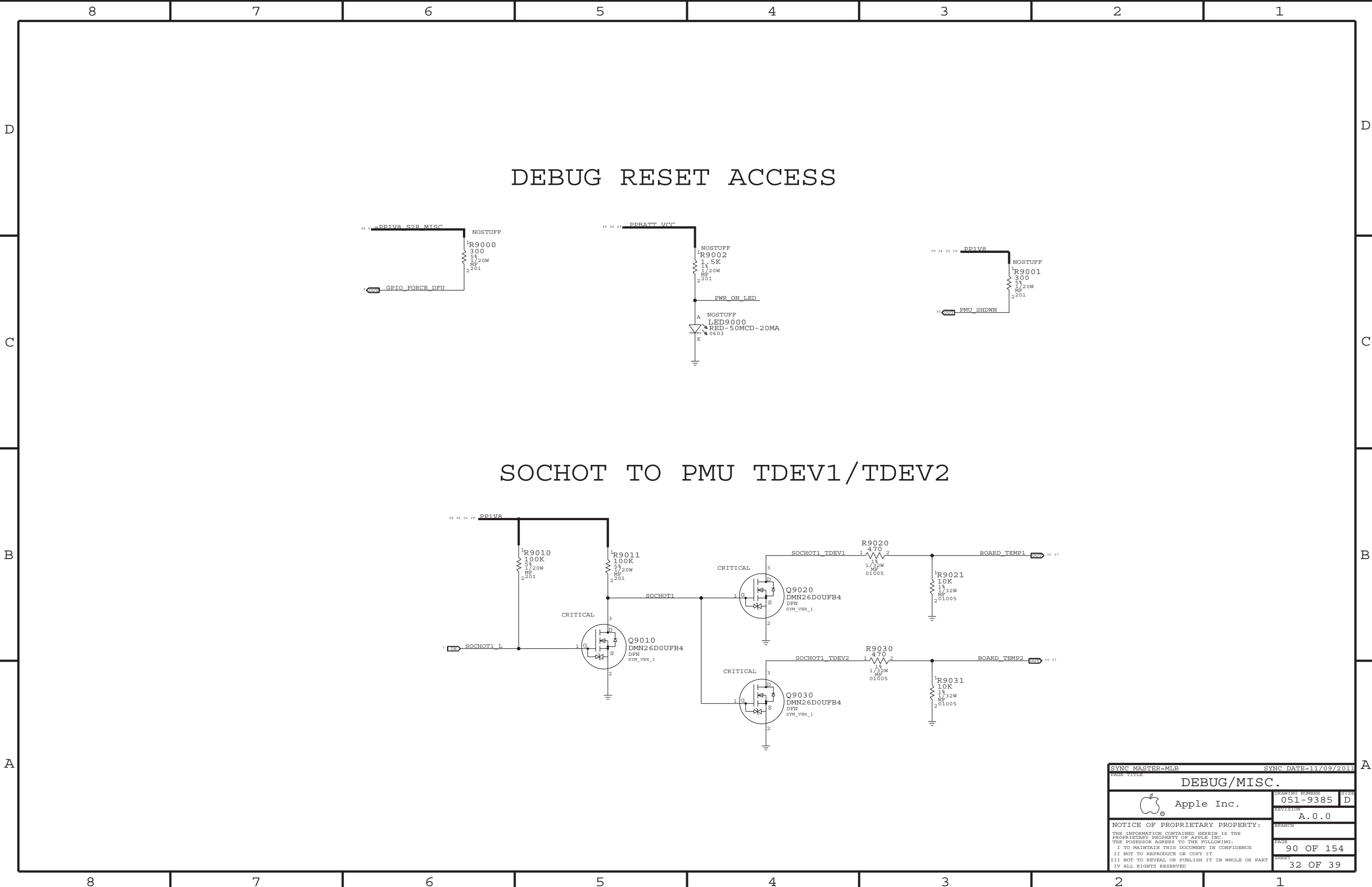
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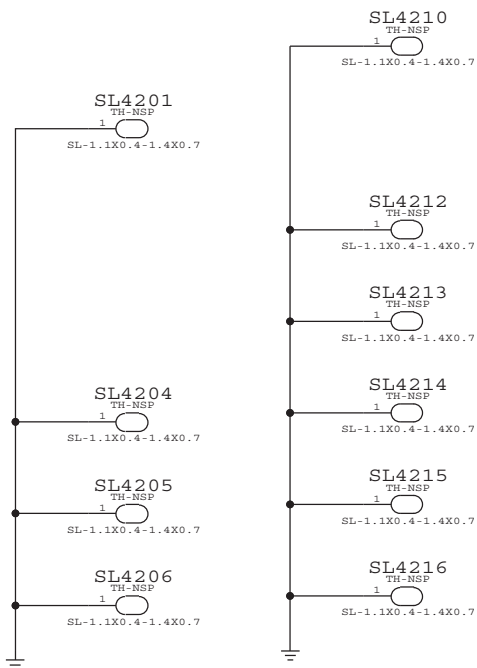
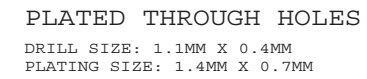
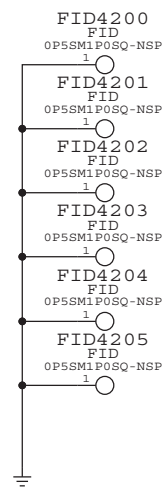
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SHEET

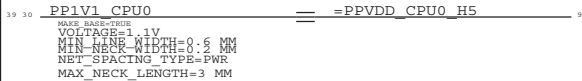
30 OF 39



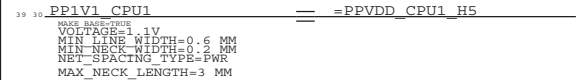


POWER CONNECTIONS

BUCK0A



BUCK0B



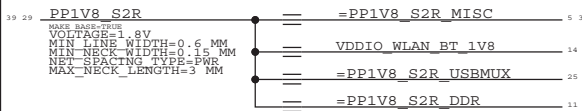
BUCK0C



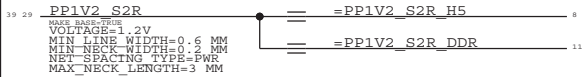
BUCK2



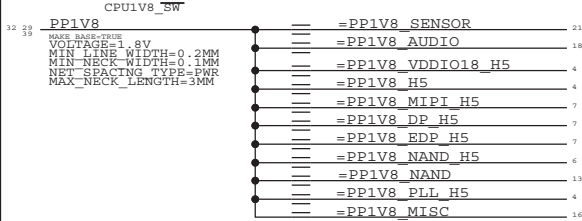
BUCK3



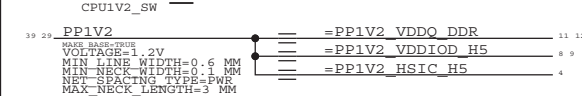
BUCK4



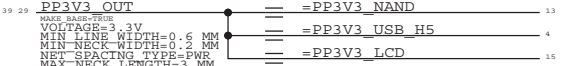
BUCK3_SW



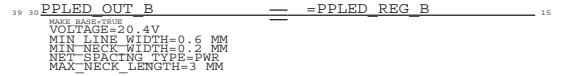
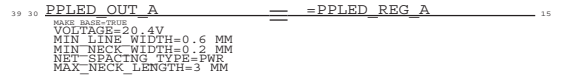
BUCK4_SW



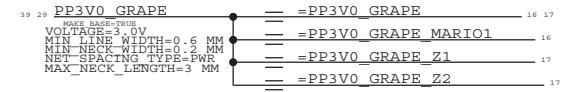
BUCK5



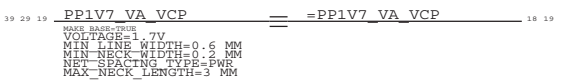
BACKLIGHT BOOST



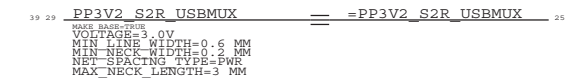
LDO1



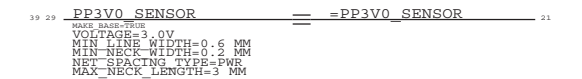
LDO2



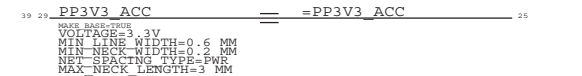
LDO3 (NO LONGER NEEDED)



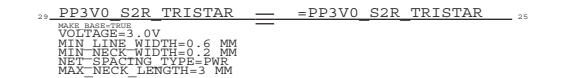
LDO4



LDO6



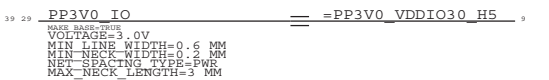
LDO7



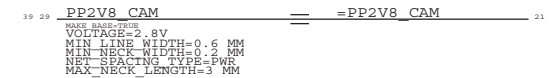
LDO8



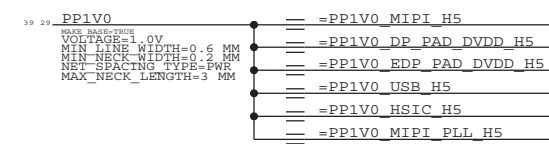
LDO9



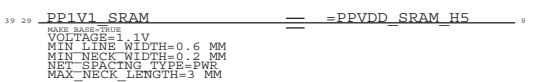
LDO11



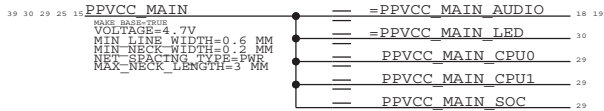
LDO12



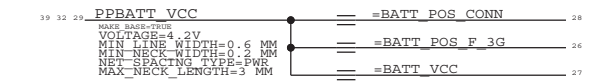
LDO16



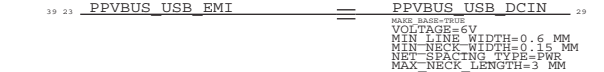
CHARGER MAIN



BATTERY



USB POWER INPUT



PAGE TITLE		SYNC DATE=N/A	
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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM	NO_TYPE, BGA, BGA06-06, BGA_P4	MM	16.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	3.0 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.105 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL2, ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL3, ISL8	Y	0.065 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4, ISL7	Y	0.053 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL5	Y	0.072 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL6	Y	0.059 MM	0.055 MM	3.0 MM		

90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
90_OHM_DIFF	ISL2, ISL9	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL3, ISL8	Y	0.062 MM	0.052 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL4, ISL7	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL5, ISL6	Y	0.052 MM	0.052 MM	=STANDARD	0.105 MM	0.105 MM

DDR 45 OHMS SINGLE-ENDED PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_45_OHM_SE	TOP, BOTTOM	Y	0.105 MM	0.105 MM	3.0 MM		
DDR_45_OHM_SE	ISL2	Y	0.055 MM	0.055 MM	3.0 MM		
DDR_45_OHM_SE	ISL3	Y	0.065 MM	0.065 MM	3.0 MM		
DDR_45_OHM_SE	ISL4	Y	0.053 MM	0.053 MM	3.0 MM		
DDR_45_OHM_SE	ISL5, ISL6	Y	0.072 MM	0.072 MM	3.0 MM		
DDR_45_OHM_SE	*	N	0.055 MM	0.055 MM	3.0 MM		

DDR 90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_90_OHM_DIFF	TOP, BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
DDR_90_OHM_DIFF	ISL2	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL3	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL4	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL5, ISL6	Y	0.066 MM	0.066 MM	=STANDARD	0.180 MM	0.180 MM
DDR_90_OHM_DIFF	*	N	0.056 MM	0.056 MM	=STANDARD	0.180 MM	0.180 MM

WIFI PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WIFI_50S	TOP, BOTTOM	Y	0.245 MM	0.2 MM	=STANDARD		
WIFI_50S	*	N	=STANDARD	=STANDARD	=STANDARD		
WIFI_PWR100	*	Y	0.10 MM	0.050 MM	=STANDARD		
WIFI_PWR1000	*	Y	1.00 MM	0.100 MM	=STANDARD		

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.5 MM	0.20 MM	10 MM	0.10 MM	0.10 MM
AUDIO_DIFF	*	Y	0.1 MM	0.09 MM	10 MM	0.10 MM	0.10 MM
LED	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM
TEMP_SENSE	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

TCF VERSION (USING SPACING RULE)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TCF_VERSION	*	0.104 MM	?

0.104 - 11/30/2011

TCF_VERSION NC_UART5_TXD *ASSIGNING RULE TO NC NET

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?
BGA_P4_SPA	*	0.200 MM	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.050 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.075 MM	?
2:1_SPACING	*	0.100 MM	?
2.5:1_SPACING	*	0.125 MM	?
3:1_SPACING	*	0.150 MM	?
4:1_SPACING	*	0.200 MM	?
5:1_SPACING	*	0.250 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?
0P2_SPACING	*	0.20 MM	?

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	
GND_P1SPACING	*	0.1 MM	
SWITCHNODE	*	0.2 MM	

POWER

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.20 MM	3.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	3.0 MM		
PWR_PMU	*	Y	0.6MM	0.20 MM	3.0 MM		

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
*	*	BGA_P4	BGA_P4_SPA

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

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		PAGE	150 OF 154
		SHEET	35 OF 39

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	3:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
PMU	CLK_50S	CLK	PMU_GPIO_CLK_32K_GRAPE 17 30
PMU	CLK_50S	CLK	PMU_GPIO_CLK_32K_WLAN 14 30
ISP1	CLK_50S	CLK	ISP1_CAM_FF_CLK 7 22
CONN	CLK_50S	CLK	CONN_ISP1_CAM_FF_CLK 20 22
ISP0	CLK_50S	CLK	ISP0_CAM_RF_CLK 7 22
CONN	CLK_50S	CLK	CONN_ISP0_CAM_RF_CLK 20 22
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_MCK 5 36
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R 5 18 36
ISP0	CLK_50S	CLK	ISP0_CAM_RF_CLK_R 7
ISP1	CLK_50S	CLK	ISP1_CAM_FF_CLK_R 7
ISP1	CLK_50S	CLK	ISP1_CAM_FF_C 22
ISP0	CLK_50S	CLK	ISP0_CAM_RF_C 22
ISP1	CLK_50S	CLK	ISP1_CAM_FF_FILT 22
ISP0	CLK_50S	CLK	ISP0_CAM_RF_FILT 22

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
UART2	UART_50S	UART	UART2_TS_ACC_RXD 5 25
UART2	UART_50S	UART	UART2_TS_ACC_TXD 5 25
UART4	UART_50S	UART	UART4_WLAN_RXD 5 14
UART4	UART_50S	UART	UART4_WLAN_TXD 5 14
UART1	UART_50S	UART	UART1_BB_CTS_L 5 26
UART1	UART_50S	UART	UART1_BB_RTS_L 5 26
UART1	UART_50S	UART	UART1_BB_TXD 5 25 26
UART1	UART_50S	UART	UART1_BB_RXD 5 25 26
UART3	UART_50S	UART	UART3_BT_CTS_L 5 14
UART3	UART_50S	UART	UART3_BT_RTS_L 5 14
UART3	UART_50S	UART	UART3_BT_RXD 5 14
UART3	UART_50S	UART	UART3_BT_TXD 5 14
UART6	UART_50S	UART	UART6_AP_RXD 5 25
UART6	UART_50S	UART	UART6_AP_TXD 5 25

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
SPI3	SPT_50S	SPT	SPI3_GRAPE_MISO 5 16
SPI3	SPT_50S	SPT	SPI3_GRAPE_MOSI 5 16
SPI3	SPT_50S	SPT	SPI3_GRAPE_SCLK 5 16
SPI3	SPT_50S	SPT	SPI3_GRAPE_CS_L 5 16
SPI2	SPT_50S	SPT	SPI2_IPC_MISO
SPI2	SPT_50S	SPT	SPI2_IPC_MOSI
SPI2	SPT_50S	SPT	SPI2_IPC_SCLK
SPI2	SPT_50S	SPT	GPIO_BB_HSIC_RESUME 5 26
SPI1	SPT_50S	SPT	SPI1_CODEC_MISO 5 18
SPI1	SPT_50S	SPT	SPI1_CODEC_MOSI 5 18
SPI1	SPT_50S	SPT	SPI1_CODEC_SCLK 5 18
SPI1	SPT_50S	SPT	SPI1_CODEC_CS_L 5 18

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DWI		DWI	DWI_AP_CLK 5 30
DWI		DWI	DWI_AP_DI 5 30
DWI		DWI	DWI_AP_DO 5 30

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
JTAG		JTAG	JTAG_AP_TCK 4 25
JTAG		JTAG	JTAG_AP_TMS 4 25
JTAG		JTAG	JTAG_AP_TDI 4
JTAG		JTAG	TR_JTAG_AP_TDO 4
JTAG		EST	JTAG_AP_TRST_L 4 10 39

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I2C1	I2C_50S	I2C	I2C1_SDA_1V8 5 22
I2C1	I2C_50S	I2C	I2C1_SCL_1V8 5 22
I2C0	I2C_50S	I2C	I2C0_SDA_1V8 5 19 25 30
I2C0	I2C_50S	I2C	I2C0_SCL_1V8 5 19 25 30
I2C2	I2C_50S	I2C	I2C2_SDA_3V0 5 22
I2C2	I2C_50S	I2C	I2C2_SCL_3V0 5 22
ISP0	I2C_50S	I2C	ISP0_CAM_RF_I2C_SCL 7 22
ISP0	I2C_50S	I2C	ISP0_CAM_RF_I2C_SDA 7 22
ISP1	I2C_50S	I2C	ISP1_CAM_FF_I2C_SCL 7 22
ISP1	I2C_50S	I2C	ISP1_CAM_FF_I2C_SDA 7 22
CONN	I2C_50S	I2C	CONN_I2C1_SDA_1V8 20 22
CONN	I2C_50S	I2C	CONN_I2C1_SCL_1V8 20 22
CONN	I2C_50S	I2C	CONN_I2C2_SCL_3V0 20 22
CONN	I2C_50S	I2C	CONN_I2C2_SDA_3V0 20 22
CONN	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SCL 20 22
CONN	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SDA 20 22
CONN	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SCL 20 22
CONN	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SDA 20 22

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
XTAL		CRYSTAL	XTAL_AP_24M_I 4
XTAL		CRYSTAL	XTAL_AP_24M_O 4
XTAL		CRYSTAL	AP_24M_O 4
PMU		CRYSTAL	PMU_XTAL 29
PMU		CRYSTAL	PMU_EXTAL 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_BCLK 5 18
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_LRCK 5 18
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_DIN 5 18
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_DOUT 5 18
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_SDOUT 18
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_MCK 5 36
I2S0	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R 5 18 36
I2S3	I2S_50S	I2S	I2S3_CODEC_XSP_BCLK 5 18
I2S3	I2S_50S	I2S	I2S3_CODEC_XSP_LRCK 5 18
I2S3	I2S_50S	I2S	I2S3_CODEC_XSP_DIN 5 18
I2S3	I2S_50S	I2S	I2S3_CODEC_XSP_DOUT 5 18
I2S0	I2S_50S	I2S	I2S0_CODEC_XSP_SDOUT 5 18
I2S2	I2S_50S	I2S	I2S2_BT_BCLK 5 14
I2S2	I2S_50S	I2S	I2S2_BT_LRCK 5 14
I2S2	I2S_50S	I2S	I2S2_BT_DIN 5 14
I2S2	I2S_50S	I2S	I2S2_BT_DOUT 5 14

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	4:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
USB	USB_90D	USB	USB_AP_P 4 25
USB	USB_90D	USB	USB_AP_N 4 25
USB	USB_90D	USB	USB_BBMUX_BB_P 25 26
USB	USB_90D	USB	USB_BBMUX_BB_N 25 26
USB	USB_90D	USB	USB_TS_BBMUX_P 25
USB	USB_90D	USB	USB_TS_BBMUX_N 25
USB	USB_90D	USB	USB11_AP_BBMUX_P 4 25
USB	USB_90D	USB	USB11_AP_BBMUX_N 4 25
CONN	USB_90D	USB	CONN_E75_DPAIR1_P 24 25
CONN	USB_90D	USB	CONN_E75_DPAIR1_N 24 25
CONN	USB_90D	USB	CONN_E75_DPAIR2_P 24 25
CONN	USB_90D	USB	CONN_E75_DPAIR2_N 24 25
TS	USB_90D	USB	TS_E75_DPAIR1_P 25
TS	USB_90D	USB	TS_E75_DPAIR1_N 25
TS	USB_90D	USB	TS_E75_DPAIR2_P 25
TS	USB_90D	USB	TS_E75_DPAIR2_N 25

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	4:1_SPACING
HSIC_RDY	*	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
HSIC3	HSIC	HSIC	HSIC3_BB_DATA 4 26
HSIC3	HSIC	HSIC	HSIC3_BB_STB 4 26
HSIC1	HSIC	HSIC	HSIC1_WLAN_DATA 4 14
HSIC1	HSIC	HSIC	HSIC1_WLAN_STB 4 14
GPIO	HSIC	HSIC_RDY	GPIO_BB_HSIC_DEV_RDY 5 26
GPIO	HSIC	HSIC_RDY	GPIO_BB_HSIC_HOST_RDY 5 26
GPIO	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY 5 14 36
GPIO	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY 5 14 36
GPIO	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_DEV_RDY 5 14

SYNC MASTER=MIKE

SYNC DATE=11/30/2011

PAGE TITLE

CONSTRAINTS: LOW SPEED BUS

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MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPIOC	*	*	4:1_SPACING
MIPI1C	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_CLK_P 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_CLK_N 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_P<0> 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_N<0> 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_P<1> 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_N<1> 7 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_CLK_F_P 20 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_CLK_F_N 20 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_F_P<0> 20 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_F_P<1> 20 21
RE30	MIPI_90D	MIPIOC	MIPIOC_CAM_RF_DATA_F_N<1> 20 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_P 7 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_N 7 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_P<0> 7 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_N<0> 7 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_P 20 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_N 20 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_P<0> 20 21
RE30	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_N<0> 20 21

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
RE30	AUDIO_DIFF	AUDIO	HP_MIC_P 18
RE30	AUDIO_DIFF	AUDIO	HP_MIC_N 18
RE30	AUDIO_DIFF	AUDIO	L81_AIN2_P 18
RE30	AUDIO_DIFF	AUDIO	L81_AIN2_N 18
RE30	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N_FILT 19
RE30	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P_FILT 19
RE30	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N 19
RE30	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N_FILT 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P_FILT 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P 19
RE30	SPEAKER	AUDIO	SPKR_L_P 19
RE30	SPEAKER	AUDIO	SPKR_L_N 19
RE30	SPEAKER	AUDIO	SPKR_L_CONN_P 19
RE30	SPEAKER	AUDIO	SPKR_L_CONN_N 19
RE30	SPEAKER	AUDIO	SPKR_R_P 19
RE30	SPEAKER	AUDIO	SPKR_R_N 19
RE30	SPEAKER	AUDIO	SPKR_R_CONN_P 19
RE30	SPEAKER	AUDIO	SPKR_R_CONN_N 19
RE30	SPEAKER	AUDIO	SPKR_L_FLR 19
RE30	SPEAKER	AUDIO	SPKR_R_FLR 19
RE30	AUDIO_DIFF	AUDIO	SPKR_L_SES_N 19
RE30	AUDIO_DIFF	AUDIO	SPKR_L_SES_P 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_SES_N 19
RE30	AUDIO_DIFF	AUDIO	SPKR_R_SES_P 19
RE30	USB_90D	USB	MIKEY_TS_P 18 25
RE30	USB_90D	USB	MIKEY_TS_N 18 25
RE30	USB_90D	USB	L81_MBUS_P 18
RE30	USB_90D	USB	L81_MBUS_N 18

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF	EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
RE30	EDP_90D	EDP	EDP_AUX_P 7 15
RE30	EDP_90D	EDP	EDP_AUX_N 7 15
RE30	EDP_50S	EDP	EDP_HPD 7 15
RE30	EDP_90D	EDP	EDP_DATA_P<0> 7 15
RE30	EDP_90D	EDP	EDP_DATA_N<0> 7 15
RE30	EDP_90D	EDP	EDP_DATA_P<1> 7 15
RE30	EDP_90D	EDP	EDP_DATA_N<1> 7 15
RE30	EDP_90D	EDP	EDP_DATA_P<2> 7 15
RE30	EDP_90D	EDP	EDP_DATA_N<2> 7 15
RE30	EDP_90D	EDP	EDP_DATA_P<3> 7 15
RE30	EDP_90D	EDP	EDP_DATA_N<3> 7 15
RE30	EDP_90D	EDP	EDP_AUX_EMI_P 15
RE30	EDP_90D	EDP	EDP_AUX_EMI_N 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_P<0> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_N<0> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_P<1> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_N<1> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_P<2> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_N<2> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_P<3> 15
RE30	EDP_90D	EDP	EDP_DATA_EMI_N<3> 15
RE30	EDP_90D	EDP	CONN_EDP_AUX_EMI_P 15
RE30	EDP_90D	EDP	CONN_EDP_AUX_EMI_N 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<0> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<0> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<1> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<1> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<2> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<2> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<3> 15
RE30	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<3> 15

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LEDA	*	*	3:1_SPACING
LEDB	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
RE30	LED	LEDA	LED_IO1_A_R 30
RE30	LED	LEDR	LED_IO1_B_R 30
RE30	LED	LEDA	LED_IO2_A_R 30
RE30	LED	LEDR	LED_IO2_B_R 30
RE30	LED	LEDA	LED_IO3_A_R 30
RE30	LED	LEDR	LED_IO3_B_R 30
RE30	LED	LEDA	LED_IO4_A_R 30
RE30	LED	LEDR	LED_IO4_B_R 30
RE30	LED	LEDA	LED_IO5_A_R 30
RE30	LED	LEDR	LED_IO5_B_R 30
RE30	LED	LEDA	LED_IO6_A_R 30
RE30	LED	LEDR	LED_IO6_B_R 30
RE30	LED	LEDA	LED_IO_1_A 15 30
RE30	LED	LEDR	LED_IO_1_B 15 30
RE30	LED	LEDA	LED_IO_2_A 15 30
RE30	LED	LEDR	LED_IO_2_B 15 30
RE30	LED	LEDA	LED_IO_3_A 15 30
RE30	LED	LEDR	LED_IO_3_B 15 30
RE30	LED	LEDA	LED_IO_4_A 15 30
RE30	LED	LEDR	LED_IO_4_B 15 30
RE30	LED	LEDA	LED_IO_5_A 15 30
RE30	LED	LEDR	LED_IO_5_B 15 30
RE30	LED	LEDA	LED_IO_6_A 15 30
RE30	LED	LEDR	LED_IO_6_B 15 30

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
BOARD_TEMP	*	TEMP_SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
RE30		BOARD_TEMP	BOARD_TEMP1 30 32
RE30		BOARD_TEMP	BOARD_TEMP2 30 32
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_N 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_N 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_N 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_N 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_N 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_P 30
RE30	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_N 30

SYNC MASTER=MIKE		SYNC DATE=11/30/2011	
PAGE TITLE		CONSTRAINTS: DISPLAY/AUDIO	
 Apple Inc.		DRAWING NUMBER	051-9385
		REVISION	A.0.0
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DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DDR_45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DDR_90_OHM_DIFF

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND0	*	*	2:1_SPACING
NAND1	*	*	2:1_SPACING

WIFI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
WIFI_50S	*	WIFI_50S
WIFI_PWR100	*	WIFI_PWR100
WIFI_PWR1000	*	WIFI_PWR1000

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
DDR0	DDR_50S	DDR	DDR0_CA<9..0>
DDR0	DDR_50S	DDR	DDR0_DM<3..0>
DDR0	DDR_90D	DDR	DDR0_CK_P
DDR0	DDR_90D	DDR	DDR0_CK_N
DDR0	DDR_50S	DDR	DDR0_CKE<1..0>
DDR0	DDR_50S	DDR	DDR0_CSN<2..0>
DDR0	DDR_50S	DDR	DDR0_ZQ
DDR0	DDR_50S	DDR	DDR0_DQ<7..0>
DDR0	DDR_90D	DDR	DDR0_DQS_P<0>
DDR0	DDR_90D	DDR	DDR0_DQS_N<0>
DDR0	DDR_50S	DDR	DDR0_DQ<15..8>
DDR0	DDR_90D	DDR	DDR0_DQS_P<1>
DDR0	DDR_90D	DDR	DDR0_DQS_N<1>
DDR0	DDR_50S	DDR	DDR0_DQ<23..16>
DDR0	DDR_90D	DDR	DDR0_DQS_P<2>
DDR0	DDR_90D	DDR	DDR0_DQS_N<2>
DDR0	DDR_50S	DDR	DDR0_DQ<31..24>
DDR0	DDR_90D	DDR	DDR0_DQS_P<3>
DDR0	DDR_90D	DDR	DDR0_DQS_N<3>
DDR0	DDR_50S	DDR	DDR1_CA<9..0>
DDR0	DDR_50S	DDR	DDR1_DM<3..0>
DDR0	DDR_90D	DDR	DDR1_CK_P
DDR0	DDR_90D	DDR	DDR1_CK_N
DDR0	DDR_50S	DDR	DDR1_CKE<1..0>
DDR0	DDR_50S	DDR	DDR1_CSN<2..0>
DDR0	DDR_50S	DDR	DDR1_ZQ
DDR0	DDR_50S	DDR	DDR1_DQ<7..0>
DDR0	DDR_90D	DDR	DDR1_DQS_P<0>
DDR0	DDR_90D	DDR	DDR1_DQS_N<0>
DDR0	DDR_50S	DDR	DDR1_DQ<15..8>
DDR0	DDR_90D	DDR	DDR1_DQS_P<1>
DDR0	DDR_90D	DDR	DDR1_DQS_N<1>
DDR0	DDR_50S	DDR	DDR1_DQ<23..16>
DDR0	DDR_90D	DDR	DDR1_DQS_P<2>
DDR0	DDR_90D	DDR	DDR1_DQS_N<2>
DDR0	DDR_50S	DDR	DDR1_DQ<31..24>
DDR0	DDR_90D	DDR	DDR1_DQS_P<3>
DDR0	DDR_90D	DDR	DDR1_DQS_N<3>
DDR0	DDR_50S	DDR	DDR2_CA<9..0>
DDR0	DDR_50S	DDR	DDR2_DM<3..0>
DDR0	DDR_90D	DDR	DDR2_CK_P
DDR0	DDR_90D	DDR	DDR2_CK_N
DDR0	DDR_50S	DDR	DDR2_CKE<1..0>
DDR0	DDR_50S	DDR	DDR2_CSN<2..0>
DDR0	DDR_50S	DDR	DDR2_ZQ
DDR0	DDR_50S	DDR	DDR2_DQ<7..0>
DDR0	DDR_90D	DDR	DDR2_DQS_P<0>
DDR0	DDR_90D	DDR	DDR2_DQS_N<0>
DDR0	DDR_50S	DDR	DDR2_DQ<15..8>
DDR0	DDR_90D	DDR	DDR2_DQS_P<1>
DDR0	DDR_90D	DDR	DDR2_DQS_N<1>
DDR0	DDR_50S	DDR	DDR2_DQ<23..16>
DDR0	DDR_90D	DDR	DDR2_DQS_P<2>
DDR0	DDR_90D	DDR	DDR2_DQS_N<2>
DDR0	DDR_50S	DDR	DDR2_DQ<31..24>
DDR0	DDR_90D	DDR	DDR2_DQS_P<3>
DDR0	DDR_90D	DDR	DDR2_DQS_N<3>
DDR0	DDR_50S	DDR	DDR3_CA<9..0>
DDR0	DDR_50S	DDR	DDR3_DM<3..0>
DDR0	DDR_90D	DDR	DDR3_CK_P
DDR0	DDR_90D	DDR	DDR3_CK_N
DDR0	DDR_50S	DDR	DDR3_CKE<1..0>
DDR0	DDR_50S	DDR	DDR3_CSN<2..0>
DDR0	DDR_50S	DDR	DDR3_ZQ
DDR0	DDR_50S	DDR	DDR3_DQ<7..0>
DDR0	DDR_90D	DDR	DDR3_DQS_P<0>
DDR0	DDR_90D	DDR	DDR3_DQS_N<0>
DDR0	DDR_50S	DDR	DDR3_DQ<15..8>
DDR0	DDR_90D	DDR	DDR3_DQS_P<1>
DDR0	DDR_90D	DDR	DDR3_DQS_N<1>
DDR0	DDR_50S	DDR	DDR3_DQ<23..16>
DDR0	DDR_90D	DDR	DDR3_DQS_P<2>
DDR0	DDR_90D	DDR	DDR3_DQS_N<2>
DDR0	DDR_50S	DDR	DDR3_DQ<31..24>
DDR0	DDR_90D	DDR	DDR3_DQS_P<3>
DDR0	DDR_90D	DDR	DDR3_DQS_N<3>

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	PACING	
FEF0	NAND_50S	NAND0	FMIO_AD<0>
FEF0	NAND_50S	NAND0	FMIO_AD<1>
FEF0	NAND_50S	NAND0	FMIO_AD<2>
FEF0	NAND_50S	NAND0	FMIO_AD<3>
FEF0	NAND_50S	NAND0	FMIO_AD<4>
FEF0	NAND_50S	NAND0	FMIO_AD<5>
FEF0	NAND_50S	NAND0	FMIO_AD<6>
FEF0	NAND_50S	NAND0	FMIO_AD<7>
FEF0	NAND_50S	NAND0	FMIO_ALE
FEF0	NAND_50S	NAND0	FMIO_CEO_L
FEF0	NAND_50S	NAND0	TP FMIO_CE1_L
FEF0	NAND_50S	NAND0	TP FMIO_CE2_L
FEF0	NAND_50S	NAND0	TP FMIO_CE3_L
FEF0	NAND_50S	NAND0	TP FMIO_CE4_L
FEF0	NAND_50S	NAND0	TP FMIO_CE5_L
FEF0	NAND_50S	NAND0	TP FMIO_CE6_L
FEF0	NAND_50S	NAND0	TP FMIO_CE7_L
FEF0	NAND_50S	NAND0	FMIO_CLE
FEF0	NAND_50S	NAND0	FMIO_DQS
FEF0	NAND_50S	NAND0	FMIO_RE_L
FEF0	NAND_50S	NAND0	FMIO_WE_L
FEF0	NAND_50S	NAND1	FM11_AD<0>
FEF0	NAND_50S	NAND1	FM11_AD<1>
FEF0	NAND_50S	NAND1	FM11_AD<2>
FEF0	NAND_50S	NAND1	FM11_AD<3>
FEF0	NAND_50S	NAND1	FM11_AD<4>
FEF0	NAND_50S	NAND1	FM11_AD<5>
FEF0	NAND_50S	NAND1	FM11_AD<6>
FEF0	NAND_50S	NAND1	FM11_AD<7>
FEF0	NAND_50S	NAND1	FM11_ALE
FEF0	NAND_50S	NAND1	FM11_CEO_L
FEF0	NAND_50S	NAND1	TP FM11_CE2_L
FEF0	NAND_50S	NAND1	TP FM11_CE4_L
FEF0	NAND_50S	NAND1	TP FM11_CE5_L
FEF0	NAND_50S	NAND1	TP FM11_CE6_L
FEF0	NAND_50S	NAND1	TP FM11_CE7_L
FEF0	NAND_50S	NAND1	FM11_CLE
FEF0	NAND_50S	NAND1	FM11_DQS
FEF0	NAND_50S	NAND1	FM11_RE_L
FEF0	NAND_50S	NAND1	FM11_WE_L

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
WIFI	WIFI_50S	50 WLAN G
WIFI	WIFI_50S	50 WLAN A
WIFI	WIFI_50S	50 WLAN G 1
WIFI	WIFI_50S	50 WLAN A DIPLX
WIFI	WIFI_50S	50 WIFI ANT PD 2
WIFI	WIFI_50S	50 WIFI ANT PD 1
WIFI	WIFI_50S	50 WIFI ANT PD

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
SECD0			PWR	PPVREF_DDR0_CA	11 39
SECD0			PWR	PPVREF_DDR0_DQ	11 39
SECD0			PWR	PPVREF_DDR1_CA	11 39
SECD0			PWR	PPVREF_DDR1_DQ	11 39
SECD0			PWR	PPVREF_DDR2_CA	12 39
SECD0			PWR	PPVREF_DDR2_DQ	12 39
SECD0			PWR	PPVREF_DDR3_CA	12 39
SECD0			PWR	PPVREF_DDR3_DQ	12 39

SYNC MASTER=MIKE		SYNC DATE=11/30/2011	
PAGE TITLE			
CONSTRAINTS: DDR/FMI			
 Apple Inc.	DRAWING NUMBER		SIZE
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	REVISION		
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