1.HSIC1_WLAN2SOC_DEVICE_RDY
2.PMU_GPIO_BT_REG_ON_R
3.PMU_GPIO_WLAN_REG_ON_R
4.PMU_GPIO_BT_REG_ON
5.PMU_GPIO_WLAN_REG_ON
6.JTAG_WLAN_TMS_TX_BLANK
7.JTAG_WLAN_TDI_OSCAR_A
8.HSIC1_SOC2WLAN_HOST_RDY_R
9.JTAG_WLAN_SEL
10.TP_JTAG_WLAN_TCK
11.TP_JTAG_WLAN_TRST_L
12.JTAG_WLAN_TDO_OSCAR_B
13.OSCAR2RADIO_CONTEXT_A
14.PMU_GPIO_WLAN_HOST_WAKE
15.VCC_MAIN_GRAPE_RAMP
16.WLAN_TX_BLANK
17.PP3V3_S2R
18.GPIO_BT_WAKE
19.SIM_TRAY_DETECT
20.UART2_SOC2WLAN_TX_R
21.SIMCRD_CLK_CONN_FILT
22. UART2_WLAN2SOC_TX_R
23.UART_BB2WLAN_LTE_COEX_R
24.UART_WLAN2BB_LTE_COEX_R
25.BOARD_TEMP3_P
26.SIMCRD_CLK_CONN

1.PMU_GPIO_CLK_32K_WLAN_R
2.UART1_BT2SOC_RTS_L
3.UART1_BT2SOC_TX
4.UART1_SOC2BT_RTS_L
5&12&15&17&21&26&28.GND
6.GPIO_SOC2GRAPE_RESET_L

7.CUMULUS_M_VDDCORE
8.CUMULUS_M_VDDANA
9. CUMULUS_S_VDDCORE
10.TP_CUMULUS_S_H_SDO
11.TP_CUMULUS_S_H_SDI
13.CUMULUS_MS_CK
14.CUMULUS_S_BCFG_RTCK
16.JTAG_CUMULUS_S_TMS
18.CUMULUS_MS_SD
19.TP_CUMULUS_S_H_SCLK
20.CUMULUS_S_VDDANA
22.PP5V25_GRAPE
23.TP_CUMULUS_S_H_CS_L
24.GPIO_GRAPE2SOC_IRQ_L
25.PP1V8_GRAPE_SW
27.DISPLAY_SYNC
29.CUMULUS_M_BCFG_RTCK
30.SPI2_GRAPE_MOSI
31.TP_JTAG_CUMULUS_M_TDI
32.TP_JTAG_CUMULUS_M_TDO
33.SPI2_GRAPE_CS_L
34.TP_JTAG_CUMULUS_M_TCK
35.SPI2_GRAPE_SCLK
36.JTAG_CUMULUS_M_TMS

1&19&20&22&24&25&26&27&28&29&30&31&32&33.GND
2.PP1V8_SW1_FOREHEAD
3.PP_RF1_1V8_DIG
4.GPIO_SOC2BB_WAKE_MODEM
5.HSIC2_SOC2BB_HOST_RDY
6.PS_HOLD_PMIC
7.BB_JTAG_TMS
8.DEBUG_RST_L
9.USB_BB_DEBUG_N
10.USB_BB_DEBUG_P
11.BB_JTAG_TRST_L
12.BB_JTAG_TCK
13.BB_JTAG_TDI
14.BB_JTAG_TDO
15.BB_JTAG_RTCLK
16.PP_SMPS1_MSMC_1V05
17.PP_SMPS4_RF2_2V05
18.TP_BB_TEST_MODE_1
21.TP_BB_TEST_MODE_0
23.PP_SMPS2_RF1_1V3

1&2&4&5&6.GND
3.PP3V0_SENSOR_PROX_AD7149_FILT
7.PP2V9_AVDD_CAM_REAR_FILT
8.PP2V6_CAM_REAR_AF_FILT
9.CAM_REAR_VSYNC
10.PP1V8_CAM_REAR_FILT
11.ISP0_CAM_REAR_SHUTDOWN_L_F
12.ISP0_CAM_REAR_SDA_F
13.PP1V3_CAM_REAR_FILT
14.ISP0_CAM_REAR_CLK_F
15.ISP0_CAM_REAR_SCL_F
16.PP1V8_S2R_SW3_COMP

1.SIM_TRAY_DETECT_FILT
2.SIMCRD_RST_CONN_FILT
3.PP3V0_S2R_NAVAJO_FILT
4&5&6.PPVBUS_E75_USB_CONN
7.PMU_GPIO_MB_HALL1_IRQ
8.SIMCRD_IO_CONN_FILT
9.PP_LDO6_RUIM_1V8_FILT
10.PMU_GPIO_MB_HALL2_IRQ_FILT
11&12&13&14&60.GND
15.MAX983X4_L1_GAIN
16.PMU_GPIO_MB_HALL2_IRQ
17.SPKRAMP_L1_OUT_P
18.LEFT_CH_OUT_N
19.LEFT_CH_OUT_P
20.SPKRAMP_L1_OUT_N
21.MAX983X4_L2_GAIN
22.AUD_SPKRAMP_MUTE_L
23.RIGHT_CH_OUT_N
24.RIGHT_CH_OUT_P
25.PPOUT_E75_ACC_ID1_CONN
26.SPKRAMP_L2_OUT_N
27.SPKRAMP_L2_OUT_P
28.PPOUT_E75_ACC_ID2_CONN
29.E75_DPAIR2_CONN_N
30.E75_DPAIR2_CONN_P
31.SPKRAMP_R2_OUT_P
32.MAX983X4_R1_GAIN
33.SPKRAMP_R1_OUT_P
34.SPKRAMP_R1_OUT_N
35.MAX983X4_R2_GAIN
36.SPKRAMP_R2_OUT_N
37.E75_ACC_DET_CONN_L
38.E75_DPAIR1_CONN_N
39.E75_DPAIR1_CONN_P
40.LED_IO_1_B
41.LED_IO_2_B
42.LED_IO_4_B
43.LED_IO_3_B
44.LED_IO_6_A
45.LED_IO_5_B
46.LED_IO_6_B
47.LED_IO_5_A
48.LED_IO_4_A
49.LED_IO_3_A
50.PPVCC_MAIN_LCD_SW_CONN
51.PPVCC_MAIN_LCD_SW
52.CLK_32K_SOC2CUMULUS
53.LED_IO_2_A
54.LED_IO_1_A
56.PPLED_BACK_REG_A
57.PPLED_BACK_REG_B
58.PPLED_OUT_A
59.PP1V8_SW2
61.PP3V3_ACC
62.PMU_USB_BRICKID
63.RESET_SOC_L
64.UART0_SOC_RXD
65.USB_SOC_P
66.USB_SOC_N
67.JTAG_SOC_TCK
68.USB_BB_P
69.TS_E75_ACC_DET_L
70.JTAG_SOC_TMS
71.USB_BB_N
72.PMU_E75_ACC_DET_L

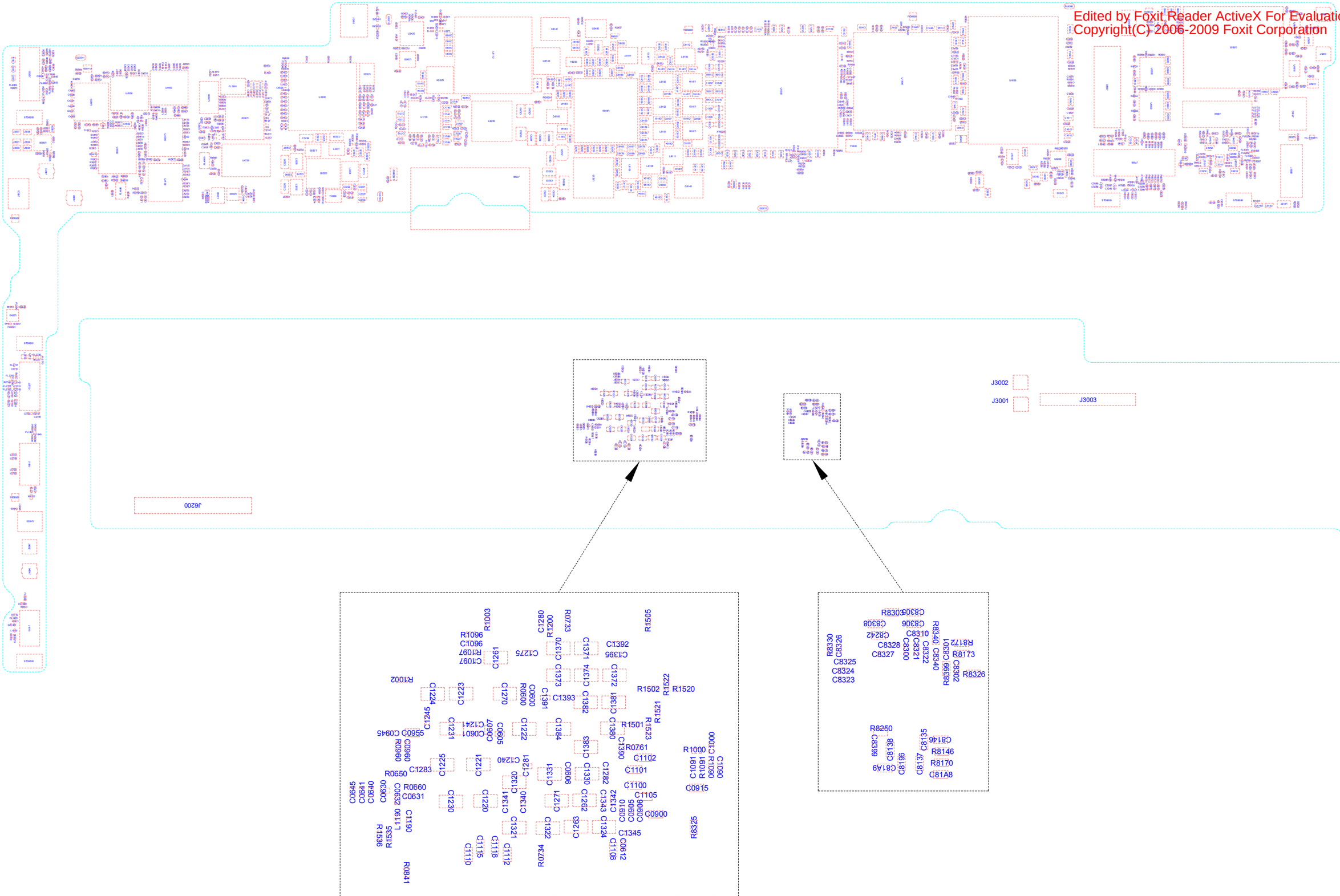
1.FMI0_CLE
2. BOARD_TEMP5_P
3.GPIO_BTN_HOME_L
4.PPVREF_FMI_NAND
5.PP1V8_EXT_SW
6.FMI0_RE_L
7.FMI0_CE0_L
8.FMI0_WE_L
9. FMI0_ALE
10.FMI0_AD<7>
11.FMI0_DQS
12.FMI0_AD<6>
13.FMI0_AD<5>
14.FMI0_AD<4>
15.FMI0_AD<0>
16.FMI1_AD<0>
17.FMI0_AD<1>
18.FMI0_AD<2>
19.FMI0_AD<3>
20.PP1V2_S2R
21.PP1V2_SW1
22.PP3V3_SW
23.I2C2_SDA_1V8
24.VCC_MAIN_PP3V3SW_RAMP
25.PP1V8_SW1
26.I2C2_SCL_1V8
27.JTAG_SOC_TDI
28.JTAG_SOC_SEL
29.UART6_TS_ACC_TXD

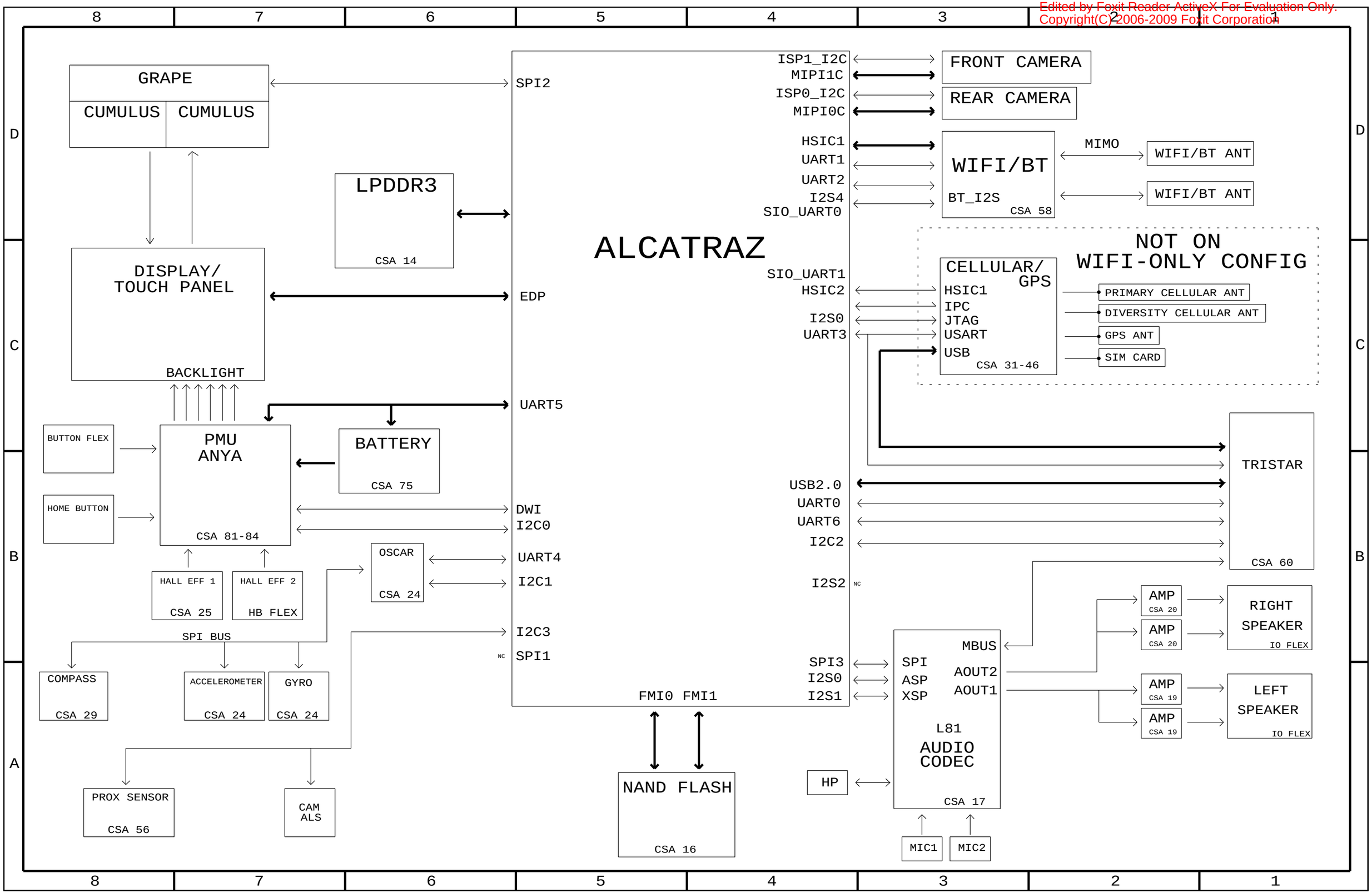
1.WDOG_SOC
2.SOC_TST_CLKOUT
3.PP1V2_SW1
4.JTAG_SOC_TRST_L
5.TP_JTAG_SOC_TDO
6.PPVREF_FMI_SOC
7&10&11&13&14.GND
8.HSIC1_WLAN2SOC_REMOTE_WAKE
9.UART6_TS_ACC_RXD
12.SOC_TESTMODE
15.UART1_SOC2BT_TX
16.TP_GPIO_DFU_STATUS
17.SPI2_GRAPE_MISO
18.SPI3_CODEC_CS_L
19.GPIO_SOC2PMU_KEEPACT
20.UART0_SOC_TXD
21.WDOG_SOC2PMU_RESET_IN
22.SOC_TST_CPUSWITCH_OUT
23.PMU_GPIO_BT_HOST_WAKE
24.SOCHOT0_L
25.OSCAR_TIME_SYNC_HOST_INT
26.BOARD_TEMP7_P

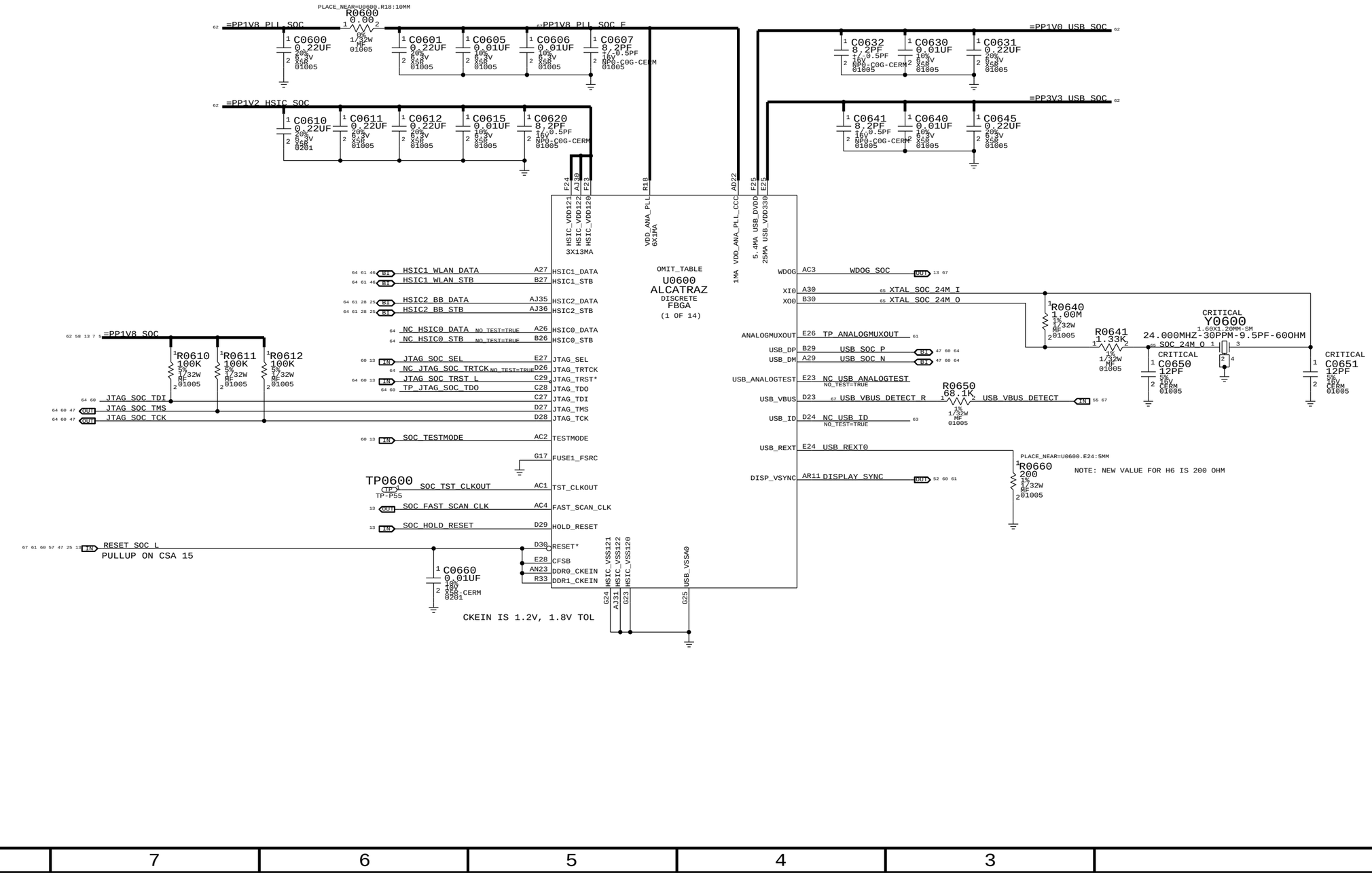
1.GPIO_TS2SOC2PMU_INT
2.SPI_OSCAR2COMPASS_CS_L
3.GPIO_FORCE_DFU
4.GPIO_SOC2BB_RST_L
5.PMU_GPIO_CLK_32K_OSCAR
6.GPIO_SOC2OSCAR_DBGEN
7.TP_OSCAR_P0_22
8.UART4_SOC2OSCAR_TXD
9.SPI_OSCAR_MISO
10.GPIO_SOC2OSCAR_DBGEN_R
11.PP3V0_S2R_SENSOR
12.PP1V2_S2R_SW2
13.GPIO_BB2SOC_GPS_SYNC
14.OSCAR2RADIO_CONTEXT_B
15.PP1V8_S2R_SW3
16.SOCHOT0_R_L
17.PPVDD_SRAM
18.PP3V0_UVLO
19.PMU_GPIO_OSCAR2PMU_HOST_WAKE
20.PMU_SHDWN
21.PP3V0_S2R_NAVAJO
22.UART4_OSCAR2SOC_RXD
23.PPVDD_SOC
24.ACCEL2OSCAR_INT1
25.GPIO_OSCAR_RESET_L
26.PP2V9_CAM
27.PPVBUS_USB_DCIN
28.PPVDD_GPU
29.DWI_AP_CLK
30.SOCHOT1_L
31.PPVDD_CPU
32.PP1V0_SOC
33.USB_VBUS_DETECT
34.PP1V8_ALWAYS
35.BOARD_TEMP2_P
36.GPIO_PMU2SOC_IRQ_L
37.PP3V0_S2R_TRISTAR
38.PP2V6_CAM_AF
39.VBUS_PROT_G
40.PMU_TCAL
41.PP3V0_ALS
42.PMU_GPIO_PMU2BBPMU_RST_L
43.PPVBUS_PROT
44.BOARD_TEMP8_P
45.PMU_VCENTER
46.BOARD_TEMP6_P
47.TP_HV_CHG_EN
48.PPVCC_MAIN
49.TP_AMUX_B3
50.TP_AMUX_BY
51.TP_AMUX_AY
52.TP_AMUX_A3
53.PPVIN_APCHG
55. I2C0_SCL_1V8
56. I2C0_SDA_1V8

1.GPIO_SOC2BB_WAKE_MODEM
2.GPIO_BTN_VOL_UP_L
3.GYRO2OSCAR_INT2
4.GPIO_BTN_VOL_DOWN_L
5.GPIO_BTN_SRL_L_FILT
6.PP3V0_GYRO
7.SPI_OSCAR2GYRO_CS_L
8.GPIO_BTN_VOL_UP_L_FILT
9.SIMCRD_IO_CONN
10.SIMCRD_RST_CONN
11.GPIO_BTN_ONOFF_L_FILT
12.GPIO_BTN_VOL_DOWN_L_FILT
13.GPIO_HS4_SHUNT_EN
14.PP3V0_SPARE1
15.PP6V0_LCM_VBOOST
16.GPIO_BB2SOC_RESET_DET_L
17.UART_WLAN2BB_LTE_COEX
18&58.BATT_NTC
19.GPIO_SOC2BB_RADIO_ON_L
20.GPIO_BTN_SRL_L
21.GPIO_BTN_ONOFF_L
22.PA_NTC_P
23.PP_LDO6_RUIM_1V8
24.GPIO_CODEC2SOC_IRQ_L
25.SPI3_CODEC_MISO
26.SPI3_CODEC_SCLK
27.GPIO_BB2SOC_GSM_TXBURST
28.ACCEL2OSCAR_INT2
29.GYRO2OSCAR_INT1
30.GYRO_DEN
31.SPI_OSCAR2ACCEL_CS_L
32.PP3V0_ACCEL
33.PPBATT_POS_RC
34.AIN3P
35.DMIC1_FF_SCLK
36.AIN3N
37.SPI3_CODEC_MOSI
38.PMU_GPIO_CODEC_HS_INT_L
39.L81_SPEAKER_VQ
40.GND
41.GND_AUDIO_CODEC
42&64&65&66&69.PPBATT_VCC
43&57.BATT_SWI_CONN
44.PMU_GPIO_BB_VBUS_DET
45.PMU_GPIO_BB2PMU_HOST_WAKE
46.PP1V8_S2R
47.PPLED_OUT_B
48.COMPASS2OSCAR_INT
50&51&52&56&59&71&72.GND
53.UART_BB2WLAN_LTE_COEX
54.MIKEY_TS_P
55.MIKEY_TS_N
60.PP1V7_VA_VCP
61.PP1V7_VCP
62.L81_DMIC1_FF_SD
63.CODEC_HP_DET_R
67.GPIO_PROX2SOC_IRQ_L
70.BATT_SNS
73.PP_SMPS5_DSP_1V05
74.PP_LDO1

1.PP3V0_COMP
2.PP3V0_S2R_SENSOR
3.SPI_OSCAR_SCLK
4.SPI_OSCAR_MOSI
5.PP1V8_COMP
6.I2C0_CAM_ALS_SCL_1V8_F
7.GPIO_CAM_ALS2SOC_IRQ_L_F
8.ISP1_CAM_FRONT_SDA_F
9.ISP1_CAM_FRONT_SCL_F
10.PP3V0_ALS_FILT
11.I2C0_CAM_ALS_SDA_1V8_F
12.ISP1_CAM_FRONT_CLK_F
13.ISP1_CAM_FRONT_SHUTDOWN_L_F
14.PP2V9_AVDD_CAM_FRONT_FILT
15.PP1V8_CAM_FRONT_FILT
16.GPIO_HS3_SHUNT_EN_FILT
17.CONN_HP_HEADSET_DET_FILT
18.GPIO_HS4_SHUNT_EN_FILT
19.CONN_HP_HS4_REF_FILT
20.CONN_HP_HS3_FILT
21.CONN_HP_RIGHT_FILT
22.CONN_HP_LEFT_FILT
23. CONN_HP_HS4_FILT
24.CONN_HP_HS3_REF_FILT
25.BOARD_TEMP4_P
26.DMIC1_FF_SCLK_FILT
27.DMIC1_FF_SD
28.DMIC1_FF_SD_FILT
29.PP1V8_DMIC_FILT
30. GPIO_HS3_SHUNT_EN







I2S0 AND I2S2 ARE OPTIMIZED FOR LOW MCK JITTER

R0700 33.2 1% 1/32W MF 01005

L81 CODEC ASP 1.8V

L81 CODEC XSP 1.8V

UNUSED 1.8V

BT 1.8V

OMIT_TABLE

U0600 ALCATRAZ DISCRETE FBGA (3 OF 14)

| | | | | | |
|---|---|---|---|---|---|
| I2S0_CODEC_ASP_MCK_R_1 | | | I2S0_CODEC_ASP_MCK | F28 | I2S0_MCK |
| | | | I2S0_CODEC_ASP_BCLK | AJ32 | I2S0_BCLK |
| | | | I2S0_CODEC_ASP_LRCK | AH32 | I2S0_LRCK |
| | | | I2S0_CODEC_ASP_DIN | AG32 | I2S0_DIN |
| | | | I2S0_CODEC_ASP_DOUT | AJ33 | I2S0_DOUT |
| | | | NC_I2S1_MCK NO_TEST=TRUE | AG33 | I2S1_MCK |
| | | | I2S1_CODEC_XSP_BCLK | AH34 | I2S1_BCLK |
| | | | I2S1_CODEC_XSP_LRCK | AH33 | I2S1_LRCK |
| | | | I2S1_CODEC_XSP_DIN | AG34 | I2S1_DIN |
| | | | I2S1_CODEC_XSP_DOUT | AF32 | I2S1_DOUT |
| | | | NC_I2S2_MCK NO_TEST=TRUE | F26 | I2S2_MCK |
| | | | NC_I2S2_BCLK NO_TEST=TRUE | AG35 | I2S2_BCLK |
| | | | NC_I2S2_LRCK NO_TEST=TRUE | AE32 | I2S2_LRCK |
| | | | NC_I2S2_DIN NO_TEST=TRUE | AE33 | I2S2_DIN |
| | | | NC_I2S2_DOUT NO_TEST=TRUE | AF34 | I2S2_DOUT |
| | | | BB_JTAG_TRST_L | AD32 | I2S3_MCK |
| | | | BB_JTAG_TDI | AF36 | I2S3_BCLK |
| | | | BB_JTAG_TDO | AG36 | I2S3_LRCK |
| | | | BB_JTAG_TCK | AC32 | I2S3_DIN |
| | | | BB_JTAG_TMS | AD33 | I2S3_DOUT |
| | | | NC_I2S4_MCK NO_TEST=TRUE | AD34 | I2S4_MCK |
| | | | I2S4_SOC2BT_BCLK | AE36 | I2S4_BCLK |
| | | | I2S4_SOC2BT_LRCK | AE35 | I2S4_LRCK |
| | | | I2S4_BT2SOC_DATA | AB32 | I2S4_DIN |
| | | | I2S4_SOC2BT_DATA | AC33 | I2S4_DOUT |
| | | | GPIO_BOARD_ID_2 | AN4 | SPI0_MISO |
| | | | GPIO_BOARD_ID_1 | AP2 | SPI0_MOSI |
| | | | GPIO_BOARD_ID_0 | AN3 | SPI0_SCLK |
| | | | NC_SPI0_SSIN NO_TEST=TRUE | AM9 | SPI0_SSIN |
| | | | NC_SPI1_MISO NO_TEST=TRUE | AN1 | SPI1_MISO |
| | | | NC_SPI1_MOSI NO_TEST=TRUE | AM4 | SPI1_MOSI |
| | | | NC_SPI1_SCLK NO_TEST=TRUE | AM5 | SPI1_SCLK |
| | | | NC_SPI1_SSIN NO_TEST=TRUE | AM7 | SPI1_SSIN |
| | | | SPI2_GRAPE_MISO | AN8 | SPI2_MISO |
| | | | SPI2_GRAPE_MOSI | AN7 | SPI2_MOSI |
| | | | SPI2_GRAPE_SCLK | AN5 | SPI2_SCLK |
| | | | SPI2_GRAPE_CS_L | AN9 | SPI2_SSIN |
| | | | SPI3_CODEC_MISO | AN13 | SPI3_MISO |
| | | | SPI3_CODEC_MOSI | AT6 | SPI3_MOSI |
| | | | SPI3_CODEC_SCLK | AR7 | SPI3_SCLK |
| | | | SPI3_CODEC_CS_L | AP10 | SPI3_SSIN |
| | | | I2C0_SCL_1V8 | AN6 | I2C0_SCL |
| | | | I2C0_SDA_1V8 | AP4 | I2C0_SDA |
| | | | I2C1_SOC2OSCAR_SWDCLK_1V8 | AP5 | I2C1_SCL |
| | | | I2C1_SOC2OSCAR_SWDIO_1V8 | AR3 | I2C1_SDA |
| | | | I2C2_SCL_1V8 | AR14 | I2C2_SCL |
| | | | I2C2_SDA_1V8 | AT7 | I2C2_SDA |
| | | | I2C3_SCL_1V8 | AA35 | I2C3_SCL |
| | | | I2C3_SDA_1V8 | AA36 | I2C3_SDA |
| | | | DWI_AP_CLK | AT17 | DWI_CLK |
| | | | SOC_TST_CPUSWITCH_OUT | AT16 | DWI_DI |
| | | | DWI_AP_DO | AR16 | DWI_DO |
| | | | NC_SEP_7816UART0_RST NO_TEST=TRUE | AL1 | SEP_7816UART0_RST |
| | | | SEP_I2C0_SCL | AK5 | SEP_7816UART0_SCL |
| | | | SEP_I2C0_SDA | AK3 | SEP_7816UART0_SDA |
| | | | NC_SEP_7816UART1_RST NO_TEST=TRUE | AM1 | SEP_7816UART1_RST |
| | | | NC_SEP_7816UART1_SCL NO_TEST=TRUE | AL4 | SEP_7816UART1_SCL |
| | | | NC_SEP_7816UART1_SDA NO_TEST=TRUE | AL2 | SEP_7816UART1_SDA |
| | | | HSIC1_WLAN2SOC_REMOTE_WAKE | Y32 | SIO_7816UART0_RST |
| | | | HSIC1_WLAN2SOC_DEVICE_RDY | AB33 | SIO_7816UART0_SCL |
| | | | HSIC1_SOC2WLAN_HOST_RDY | AA32 | SIO_7816UART0_SDA |
| | | | HSIC2_BB2SOC_REMOTE_WAKE | AA34 | SIO_7816UART1_RST |
| | | | HSIC2_BB2SOC_DEVICE_RDY | AC36 | SIO_7816UART1_SCL |
| | | | HSIC2_SOC2BB_HOST_RDY | AA33 | SIO_7816UART1_SDA |
| | | | SOCHOT0_L | AM20 | SOCHOT0 |
| | | | SOCHOT1_L | AM19 | SOCHOT1 |

TO: ANYA PMU 0111100X

TO: OSCAR SWD NOTE: I2C1 IS ASSUMED TO USE PUSH-PULL INSTEAD OF OPEN-DRAIN

TO: TRISTAR 0011010X

TO: AD7149 PROX 0101101X FF CAM CT817 ALS 0111001X

TP0700 TP-P55

OMIT_TABLE

U0600 ALCATRAZ DISCRETE FBGA (2 OF 14)

| | | | |
|---|---|---|---|
| GPIO_BTN_HOME_L | AB6 | GPIO00 | |
| GPIO_BTN_ONOFF_L | AD1 | GPIO01 | |
| GPIO_BTN_VOL_DOWN_L | AB5 | GPIO02 | |
| GPIO_BTN_VOL_UP_L | AC5 | GPIO03 | |
| GPIO_CAM_ALS2SOC_IRQ_L | AC6 | GPIO04 | |
| GPIO_BT_WAKE | AD3 | GPIO05 | |
| GPIO_SOC2BB_WAKE_MODEM | AD4 | GPIO06 | |
| NC_GPIO7 NO_TEST=TRUE | AE1 | GPIO07 | |
| GPIO_SOC2BB_RST_L | AE2 | GPIO08 | |
| GPIO_SOC2BB_RADIO_ON_L | AD5 | GPIO09 | |
| GPIO_BB2SOC_RESET_DET_L | AF1 | GPIO10 | |
| NC_GPIO11 NO_TEST=TRUE | AF2 | GPIO11 | |
| GPIO_SOC2OSCAR_DBGEN | AE4 | GPIO12 | |
| GPIO_SOC2GRAPE_RESET_L | AF3 | GPIO13 | |
| NC_GPIO14 NO_TEST=TRUE | AE5 | GPIO14 | |
| GPIO_BB2SOC_GSM_TXBURST | AE6 | GPIO15 | |
| GPIO_BOARD_ID_3 | AG1 | GPIO16 | |
| GPIO_TS2SOC2PMU_INT | AF4 | GPIO17 | |
| GPIO_BOOT_CONFIG_0 | AG3 | GPIO18 | |
| GPIO_BB2SOC_GPS_SYNC | AF5 | GPIO19 | |
| GPIO_PROX2SOC_IRQ_L | AH1 | GPIO20 | |
| GPIO_SOC2LCD_PWREN | AG4 | GPIO21 | |
| GPIO_SOC2PMU_KEEPACT | AR10 | GPIO22 | |
| GPIO_PMU2SOC_IRQ_L | AN14 | GPIO23 | |
| GPIO_CODEC2SOC_IRQ_L | AR9 | GPIO24 | |
| GPIO_BOOT_CONFIG_1 | AP13 | GPIO25 | |
| GPIO_FORCE_DFU | AT14 | GPIO26 | |
| TP_GPIO_DFU_STATUS | AT8 | GPIO27 | |
| GPIO_BOOT_CONFIG_2 | AM17 | GPIO28 | |
| GPIO_BOOT_CONFIG_3 | AT9 | GPIO29 | |
| GPIO_BTN_SRL_L | AP14 | GPIO30 | |
| GPIO_GRAPE2SOC_IRQ_L | AN16 | GPIO31 | |
| NC_GPIO32 NO_TEST=TRUE | AT11 | GPIO32 | |
| GPIO_HS3_SHUNT_EN | AT10 | GPIO33 | |
| GPIO_HS4_SHUNT_EN | AP11 | GPIO34 | |
| GPIO_BRD_REV3 | AN17 | GPIO35 | |
| GPIO_BRD_REV2 | AR13 | GPIO36 | |
| GPIO_BRD_REV1 | AP16 | GPIO37 | |
| GPIO_BRD_REV0 | AT13 | GPIO38 | |
| | | TMR32_PWM0 | AD35 OSCAR_TIME_SYNC_HOST_INT |
| | | TMR32_PWM1 | AC34 NC_TMR32_PWM1 NO_TEST=TRUE |
| | | TMR32_PWM2 | AD36 CLK_32K_SOC2CUMULUS |
| | | UART0_RXD | AR17 UART0_SOC_RXD |
| | | UART0_TXD | AP17 UART0_SOC_TXD |
| | | UART1_CTSN | AH4 UART1_BT2SOC_RTS_L |
| | | UART1_RTSN | AH2 UART1_SOC2BT_RTS_L |
| | | UART1_RXD | AG6 UART1_BT2SOC_TX |
| | | UART1_TXD | AG5 UART1_SOC2BT_TX |
| | | UART2_CTSN | AJ3 NC_GPIO_UART2_CTSN NO_TEST=TRUE |
| | | UART2_RTSN | AH5 NC_GPIO_UART2_RTSN NO_TEST=TRUE |
| | | UART2_RXD | AJ2 UART2_WLAN2SOC_TX |
| | | UART2_TXD | AJ1 UART2_SOC2WLAN_TX |
| | | UART3_CTSN | AK1 UART3_BB2SOC_RTS_L |
| | | UART3_RTSN | AJ6 UART3_SOC2BB_RTS_L |
| | | UART3_RXD | AJ5 UART3_BB2SOC_TX |
| | | UART3_TXD | AJ4 UART3_SOC2BB_TX |
| | | UART4_CTSN | AM3 PMU_GPIO_OSCAR2PMU_HOST_WAKE |
| | | UART4_RTSN | AM2 GPIO_OSCAR_RESET_L |
| | | UART4_RXD | AL5 UART4_OSCAR2SOC_RXD |
| | | UART4_TXD | AL6 UART4_SOC2OSCAR_TXD |
| | | UART5_RTXD | AK4 UART5_BATT_TRXD |
| | | UART6_RXD | AB36 UART6_TS_ACC_RXD |
| | | UART6_TXD | AB35 UART6_TS_ACC_TXD |

SOC DEBUG 1.8V

TO BT UART BCM4330

WIFI DEBUG

TO BB UART MDM9600

TO OSCAR

ACCESSORY UART 1.8V

## BUTTON PULLUPS

=PP1V8_ALWAYS

=PP1V8_S2R_MISC

R0722 100K 5% 1/32W MF 01005

R0720 100K 5% 1/32W MF 01005

NOSTUFF R0723 100K 5% 1/32W MF 01005

R0721 100K 5% 1/32W MF 01005

GPIO_BTN_SRL_L

GPIO_BTN_HOME_L

GPIO_BTN_ONOFF_L

=PP1V8_S2R_MISC

=PP1V8_SOC

R0760 100K 5% 1/32W MF 01005

R0761 100K 5% 1/32W MF 01005

SOCHOT1_L

SOCHOT0_L

## SEP EEPROM

UNPROGRAMMED P/N: 335S0894

=PP1V8_EEPROM

C9000 0.22UF 20% 6.3V X5R 01005

U9000 CAT24C08C4A WLCSP CRITICAL

VCC A1

VSS A2

SCL B1

SDA B2

SEP_I2C0_SCL

SEP_I2C0_SDA

GPIO_SOC2PMU_KEEPACT

GPIO_FORCE_DFU

GPIO_SOC2BB_RADIO_ON_L

HSIC1_SOC2WLAN_HOST_RDY

R0730 100K 5% 1/32W MF 01005

R0731 100K 5% 1/20W MF 201

NOSTUFF R0733 100K 5% 1/32W MF 01005

R0734 100K 5% 1/32W MF 01005

## I2C PULL-UPS

=PP1V8_SOC

R0750 2.2K 5% 1/32W MF 01005

R0751 2.2K 5% 1/32W MF 01005

R0752 2.2K 5% 1/32W MF 01005

R0753 2.2K 5% 1/32W MF 01005

R0754 2.2K 5% 1/32W MF 01005

R0755 2.2K 5% 1/32W MF 01005

R0756 2.2K 5% 1/32W MF 01005

R0757 2.2K 5% 1/32W MF 01005

NOSTUFF R0758 2.2K 5% 1/32W MF 01005

NOSTUFF R0759 2.2K 5% 1/32W MF 01005

I2C0_SDA_1V8

I2C0_SCL_1V8

I2C3_SDA_1V8

I2C3_SCL_1V8

I2C2_SDA_1V8

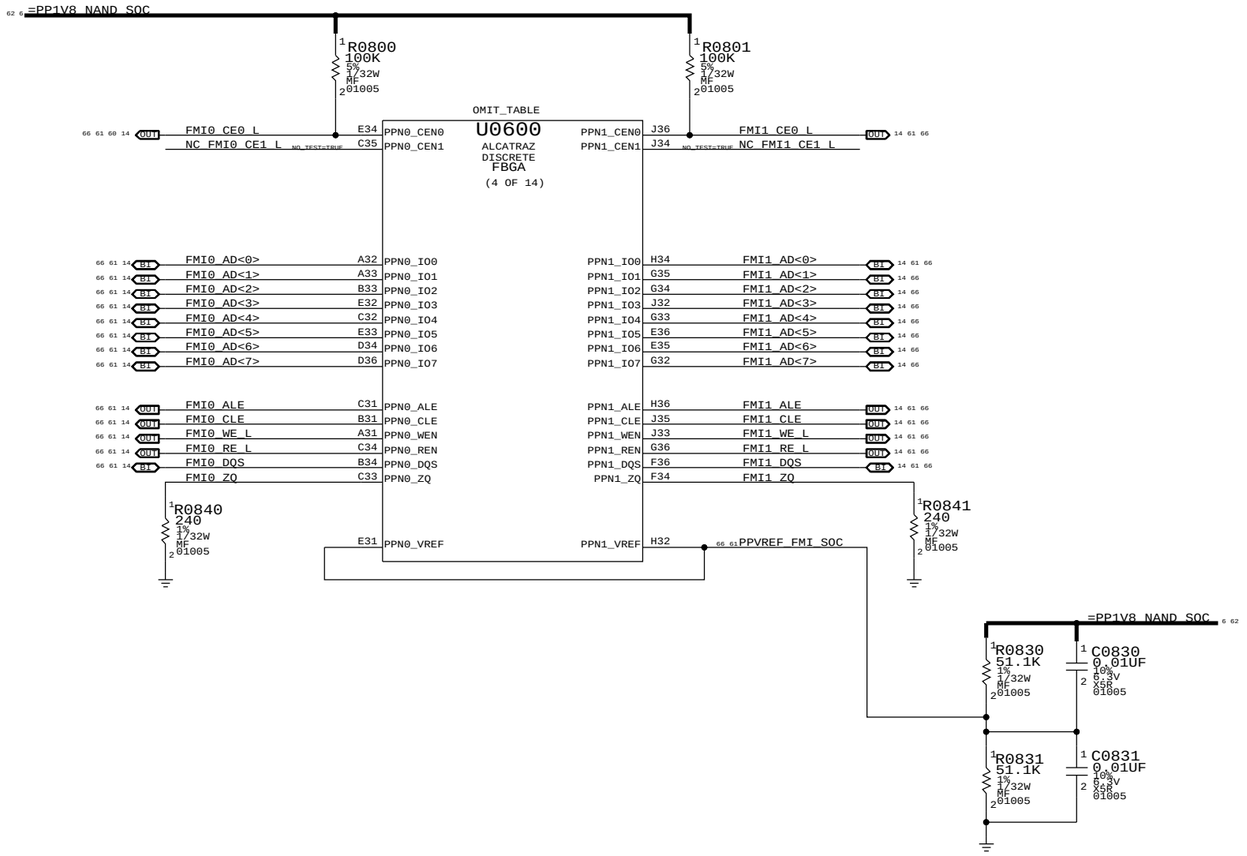
I2C2_SCL_1V8

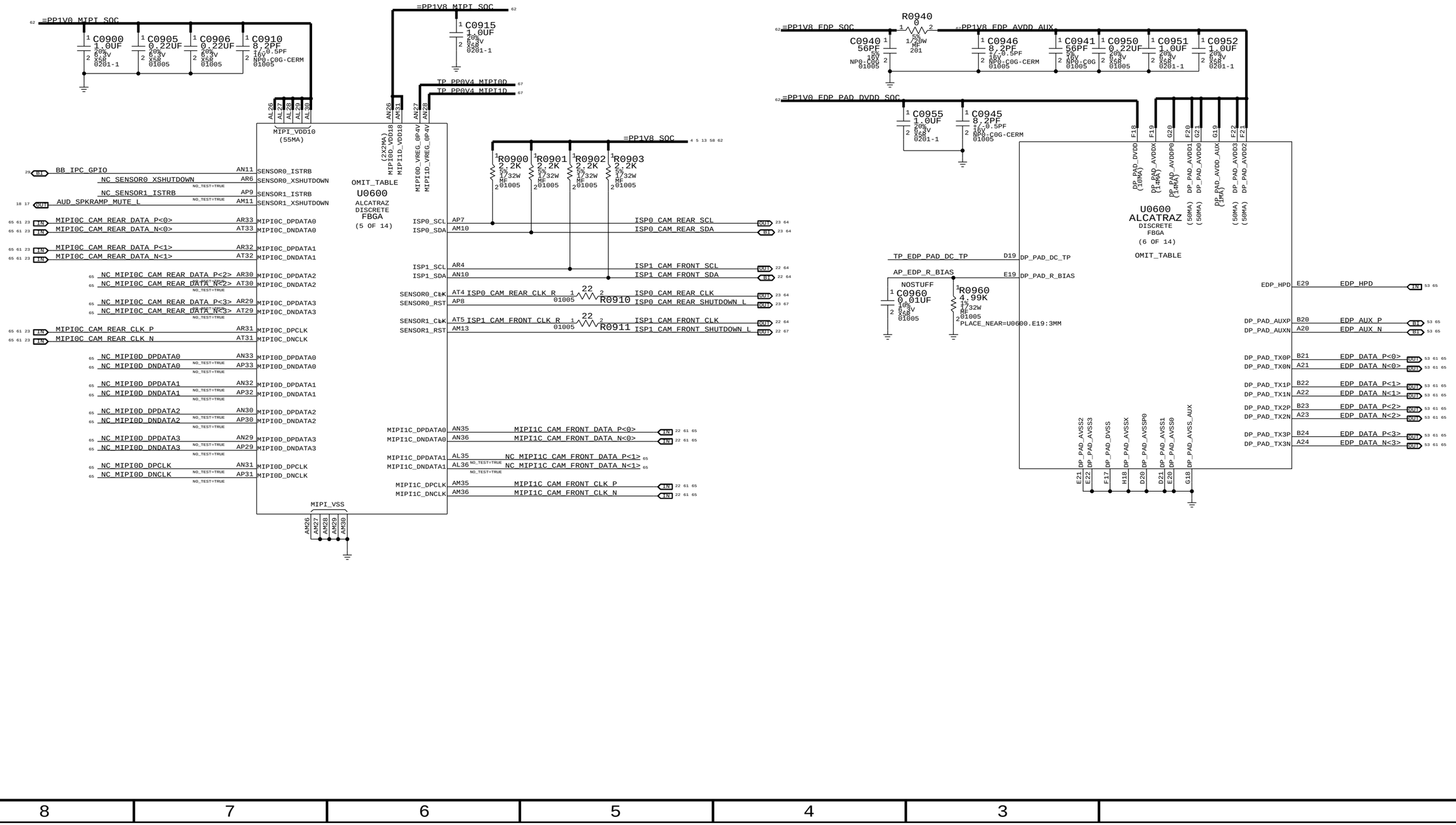
SEP_I2C0_SDA

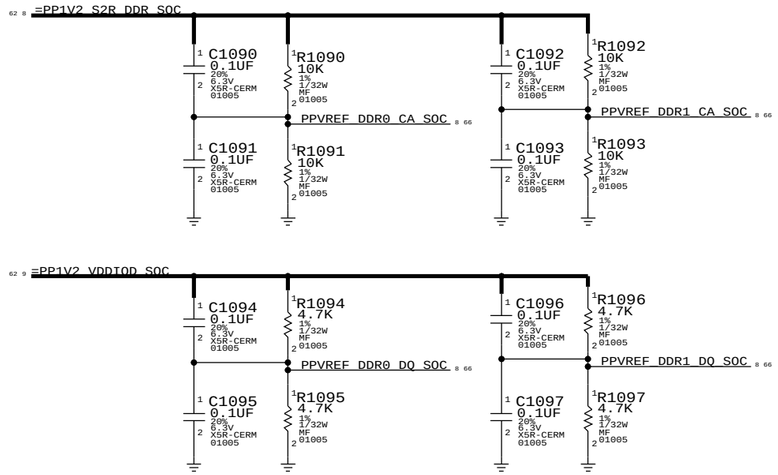
SEP_I2C0_SCL

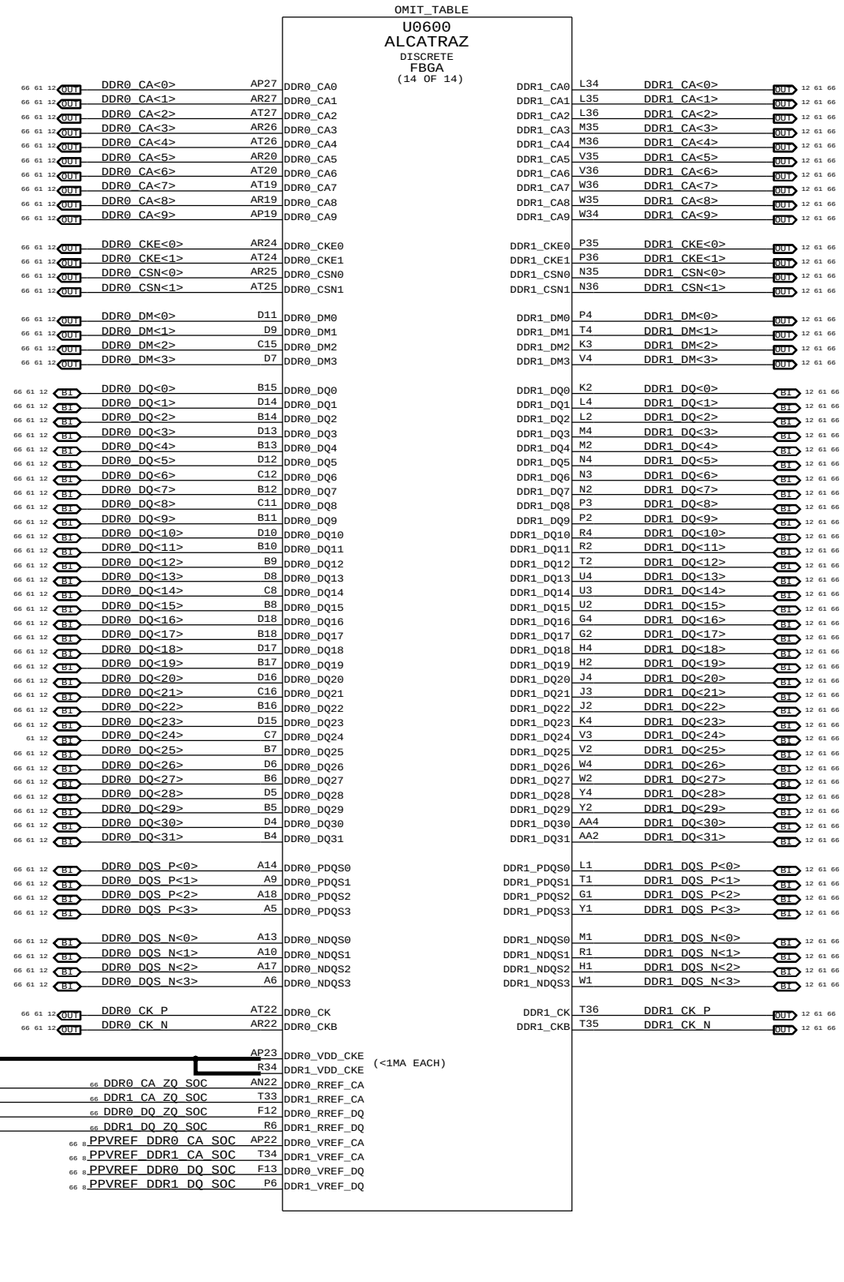
I2C1_SOC2OSCAR_SWDCLK_1V8

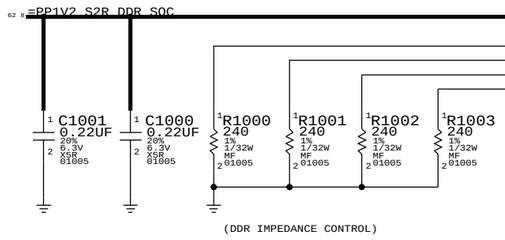
I2C1_SOC2OSCAR_SWDIO_1V8

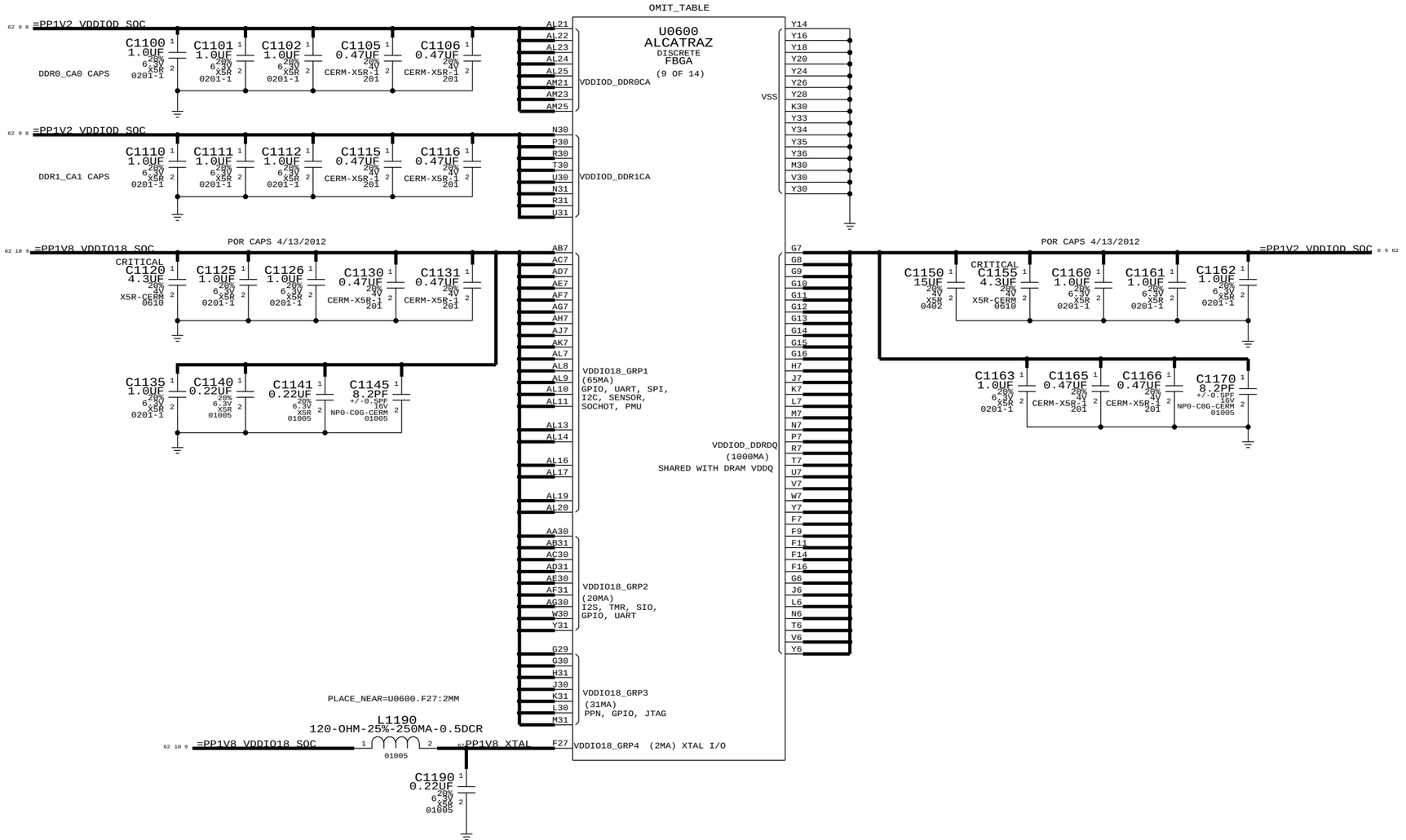


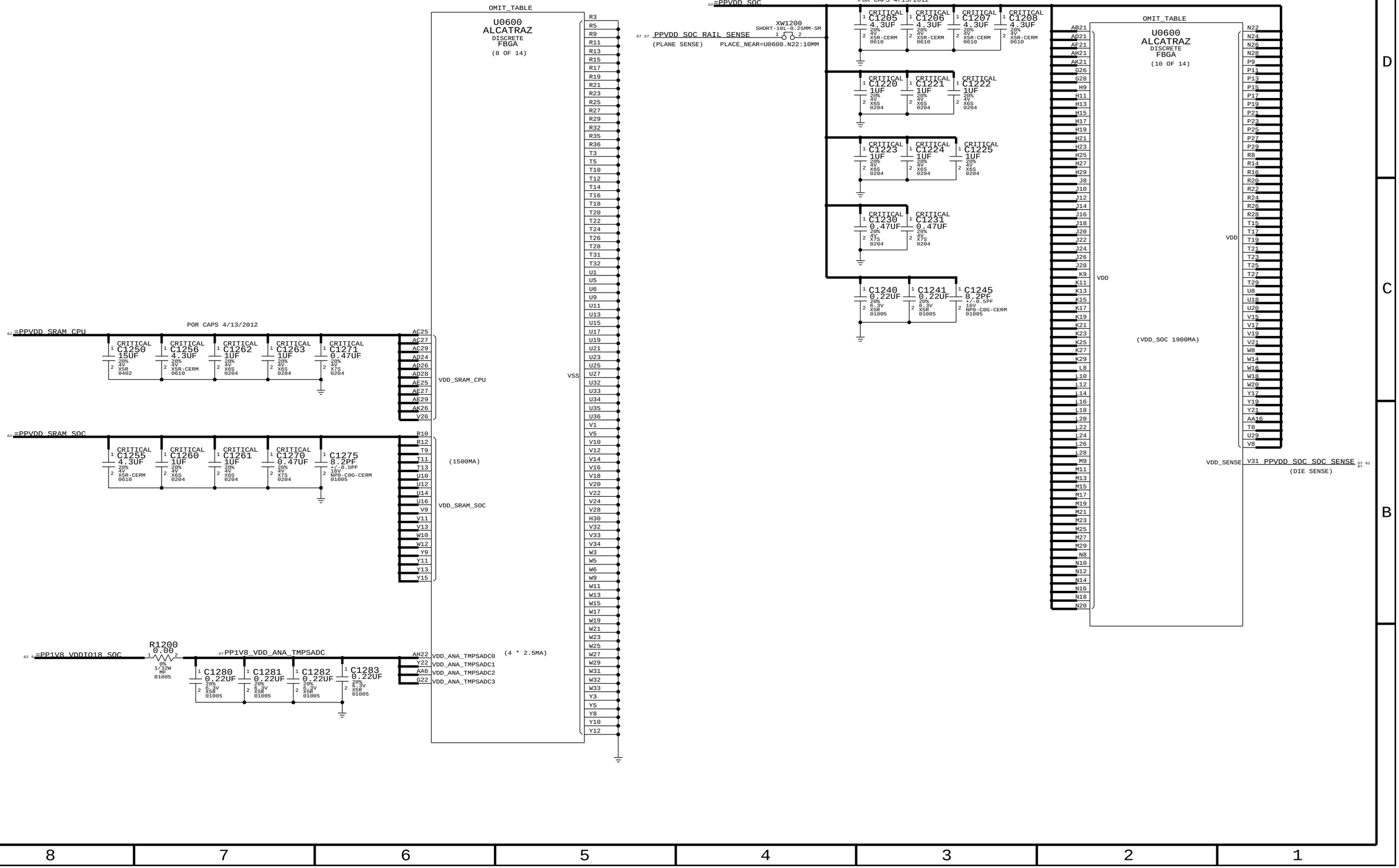


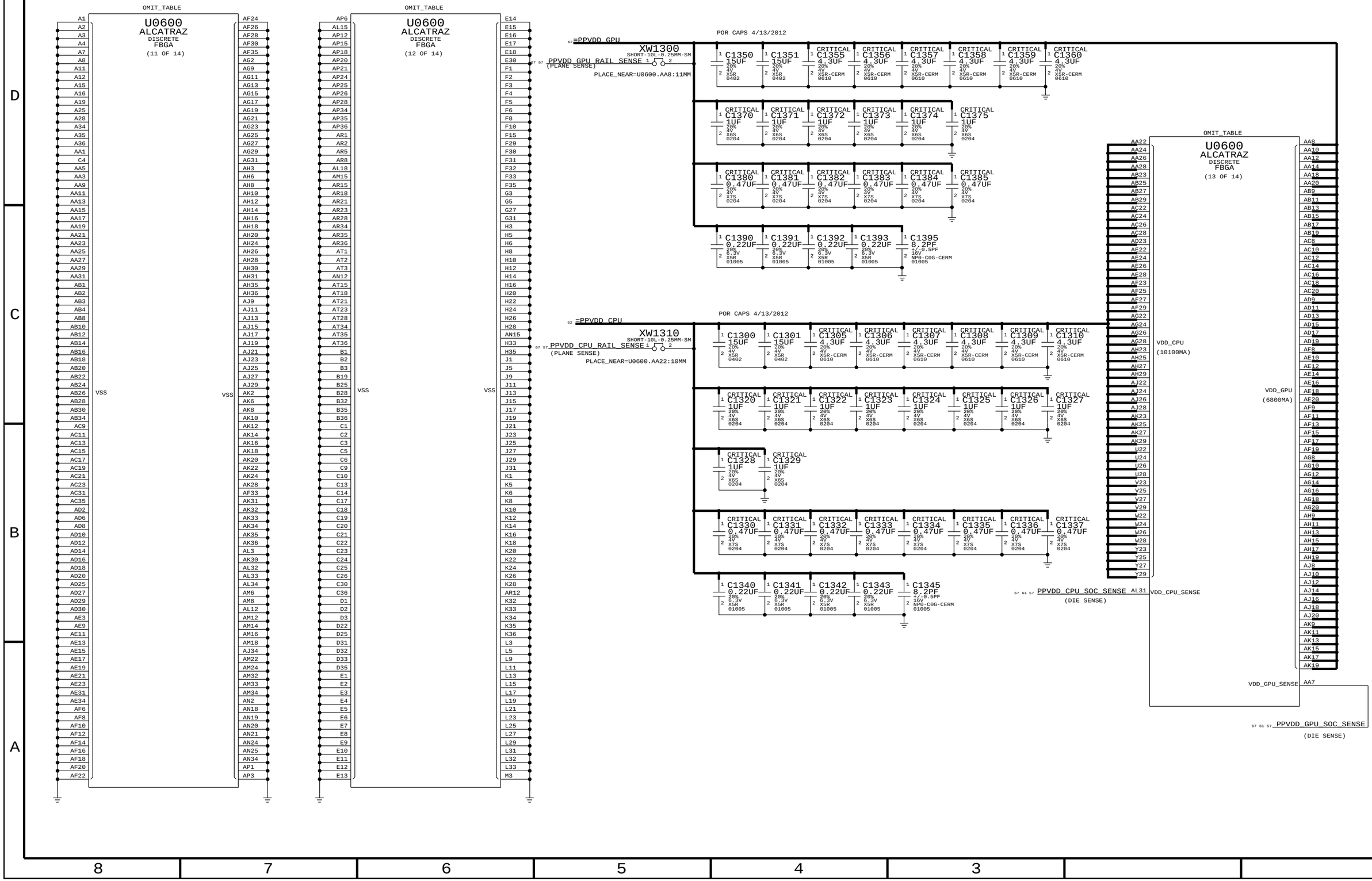


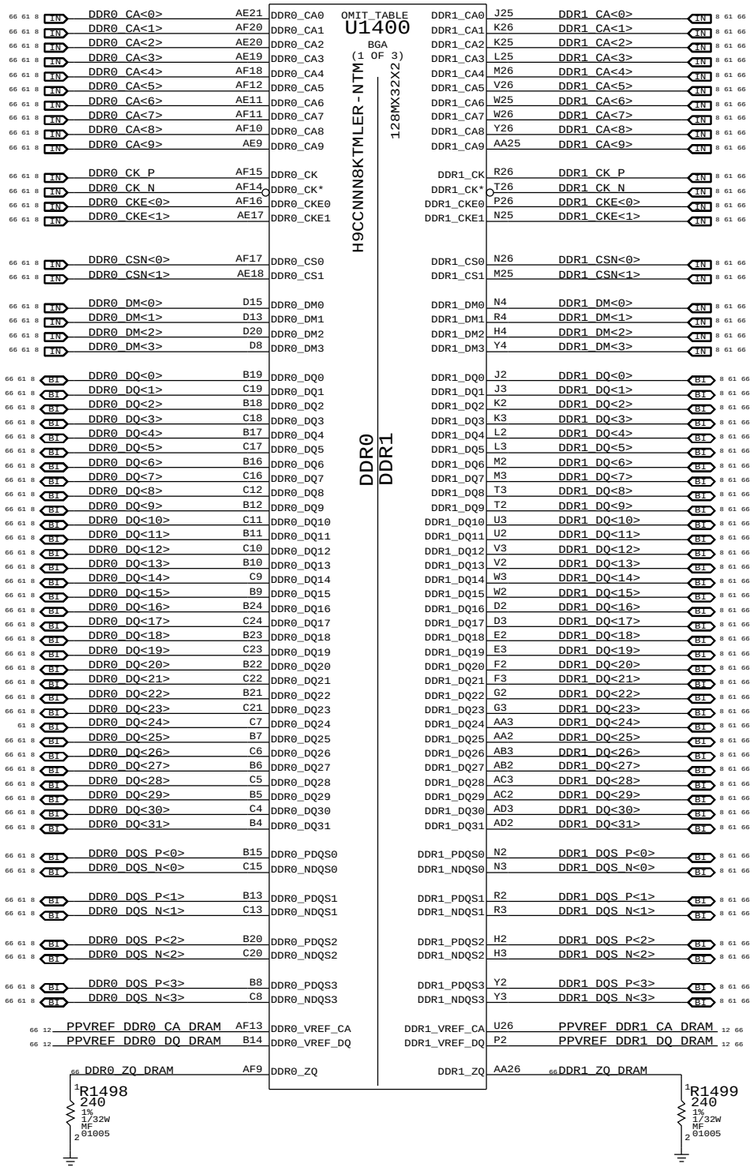



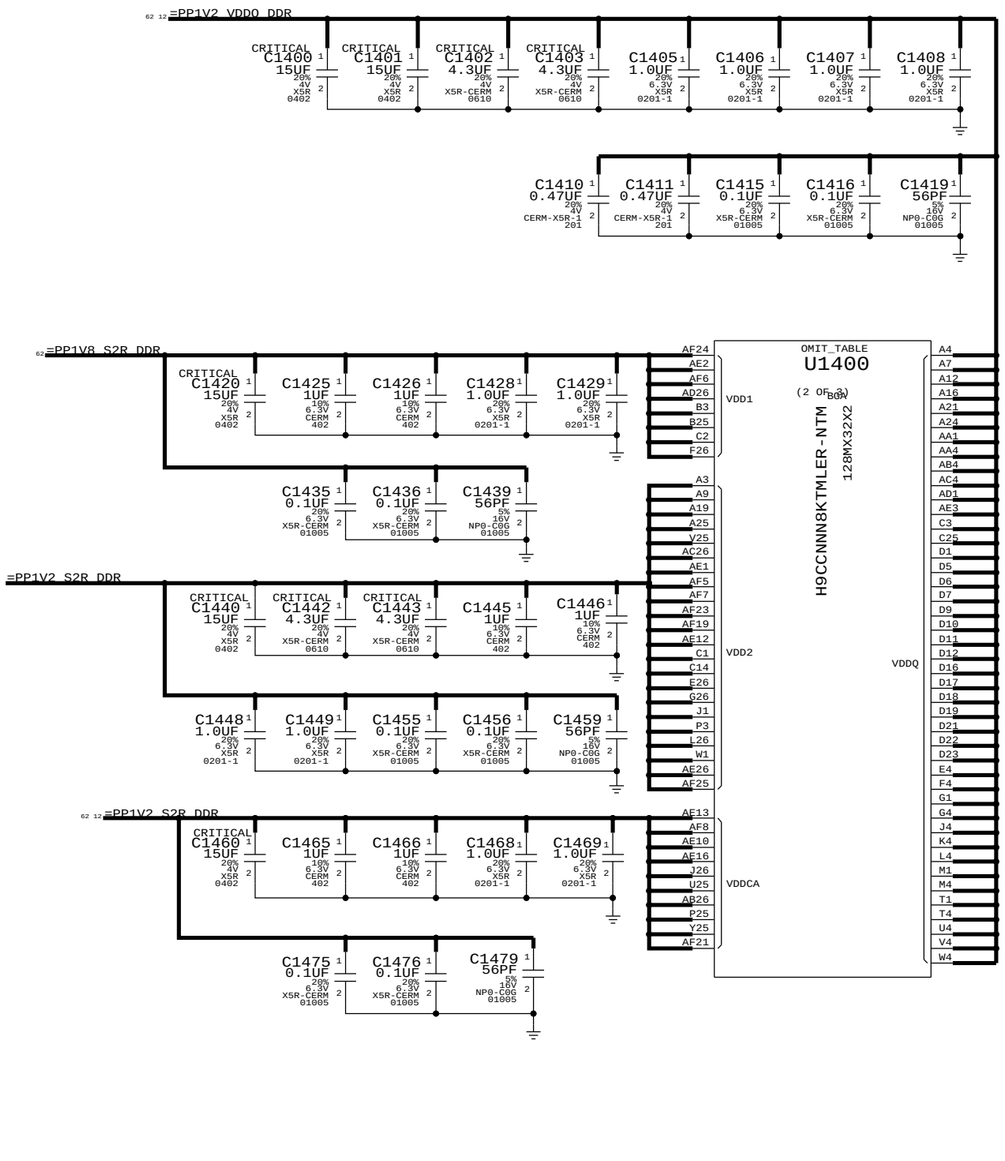



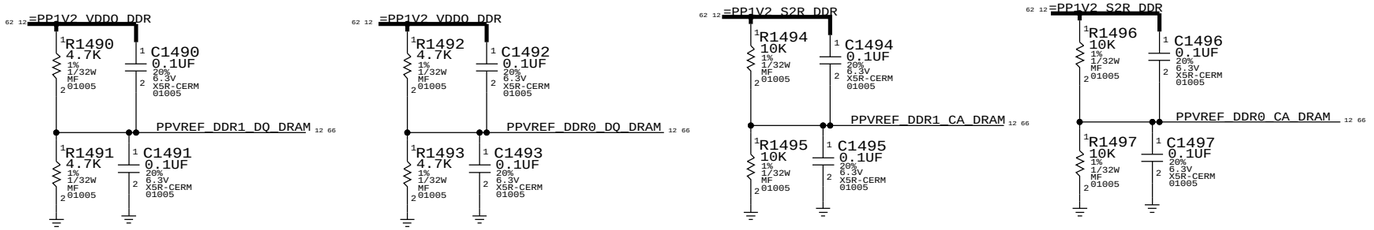




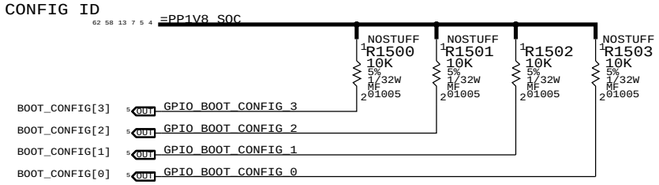




## BOOT CONFIG ID

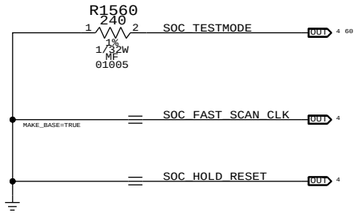



| BOOT_CONFIG[3:0] | MODE |
|---|---|
| 0000 | SPI |
| 0001 | SPI W/TEST |
| 0010 | NAND <-- CURRENT SETTING |
| 0011 | NAND W/TEST |

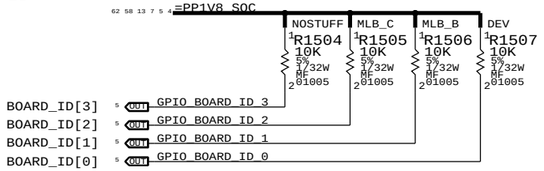
S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

## JTAG


## BOARD ID

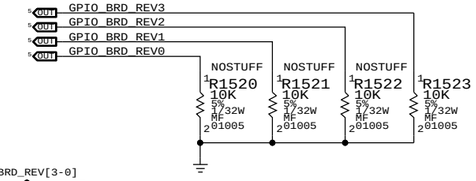



| BOARD_ID[3-0] | |
|---|---|
| 0000 | MLB_A AP |
| 0001 | MLB_A DEV |
| 0010 | MLB_B AP |
| 0011 | MLB_B DEV |
| 0100 | MLB_C AP |
| 0101 | MLB_C DEV |

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

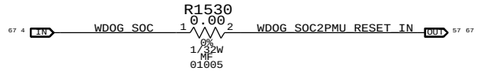
## BOARD REVISION

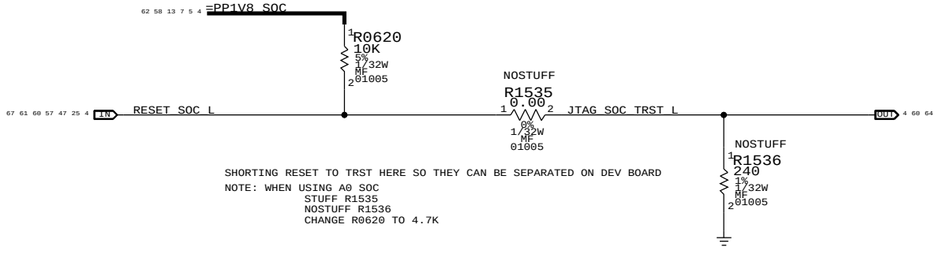



| BRD_REV[3-0] | |
|---|---|
| 0000 | PROTO 0 |
| 0001 | PROTO 0 + T2 |
| 0010 | PROTO 1 + T2 |
| 0011 | PROTO 1 + T1 |
| 0100 | PROTO 1 + T1 + B0 |
| 0101 | PROTO 2 + T2 + B0 |
| 0110 | EVT + T2 + B0 |
| CURRENT SETTING ---> 0111 | DVT + T2 + B1 |

S/W READ FLOW

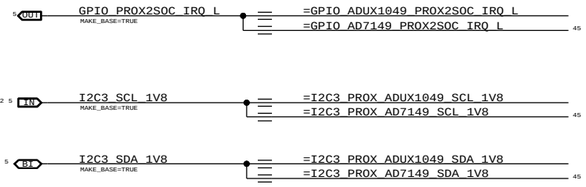
1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

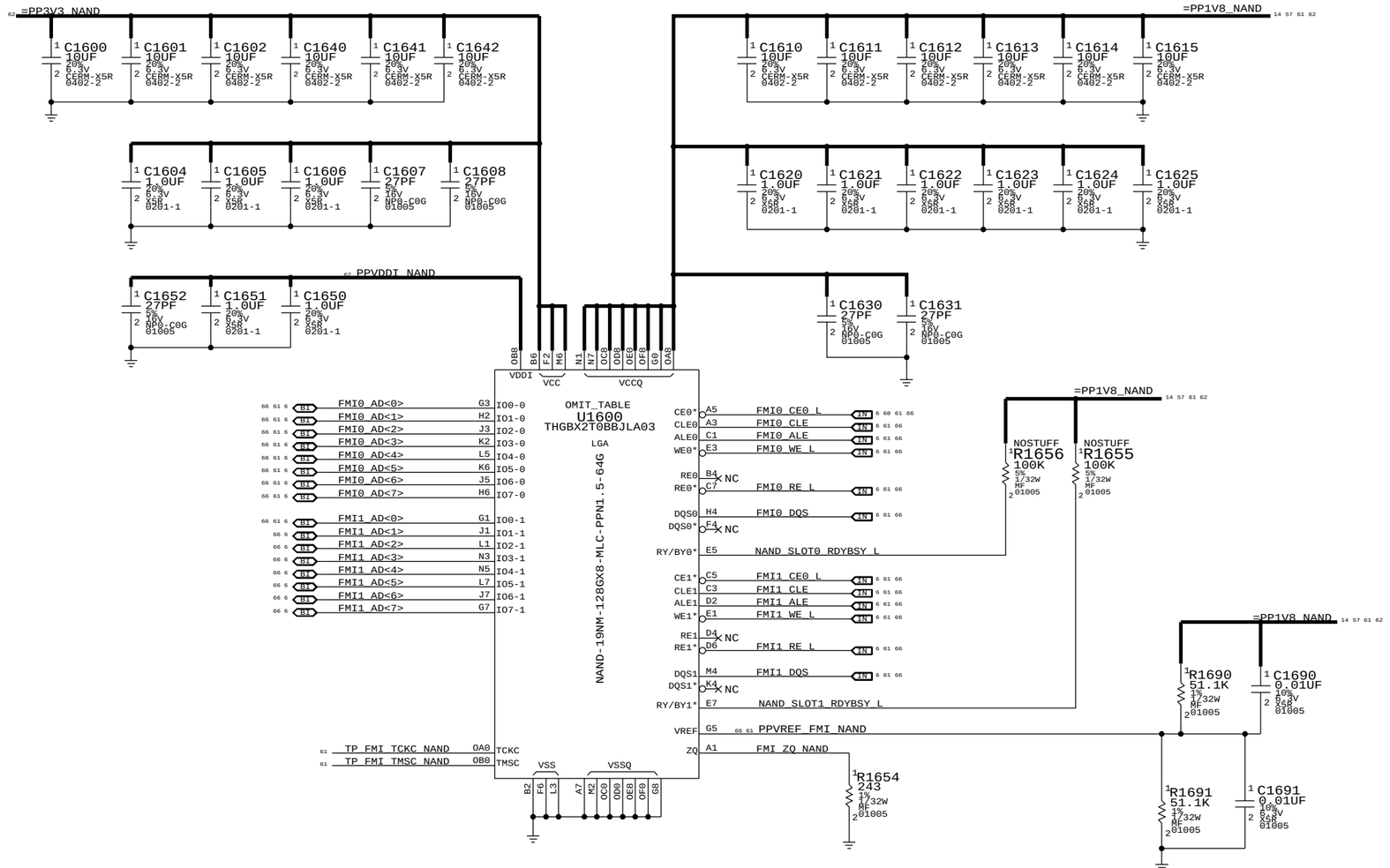



SHORTING RESET TO TRST HERE SO THEY CAN BE SEPARATED ON DEV BOARD
NOTE: WHEN USING A0 SOC
STUFF R1535
NOSTUFF R1536
CHANGE R0620 TO 4.7K

ALIASED NETS TO ALLOW BREAKING ON DEV BOARD

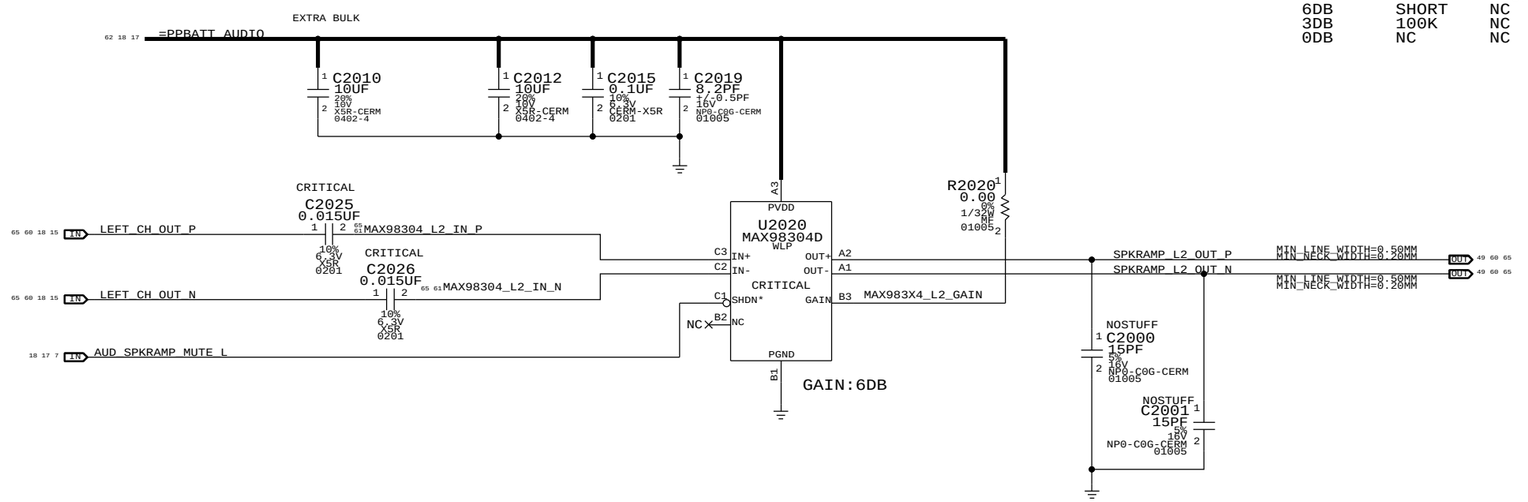


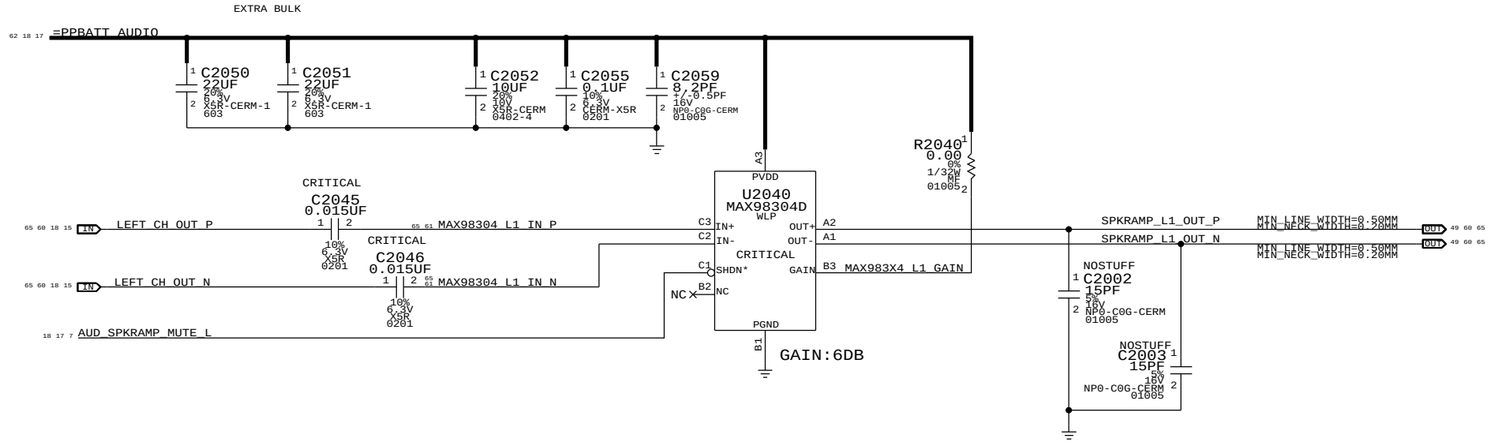


# SPEAKER AMPLIFIER

APN:353S3445
TURN ON TIME: 3.5MS
75HZ +/- XXX%  TURN ON DELAY: ?MS

| GAIN | VDD | GND |
|---|---|---|
| 12DB | NC | SHORT |
| 9DB | NC | 100K |
| 6DB | SHORT | NC |
| 3DB | 100K | NC |
| 0DB | NC | NC |

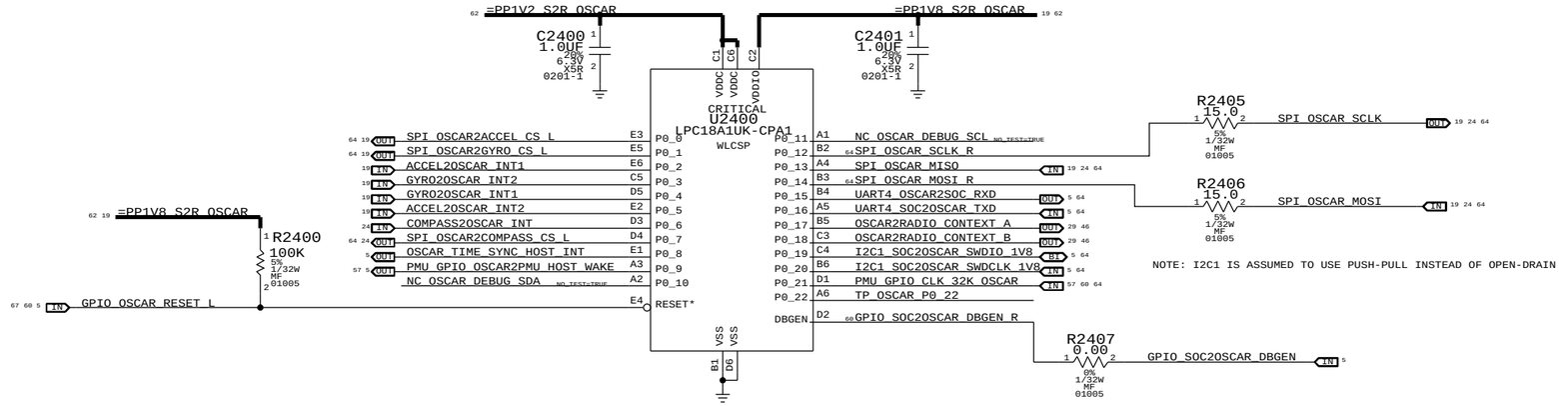


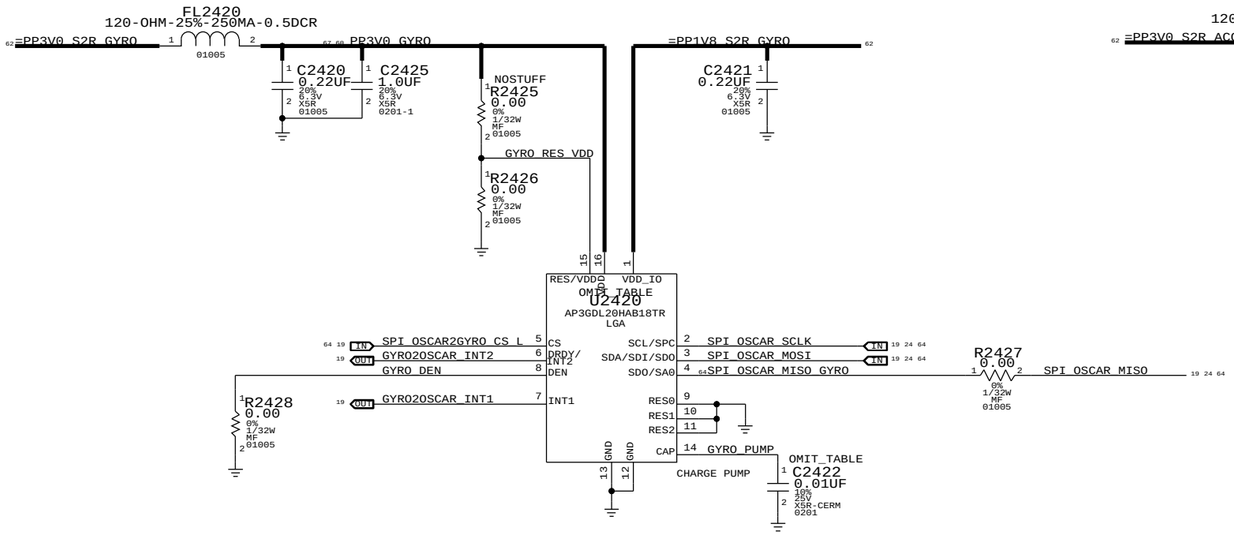
# OSCAR

APN 337S4416 (A1)

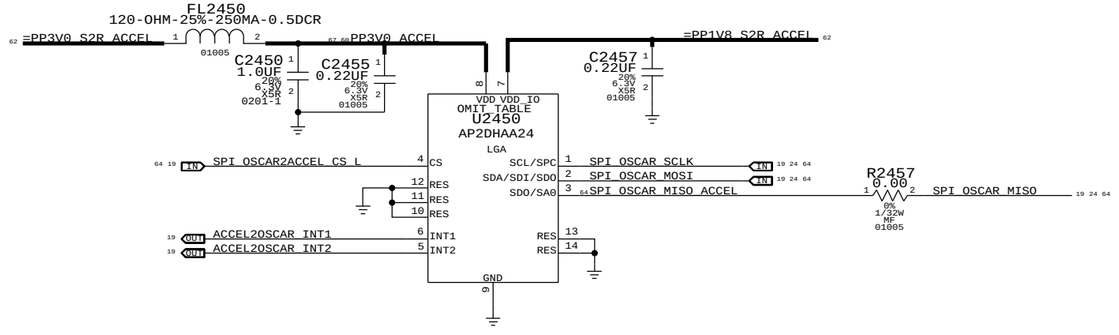
OSCAR VDDIO = 1.8V HIBERNATE (NEED TO WAKE HOST)
OSCAR CORE = 1.2V HIBERNATE (NEED TO RUN IN S2R)




## GYRO



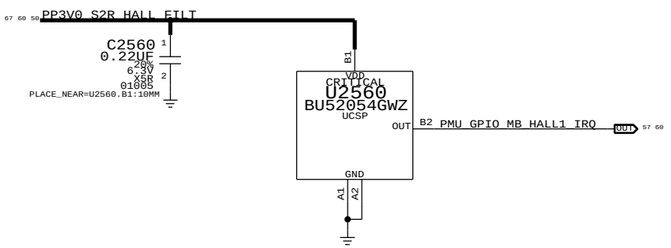

## ACCELEROMETER



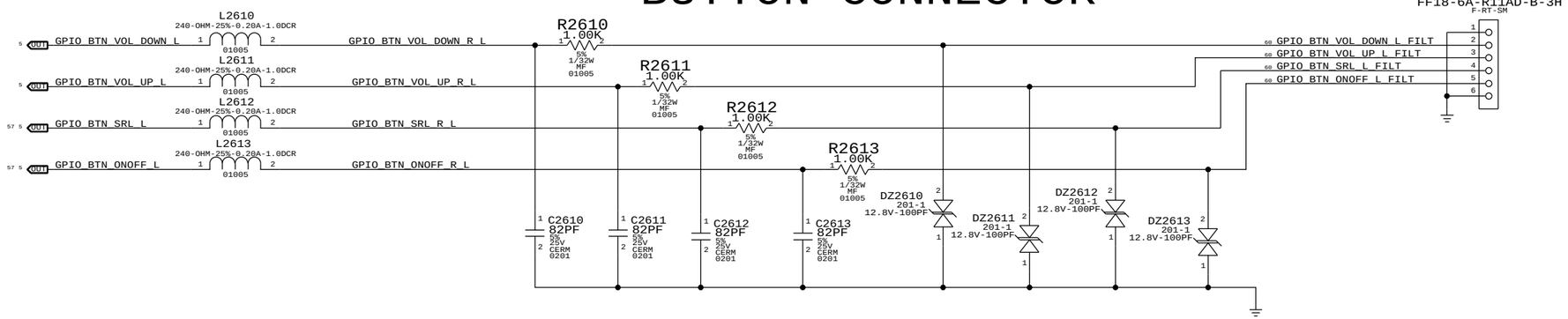
# HALL EFFECT

BIPOLAR ONE OUTPUT APN 353S3687

C-PANEL HALL EFFECT SENSOR
(B-PANEL HALL EFFECT SENSOR ON HB)



# BUTTON CONNECTOR



# FRONT CAMERA CONNECTOR

## J65 CAMERA CONNECTOR

APN:MLB 516S0876
APN:FLEX 516S0869

CRITICAL
J2700
503548-1820
F-ST-SM

| | | | | | |
|---|---|---|---|---|---|
| 64 60 22 | I2C3_CAM_ALS_SCL_1V8_F | 2 | 1 | I2C3_CAM_ALS_SDA_1V8_F | 22 60 64 |
| 60 22 | GPIO_CAM_ALS2SOC_IRQ_L_F | 4 | 3 | ISP1_CAM_FRONT_CLK_F | 22 60 64 |
| 67 60 22 | PP3V0_ALS_FILT | 6 | 5 | | |
| | | 8 | 7 | ISP1_CAM_FRONT_SHUTDOWN_L_F | 22 60 67 |
| 65 61 22 | MIPI1C_CAM_FRONT_DATA_FILT_P<0> | 10 | 9 | ISP1_CAM_FRONT_SDA_F | 22 60 64 |
| 65 61 22 | MIPI1C_CAM_FRONT_DATA_FILT_N<0> | 12 | 11 | ISP1_CAM_FRONT_SCL_F | 22 60 64 |
| | | 14 | 13 | PP2V9_AVDD_CAM_FRONT_FILT | 22 60 67 |
| 65 61 22 | MIPI1C_CAM_FRONT_CLK_FILT_P | 16 | 15 | GND_AVDD_CAM_FRONT | 22 67 |
| 65 61 22 | MIPI1C_CAM_FRONT_CLK_FILT_N | 18 | 17 | PP1V8_CAM_FRONT_FILT | 22 60 67 |
| | | 22 | 21 | | |

L2780
80-OHM-25%-500MA
0201
62 =PP1V8_CAM_FRONT → PP1V8_CAM_FRONT_FILT 22 60 67
C2780 100PF 5% 16V NP0-C0G 01005
C2781 1.0UF 20% 6.3V X5R 0201-1
XW2780 SM
XW2781 SM
67 GND_PP1V8_CAM_FRONT

L2700
80-OHM-25%-500MA
0201
62 =PP2V9_CAM_FRONT → PP2V9_AVDD_CAM_FRONT_FILT 22 60 67
C2700 100PF 5% 16V NP0-C0G 01005
C2701 1.0UF 20% 6.3V X5R 0201-1
XW2700 SM
XW2701 SM
67 GND_PP2V9_CAM_FRONT
GND_AVDD_CAM_FRONT 22 67

L2702
80-OHM-25%-500MA
0201
62 =PP3V0_ALS → PP3V0_ALS_FILT 22 60 67
C2706 100PF 5% 16V NP0-C0G 01005
C2707 1.0UF 20% 6.3V X5R 0201-1

CRITICAL
L2710
65 61 22 MIPI1C_CAM_FRONT_CLK_FILT_P → MIPI1C_CAM_FRONT_CLK_P OUT 7 61 65
65 61 22 MIPI1C_CAM_FRONT_CLK_FILT_N → MIPI1C_CAM_FRONT_CLK_N OUT 7 61 65
TCM0605-1
90-OHM-50MA

CRITICAL
L2711
65 61 22 MIPI1C_CAM_FRONT_DATA_FILT_P<0> → MIPI1C_CAM_FRONT_DATA_P<0> OUT 7 61 65
65 61 22 MIPI1C_CAM_FRONT_DATA_FILT_N<0> → MIPI1C_CAM_FRONT_DATA_N<0> OUT 7 61 65
TCM0605-1
90-OHM-50MA

FL2730
70-OHM-300MA
DCR 0.45
01005-1
64 61 13 5 IN I2C3_SCL_1V8 → I2C3_CAM_ALS_SCL_1V8_F 22 60 64
C2730 27PF 5% 16V NP0-C0G 01005

FL2731
70-OHM-300MA
DCR 0.45
01005-1
64 61 13 5 IN I2C3_SDA_1V8 → I2C3_CAM_ALS_SDA_1V8_F 22 60 64
C2731 27PF 5% 16V NP0-C0G 01005

FL2740
70-OHM-300MA
DCR 0.45
01005-1
67 7 IN ISP1_CAM_FRONT_SHUTDOWN_L → ISP1_CAM_FRONT_SHUTDOWN_L_F 22 60 67
R2740 100K 5% 1/32W MF 01005
C2740 27PF 5% 16V NP0-C0G 01005

FL2750
70-OHM-300MA
DCR 0.45
01005-1
64 7 IN ISP1_CAM_FRONT_SCL → ISP1_CAM_FRONT_SCL_F 22 60 64
C2750 27PF 5% 16V NP0-C0G 01005

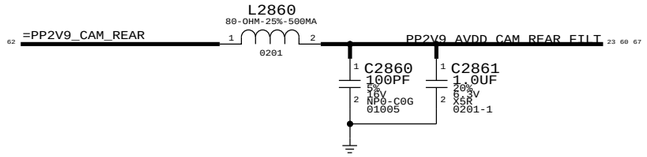
FL2751
70-OHM-300MA
DCR 0.45
01005-1
64 7 IN ISP1_CAM_FRONT_SDA → ISP1_CAM_FRONT_SDA_F 22 60 64
C2751 27PF 5% 16V NP0-C0G 01005

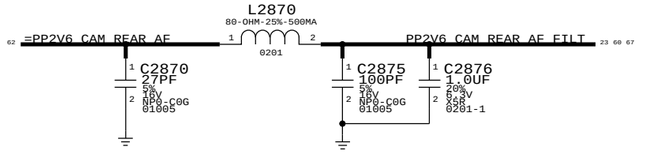
FL2760
150OHM-25%-200MA-0.7DCR
DCR 0.70
01005
64 7 IN ISP1_CAM_FRONT_CLK → ISP1_CAM_FRONT_CLK_F 22 60 64
C2760 56PF 5% 16V NP0-C0G 01005

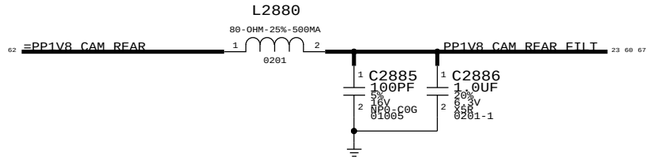
FL2770
70-OHM-300MA
DCR 0.45
01005-1
5 IN GPIO_CAM_ALS2SOC_IRQ_L → GPIO_CAM_ALS2SOC_IRQ_L_F 22 60

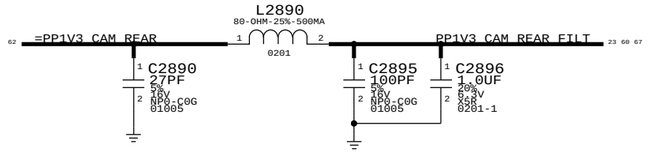
# REAR CAMERA CONNECTOR

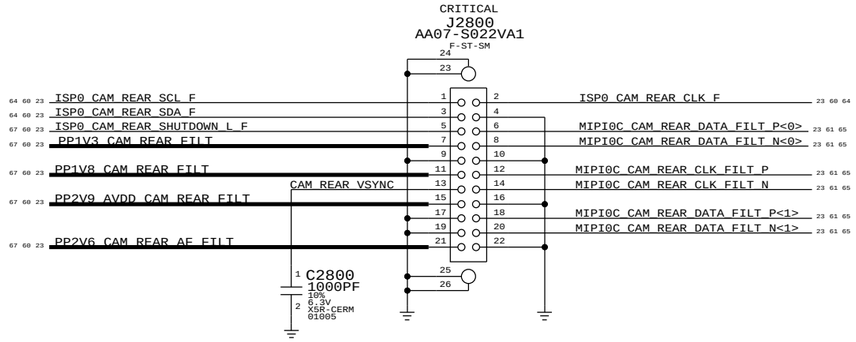
FLEX: 516S0974
MLB: 516S0973

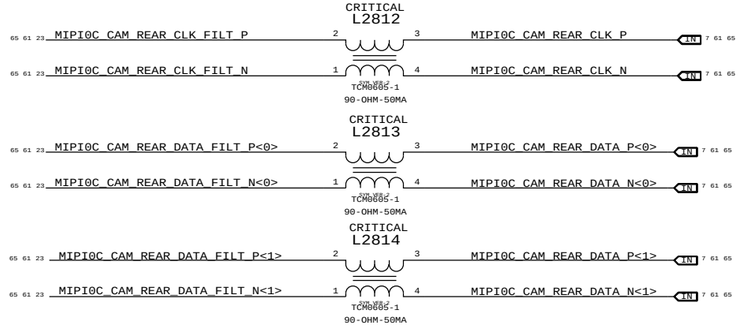


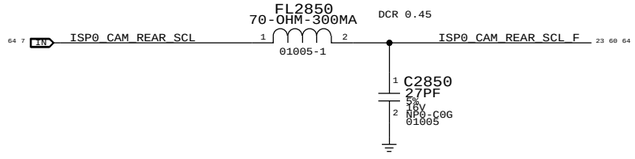



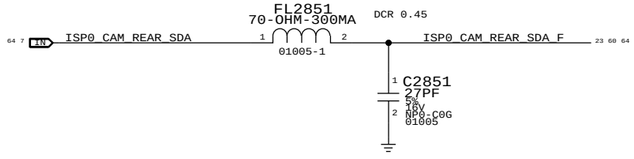



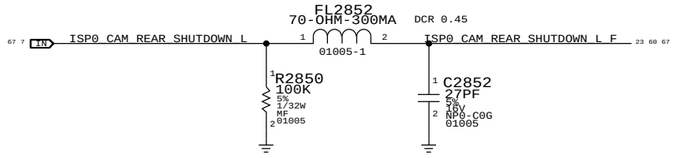



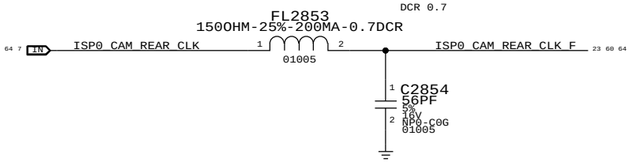



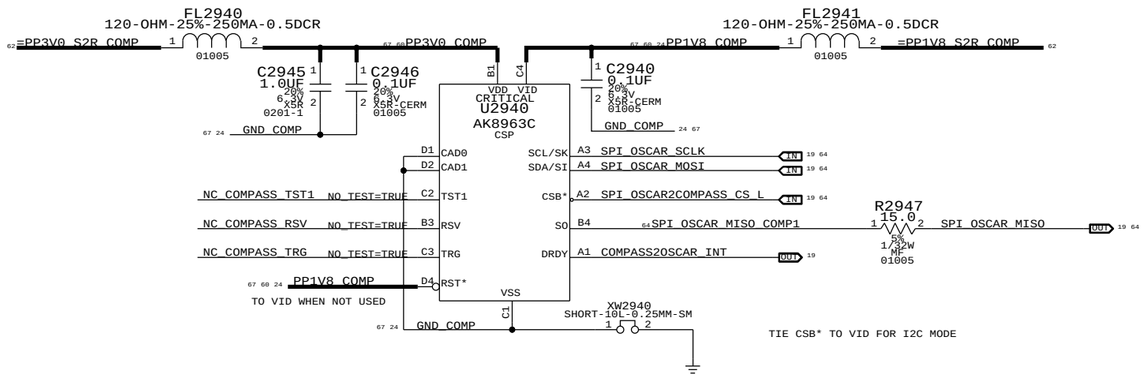



# COMPASS

APN 338S1014



# AP INTERFACE & DEBUG CONNECTOR

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

## PROBE POINTS

PP3000 — P4MM SM — PP 1 BB_ERROR_FLAG — 29 68
PP3001 — P4MM SM — PP 1 SLEEP_CLK_32K — 27 28 68
PP3002 — P4MM SM — PP 1 PMIC_SSBI — 27 28 68
PP3003 — P4MM SM — PP 1 19P2M_MDM — 27 28 68
PP3008 — P4MM SM — PP 1 WTR_SSBI_TX_GPS — 29 30
PP3009 — P4MM SM — PP 1 WTR_SSBI_PRX_DRX — 29 30
PP3010 — P4MM SM — PP 1 WTR_RX_ON — 29 30 68
PP3011 — P4MM SM — PP 1 WTR_RF_ON — 29 30 68
PP3012 — P4MM SM — PP 1 UART_WLAN2BB_LTE_COEX — 29 46
PP3013 — P4MM SM — PP 1 UART_BB2WLAN_LTE_COEX — 29 46

## DEBUG CONNECTOR

=PPBATT_VCC_BB — IN — 26 34 35 36 37 38 39 40 62

J3003
AXE654124
M-ST-SM
NOSTUFF

| | | | |
|---|---|---|---|
| | 56 | 55 | |
| | 2 | 1 | |
| | 4 | 3 | |
| | 6 | 5 | |
| 60 27 OUT PS_HOLD_PMIC | 8 | 7 | GPIO_SOC2BB_RST_L — OUT — 5 27 60 67 |
| 60 27 5 OUT GPIO_SOC2BB_RADIO_ON_L | 10 | 9 | PP_SMPS3_MSME_1V8 — IN — 25 26 28 29 31 60 |
| 67 60 57 27 OUT PMU_GPIO_PMU2BBPMU_RST_L | 12 | 11 | RESET_SOC_L — OUT — 4 13 47 57 60 61 67 |
| 68 28 27 IN PMIC_RESOUT_L | 14 | 13 | |
| | 16 | 15 | UART3_BB2SOC_TX — IN — 5 29 47 64 |
| | 18 | 17 | GPIO_DEBUG_LED — IN — 29 |
| | 20 | 19 | |
| | 22 | 21 | UART3_SOC2BB_TX — OUT — 5 29 47 64 |
| 67 61 28 OUT DEBUG_RST_L | 24 | 23 | UART3_BB2SOC_RTS_L — IN — 5 29 64 |
| 64 61 28 5 OUT BB_JTAG_TMS | 26 | 25 | UART3_SOC2BB_RTS_L — OUT — 5 29 64 |
| 64 61 28 5 OUT BB_JTAG_TRST_L | 28 | 27 | |
| 64 61 28 5 OUT BB_JTAG_TCK | 30 | 29 | |
| 64 61 28 5 IN BB_JTAG_TDO | 32 | 31 | |
| 64 61 28 5 OUT BB_JTAG_TDI | 34 | 33 | PMU_GPIO_BB_VBUS_DET — OUT — 28 57 61 67 |
| 28 OUT BB_JTAG_RTCLK | 36 | 35 | |
| | 38 | 37 | |
| 68 29 25 OUT LAT_SW1_CTL — GPIO48/BOOT_CONFIG_6 | 40 | 39 | |
| | 42 | 41 | |
| 68 40 29 OUT 2G_FEM_S1 — GPIO54/BOOT_CONFIG_0 | 44 | 43 | |
| 60 57 29 IN PMU_GPIO_BB2PMU_HOST_WAKE | 46 | 45 | HSIC2_BB2SOC_DEVICE_RDY — IN — 5 29 64 |
| 68 40 29 25 OUT 2G_FEM_S4 — GPIO53/BOOT_CONFIG_1 | 48 | 47 | |
| 29 OUT GPIO_51 — GPIO51/BOOT_CONFIG_3 | 50 | 49 | GPIO_BB2SOC_RESET_DET_L — IN — 5 29 67 |
| | 52 | 51 | HSIC2_SOC2BB_HOST_RDY — IN — 5 29 64 |
| | 54 | 53 | |
| | 58 | 57 | |

XW3002 — SHORT-10L-0.25MM-SM
64 47 BI USB_BB_N
64 61 28 BI USB_BB_DEBUG_N
64 61 28 BI USB_BB_DEBUG_P

XW3003 — SHORT-10L-0.25MM-SM
64 47 BI USB_BB_P

PP_SMPS3_MSME_1V8 — 25 26 28 29 31 60

NOSTUFF R3002 10K 5% 1/32W MF 01005
NOSTUFF R3003 10K 5% 1/32W MF 01005

68 29 25 LAT_SW1_CTL — GPIO48/BOOT_CONFIG_6
68 40 29 25 2G_FEM_S4 — GPIO53/BOOT_CONFIG_1

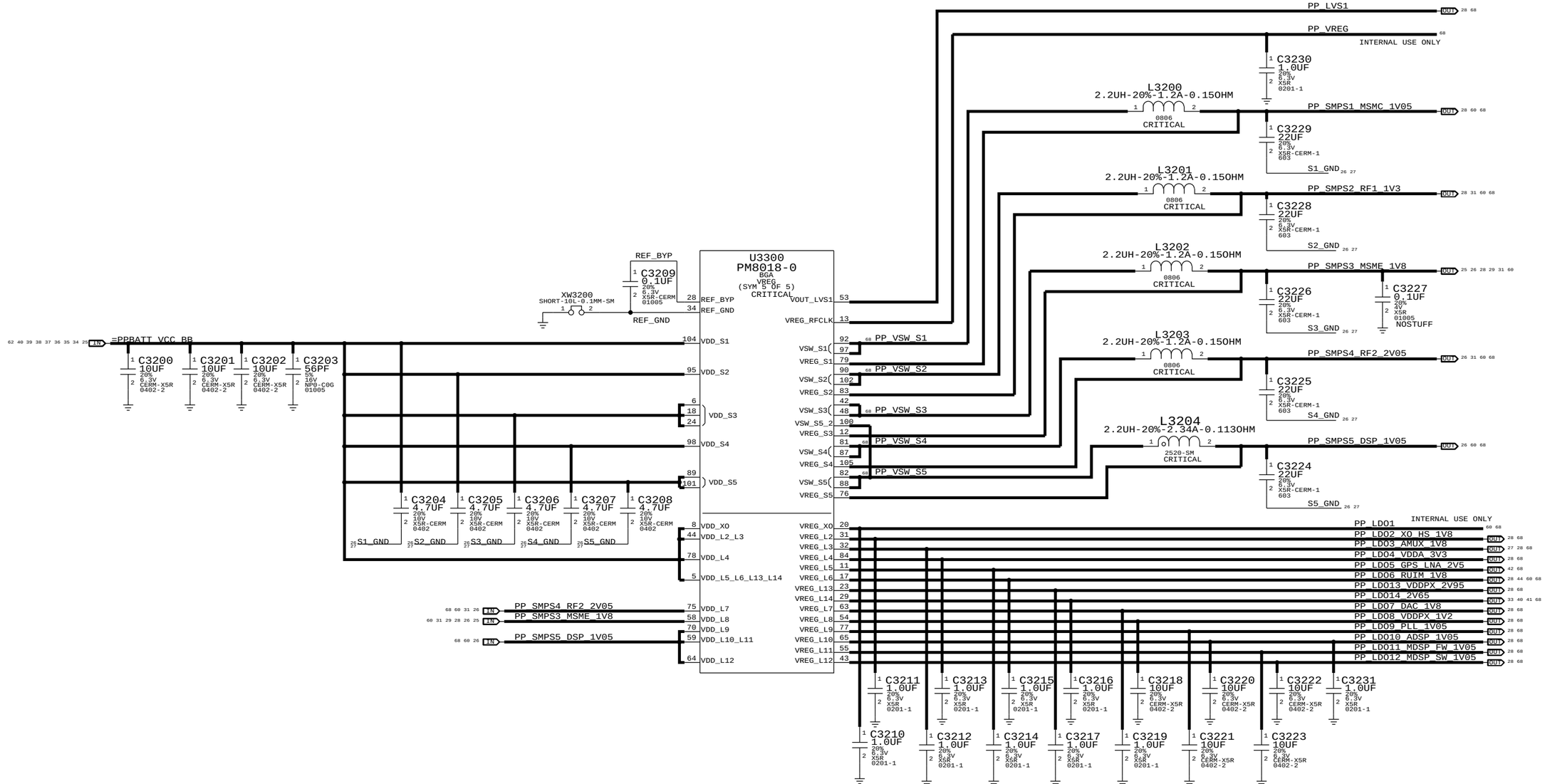
GPIO/BOOT_CONFIG CONFIGURATION

| BOOT OPTIONS | BOOT_CONFIG SW REGISTER VALUE | 6 (47) | 5 (48) | 4 (49) | 3 (50) | 2 (51) | 1 (52) | 0 (53) | (54) | (55) |
|---|---|---|---|---|---|---|---|---|---|---|
| BOOT_DEFAULT_OPTION | 0X00 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X |
| BOOT_NAND_OPTION | 0X01 | X | 1 | 0 | 0 | 0 | 0 | 1 | 0 | X |
| BOOT_HSIC_OPTION | 0X02 | X | 1 | 0 | 0 | 0 | 1 | 0 | 0 | X |
| BOOT_USB_OPTION | 0X03 | X | 1 | 0 | 0 | 0 | 1 | 1 | 0 | X |
| ENABLE SAHARA PROTOCOL | 0X08 | X | 1 | 0 | 0 | 1 | 0 | X | X | X |

J3002
MM4829-2702
F-ST-SM
NOSTUFF — 1 HSIC2_BB_DATA — 4 28 61 64
2 3 4

J3001
MM4829-2702
F-ST-SM
NOSTUFF — 1 HSIC2_BB_STB — 4 28 61 64
2 3 4

# BASEBAND PMU (1 OF 2)



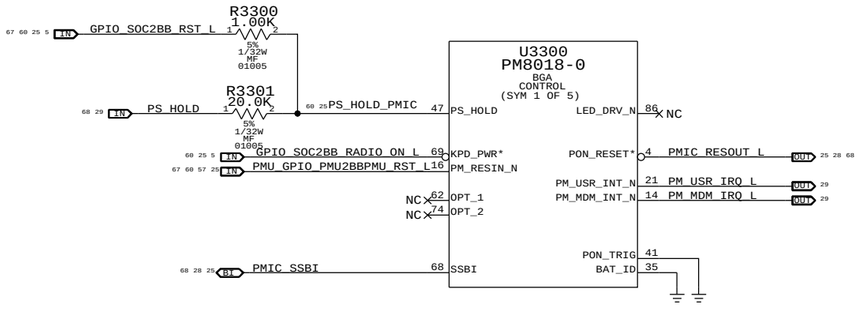
# BASEBAND PMU (2 OF 2)

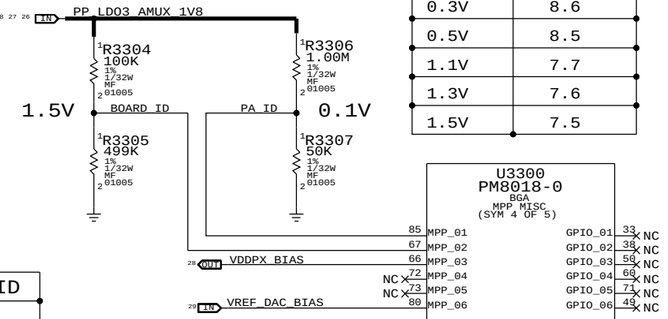
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

| BOARD_ID | REVISION |
|---|---|
| 0.7V | PROTO1 |
| 0.9V | PROTO2 |
| 1.1V | EVT1 |
| 1.3V | EVT2 |
| 1.5V | DVT |
| 1.7V | PVT |

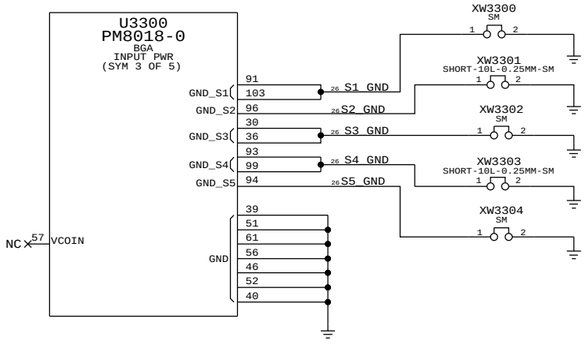
| BB GPIO_29 | PRODUCT_ID |
|---|---|
| 1 (1.8V) | JXX |
| 0 (NC, PD) | NXX |

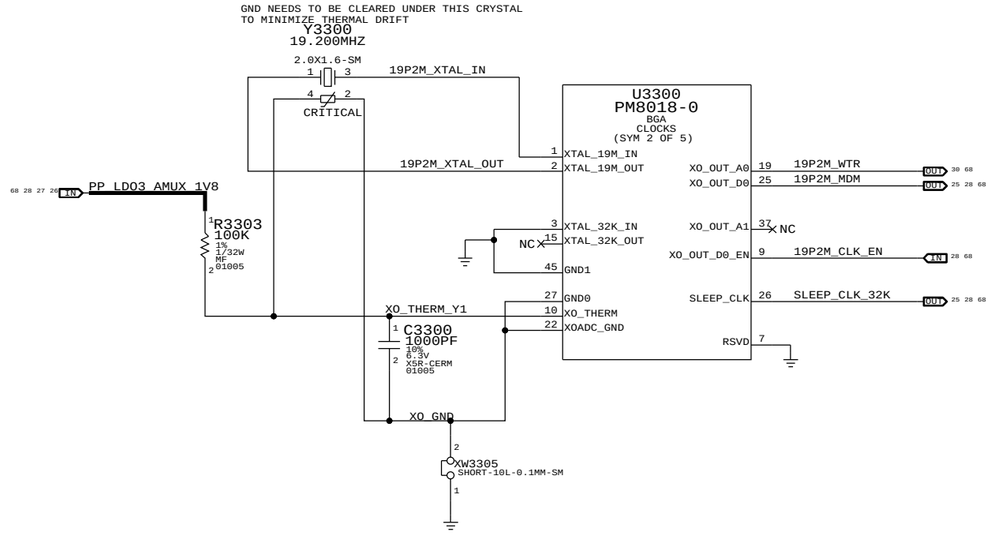
| PA_ID | MAV VER |
|---|---|
| 0.1V | 8.7 |
| 0.3V | 8.6 |
| 0.5V | 8.5 |
| 1.1V | 7.7 |
| 1.3V | 7.6 |
| 1.5V | 7.5 |



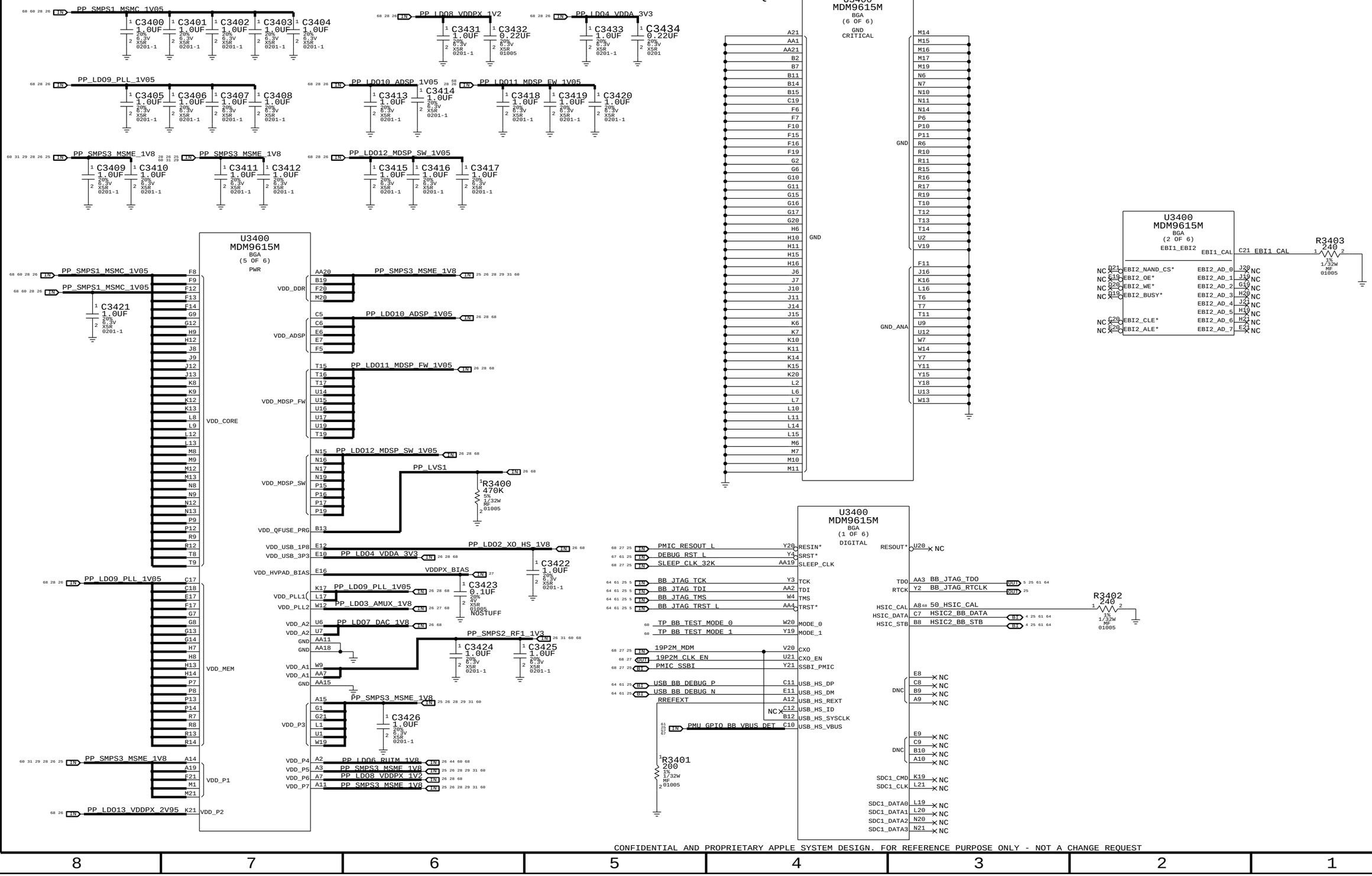

PA THERMISTOR REMOVED TO MATCH N41, AP SECTION
NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.



# BASEBAND (1 OF 2)

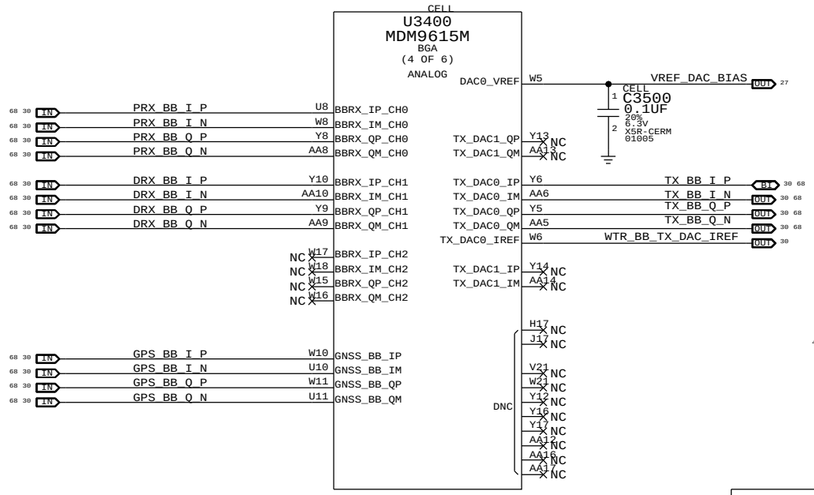
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST



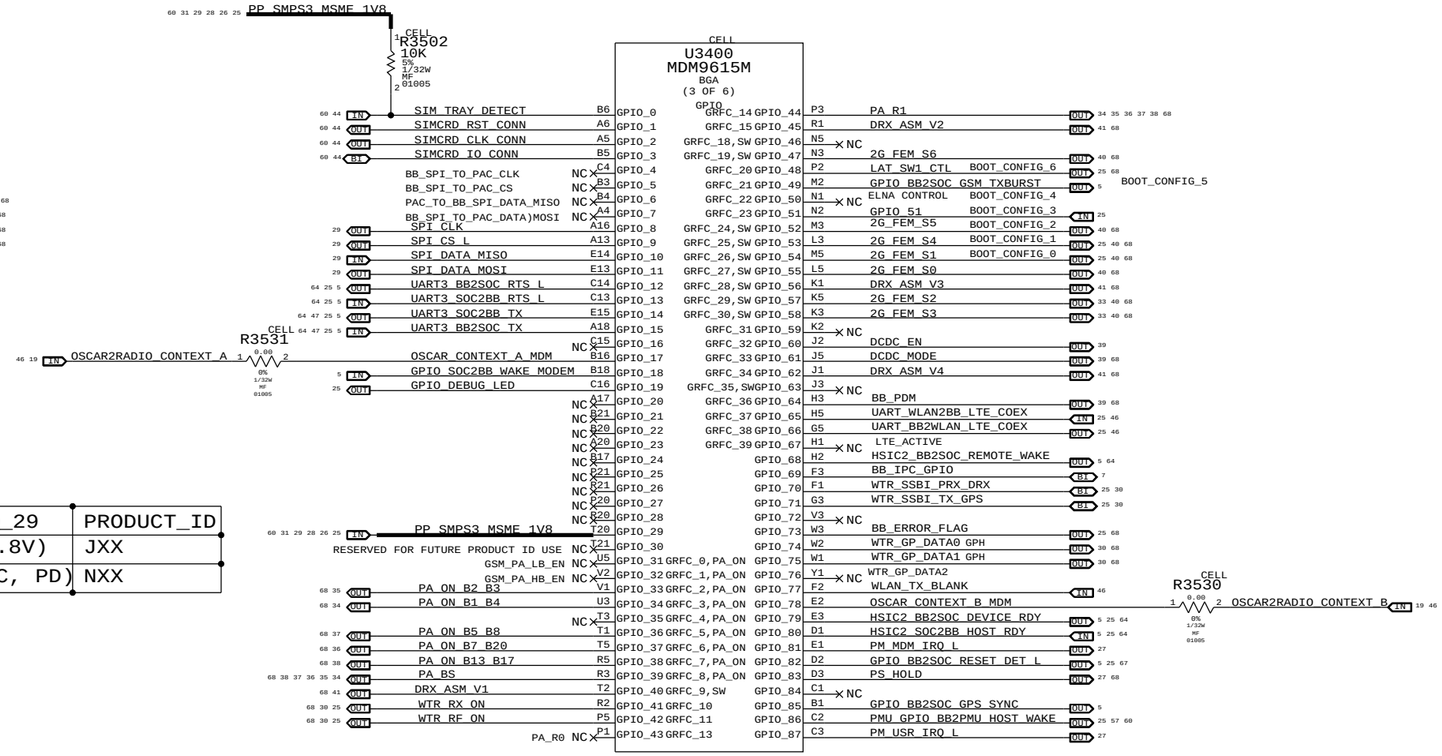

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSE ONLY - NOT A CHANGE REQUEST

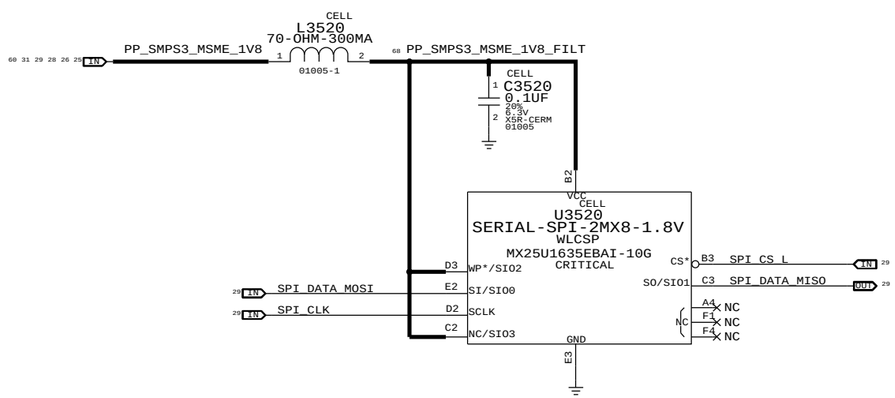
# BASEBAND (2 OF 2)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.




| GPIO_29 | PRODUCT_ID |
|---|---|
| 1 (1.8V) | JXX |
| 0 (NC, PD) | NXX |

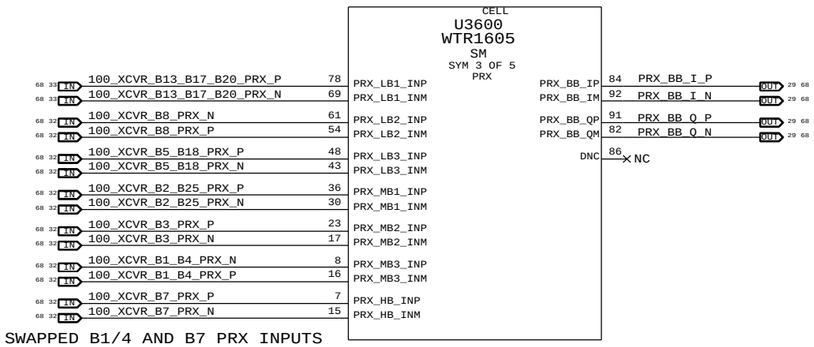


# RF TRANSCEIVER (1 OF 2)

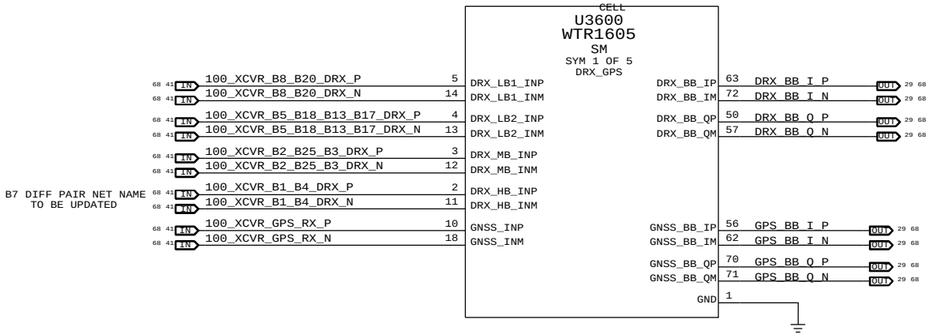
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

## PRX TRANSCEIVER RF AND IQ PORTS

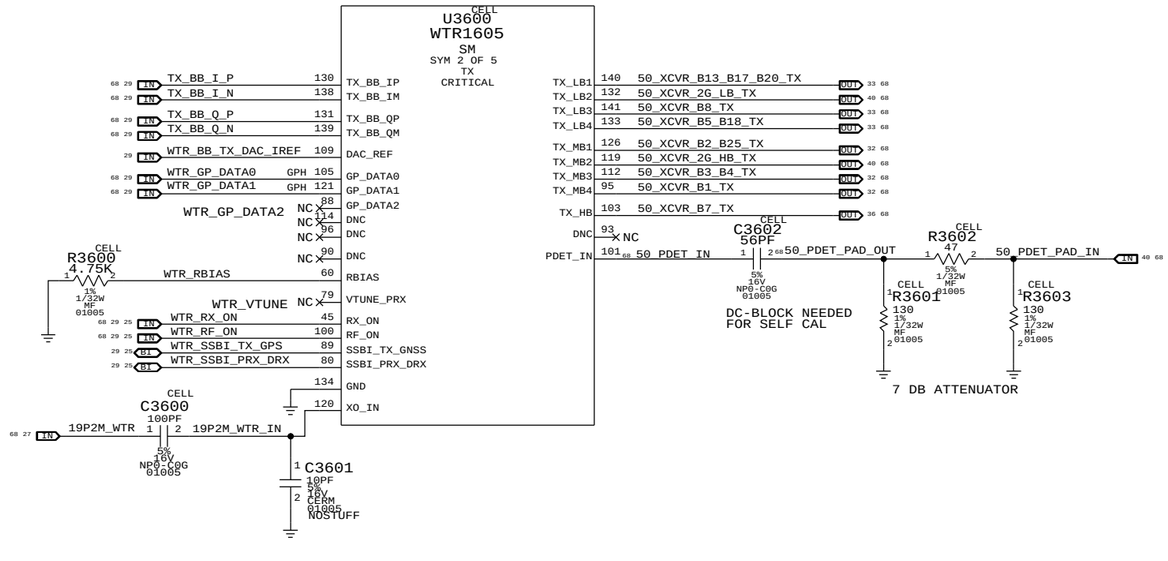



SWAPPED B1/4 AND B7 PRX INPUTS

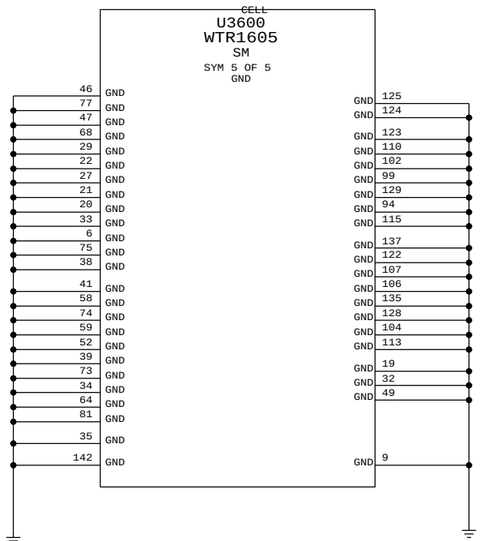
## DRX TRANSCEIVER RF AND IQ PORTS




## TRANSCEIVER PHASE CONTROL, TX RF & IQ PORTS



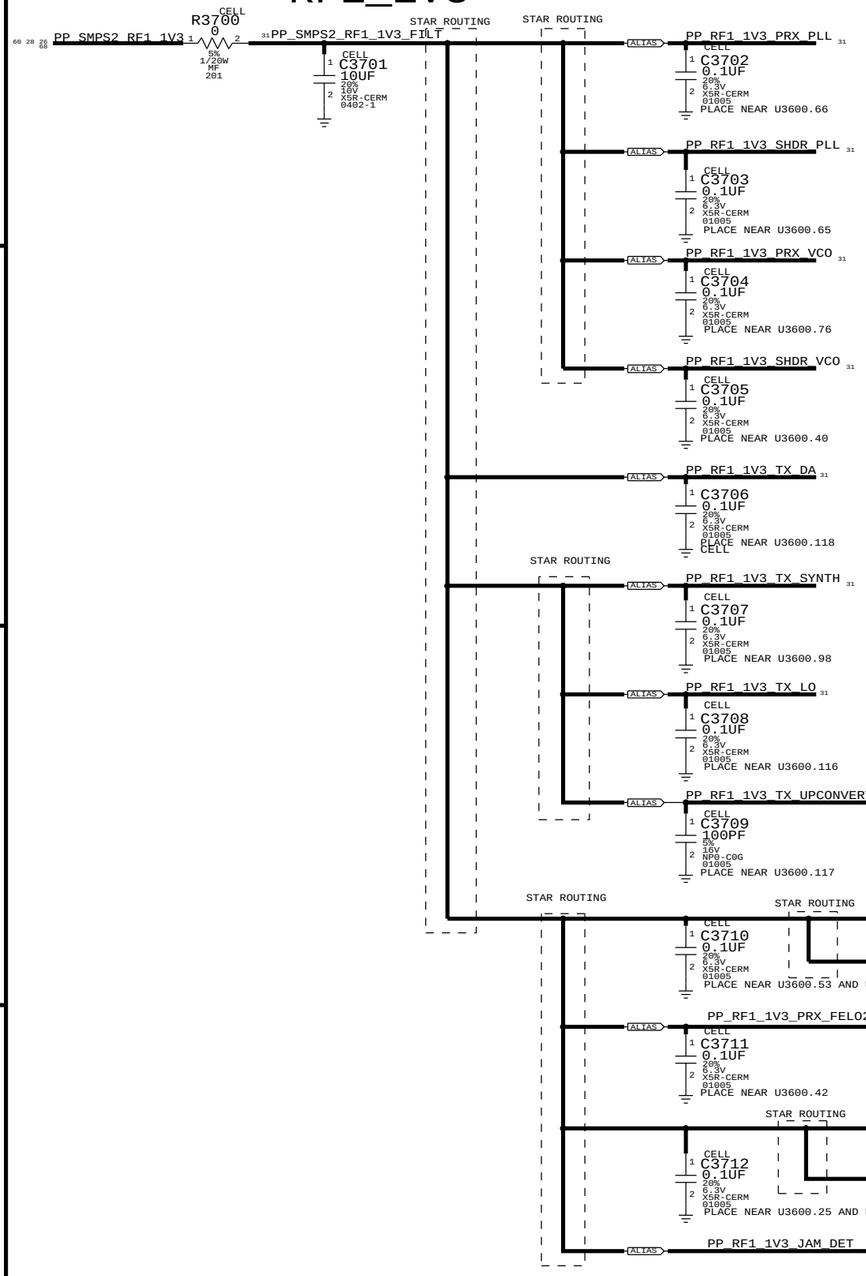

## TRANSCEIVER GROUND CONNECTIONS



# RF TRANSCEIVER (2 OF 2)



## RF1_1V3

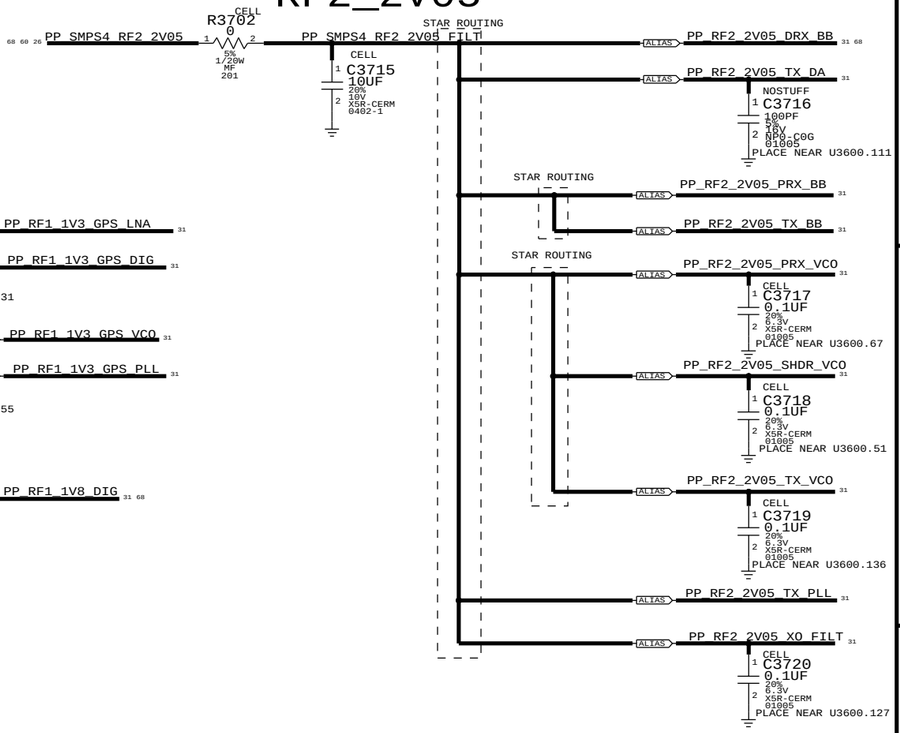



## RF1_1V3

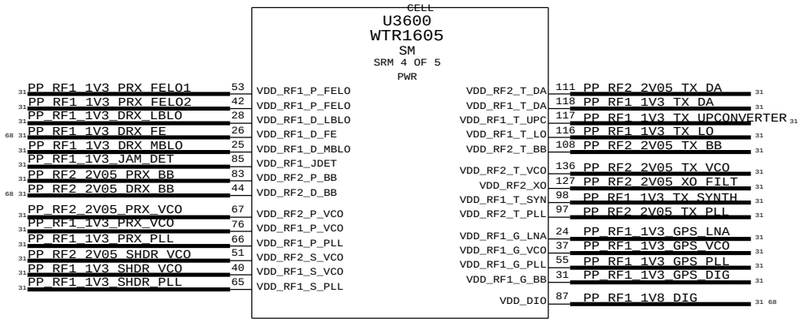

## RF1_1V8




## RF2_2V05

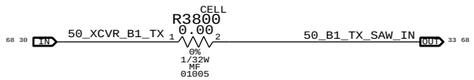


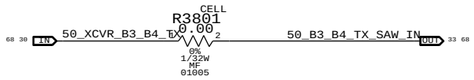

## TRANSCEIVER POWER CONNECTIONS



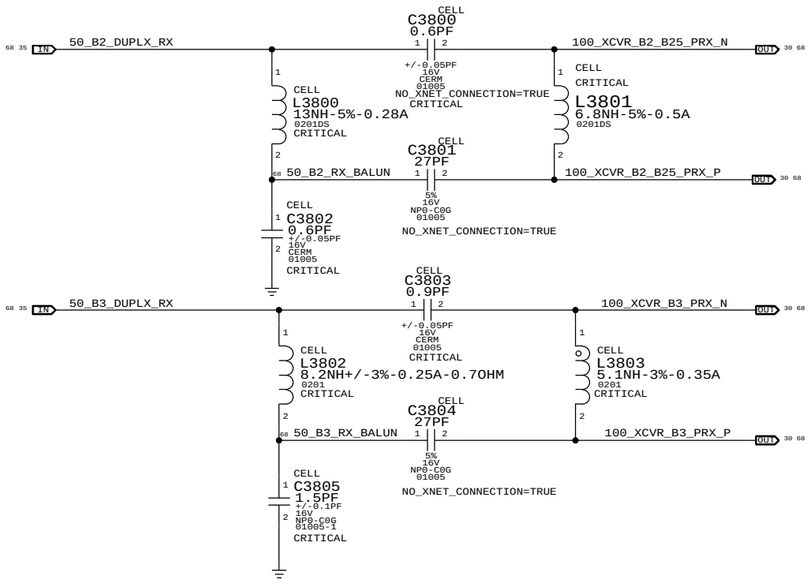
# TRANSCEIVER TX AND RX MATCHING NETWORKS

## TX MATCHING NETWORKS

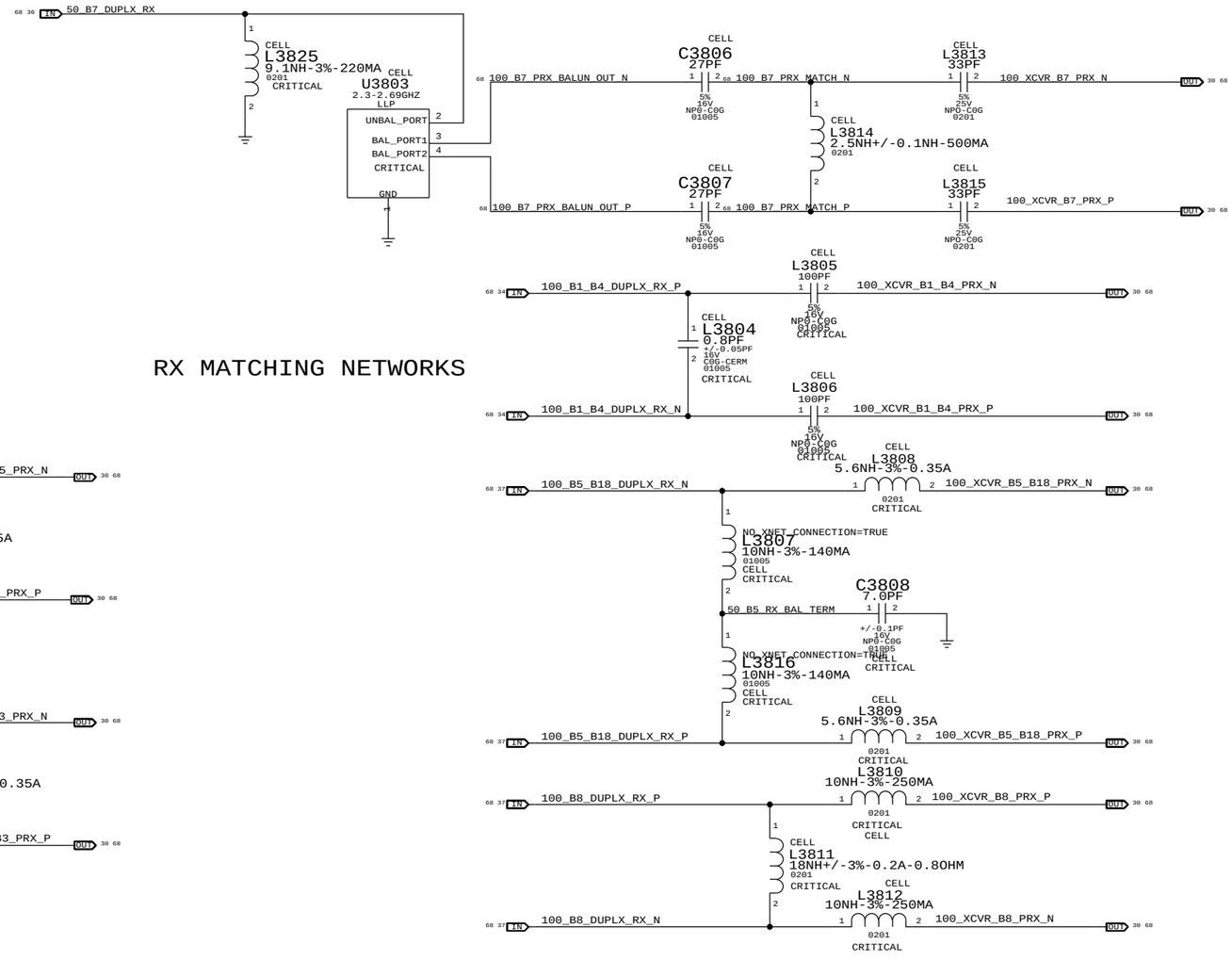






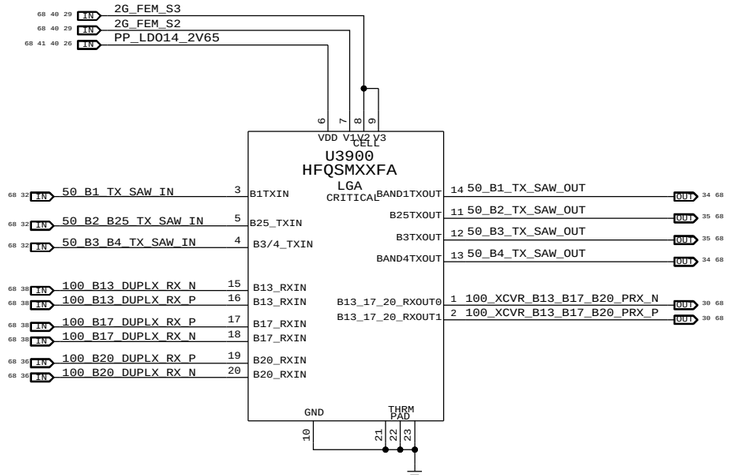

## RX MATCHING NETWORKS



# SAW BANK

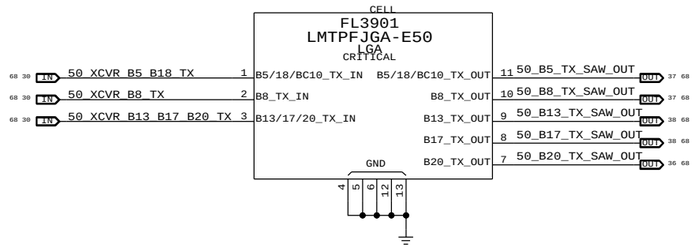
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

## HB TX SAW BANK +
## B13/B17/B20 DP6T SWITCH AND MATCHING



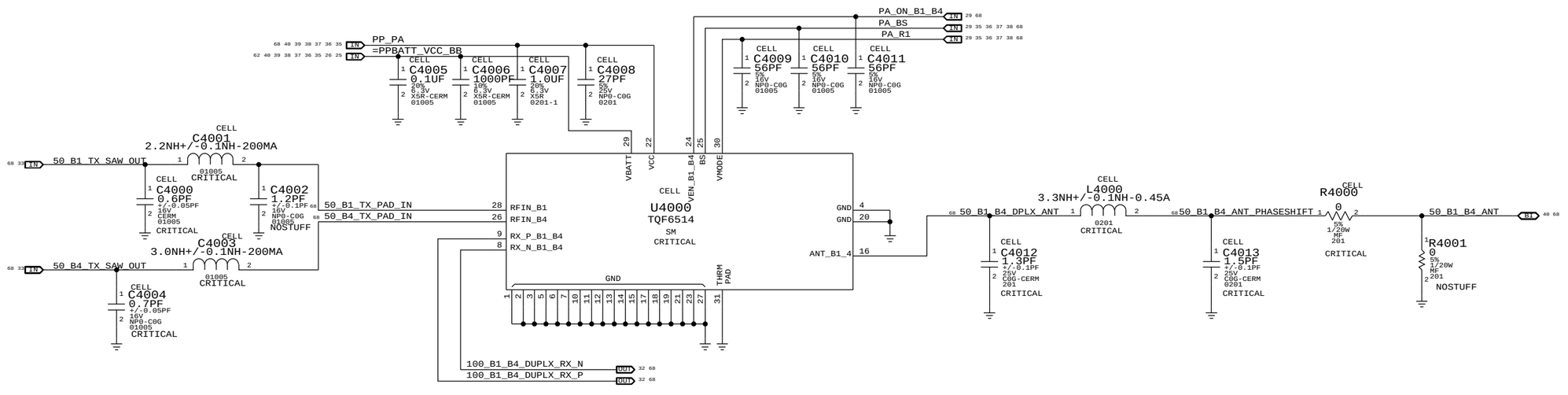

| BAND | V3=V2 | V1 |
|---|---|---|
| B3 TX | HIGH | X |
| B4 TX | LOW | X |
| B13 RX | HIGH | HIGH |
| B17 RX | HIGH | LOW |
| B20 RX | LOW | HIGH |

## LB TX SAW BANK



# BAND 1/4 PAD

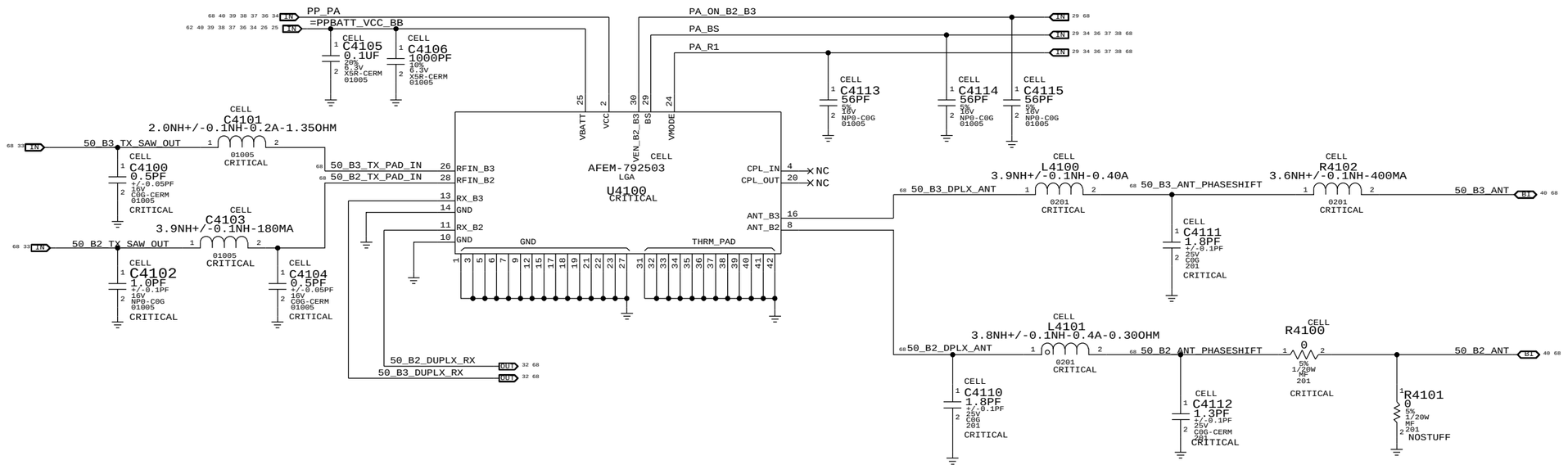
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.




| BAND | PA POWER MODE | PA_BS | PA_ON_B1_B4 | PA_R1 |
|---|---|---|---|---|
| POWER DOWN | X | 0 | 0 | 0 |
| STANDBY | X | X | 0 | X |
| B4 | HPM | 0 | 1 | 0 |
| B4 | LPM | 0 | 1 | 1 |
| B1 | HPM | 1 | 1 | 0 |
| B1 | LPM | 1 | 1 | 1 |

# BAND 2/3 PAD

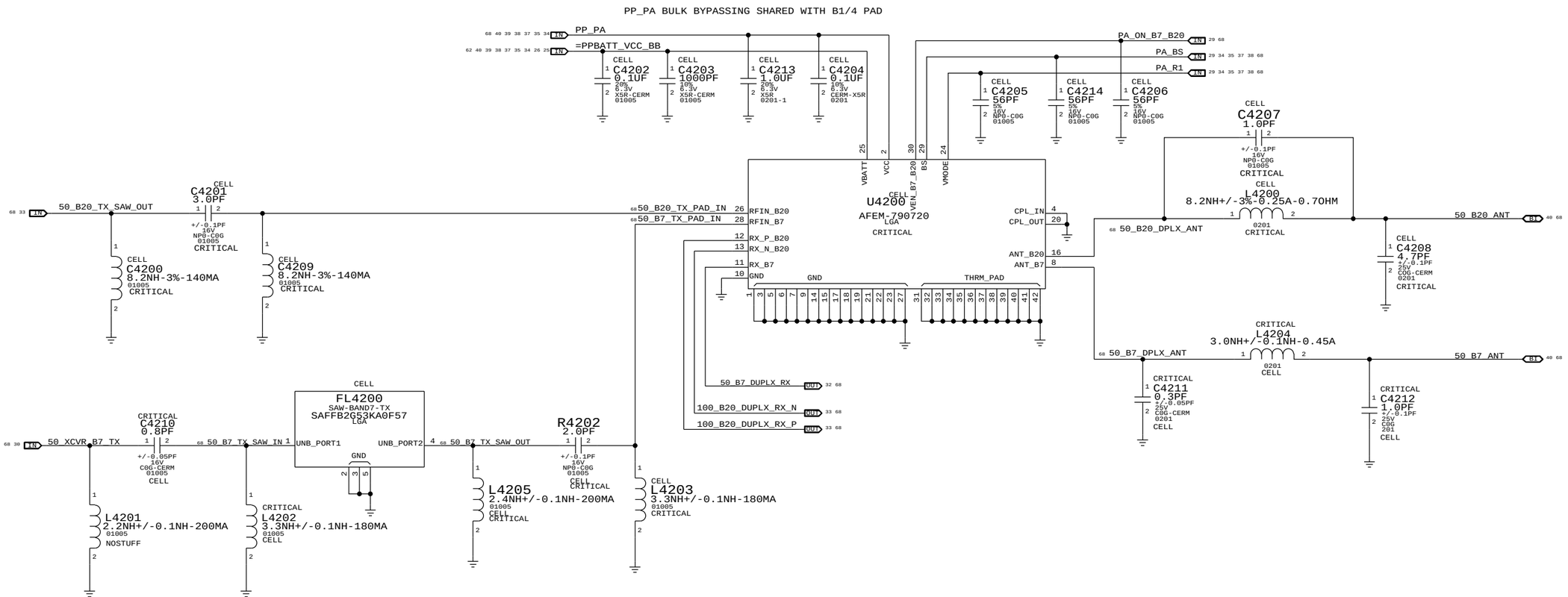





| BAND | PA POWER MODE | PA_BS | PA_ON_B2_B3 | PA_R1 |
|---|---|---|---|---|
| POWER DOWN | X | 0 | 0 | 0 |
| STANDBY | X | X | 0 | X |
| B3 | HPM | 0 | 1 | 0 |
| B3 | LPM | 0 | 1 | 1 |
| B2 | HPM | 1 | 1 | 0 |
| B2 | LPM | 1 | 1 | 1 |

# BAND 20/7 PAD

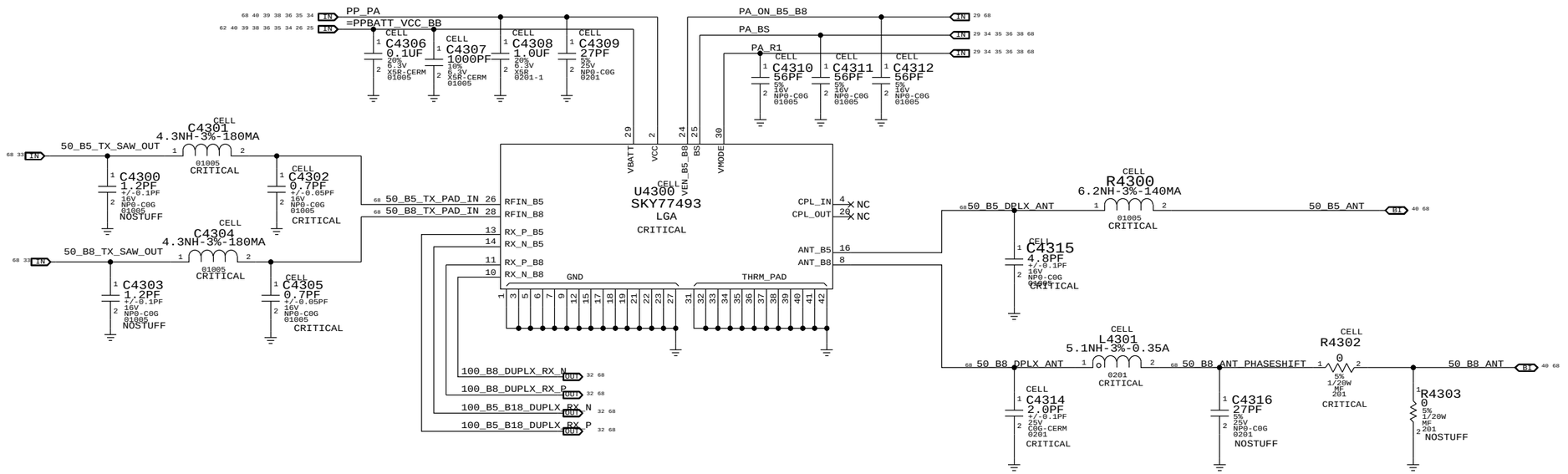
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.




| BAND | PA POWER MODE | PA_ON_B20 | PA_R1 |
|---|---|---|---|
| POWER DOWN | LPM | 0 | 0 |
| STANDBY | X | 0 | X |
| B20 | HPM | 1 | 0 |
| B20 | LPM | 1 | 1 |

# BAND 5/8 PAD

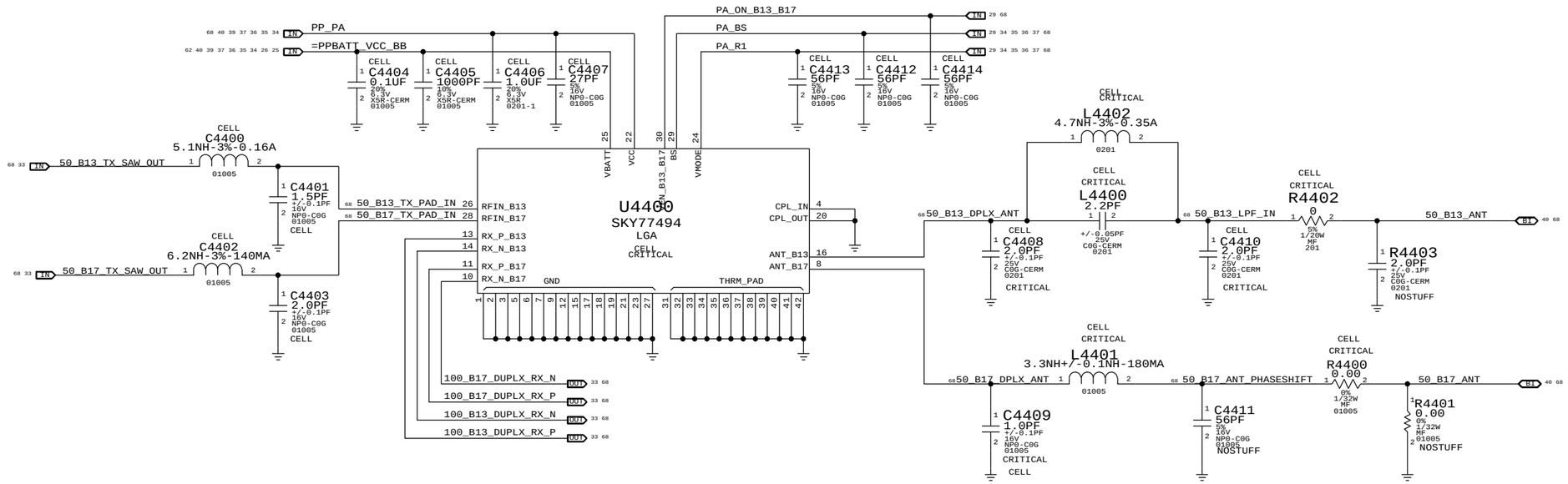
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.




| BAND | PA POWER MODE | PA_BS | PA_ON_B5_B8 | PA_R1 |
|---|---|---|---|---|
| POWER DOWN | X | 0 | 0 | 0 |
| STANDBY | X | X | 0 | X |
| B5 | HPM | 0 | 1 | 0 |
| B5 | LPM | 0 | 1 | 1 |
| B8 | HPM | 1 | 1 | 0 |
| B8 | LPM | 1 | 1 | 1 |

# BAND 13/17 PAD

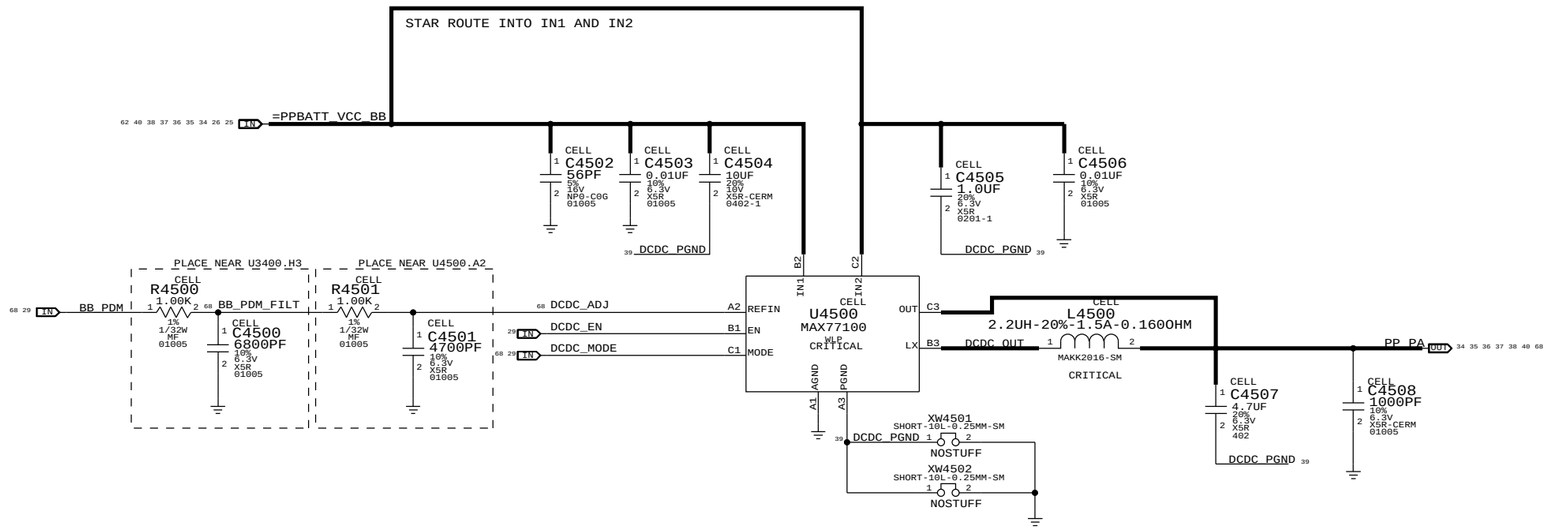





| BAND | PA POWER MODE | PA_BS | PA_ON_B13_B17 | PA_R1 |
|---|---|---|---|---|
| POWER DOWN | X | 0 | 0 | 0 |
| STANDBY | X | X | 0 | X |
| B17 | HPM | 0 | 1 | 0 |
| B17 | LPM | 0 | 1 | 1 |
| B13 | HPM | 1 | 1 | 0 |
| B13 | LPM | 1 | 1 | 1 |

# PA DC/DC CONVERTER

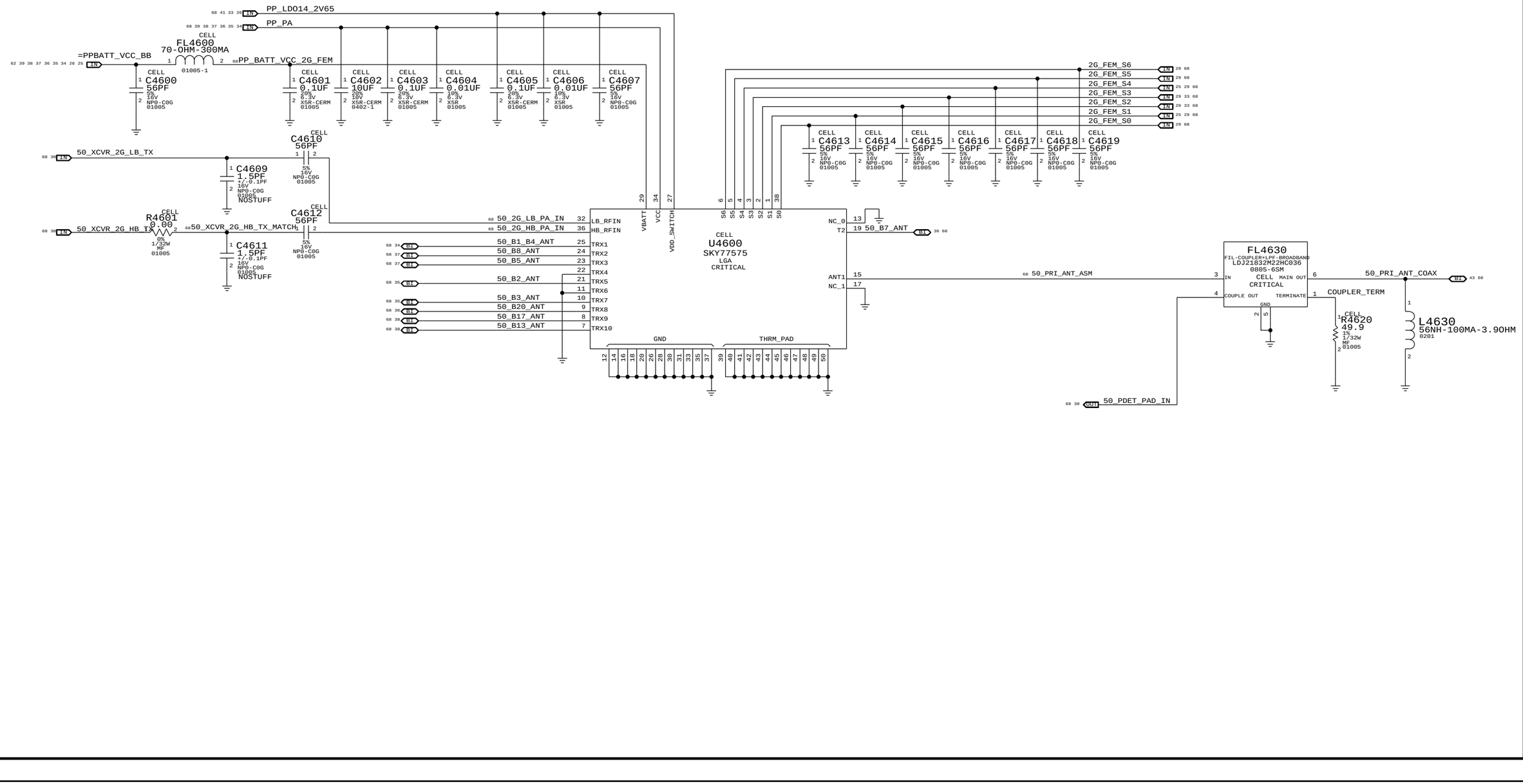
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



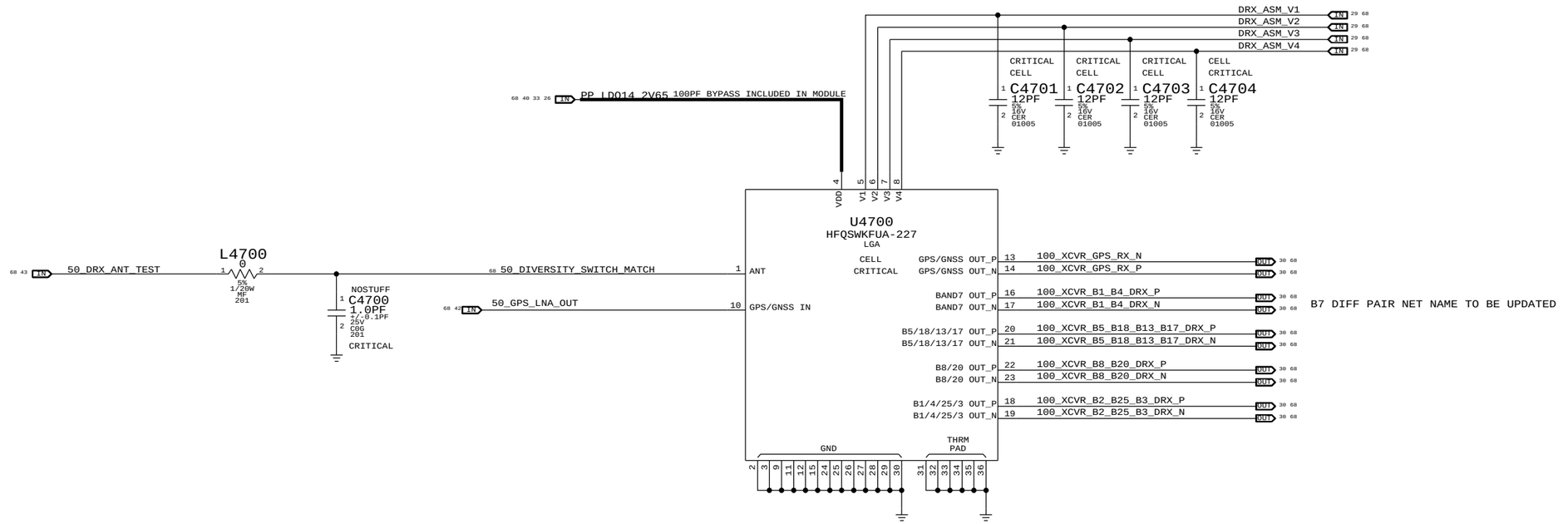
# 2G FEM

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

## 2G FEM



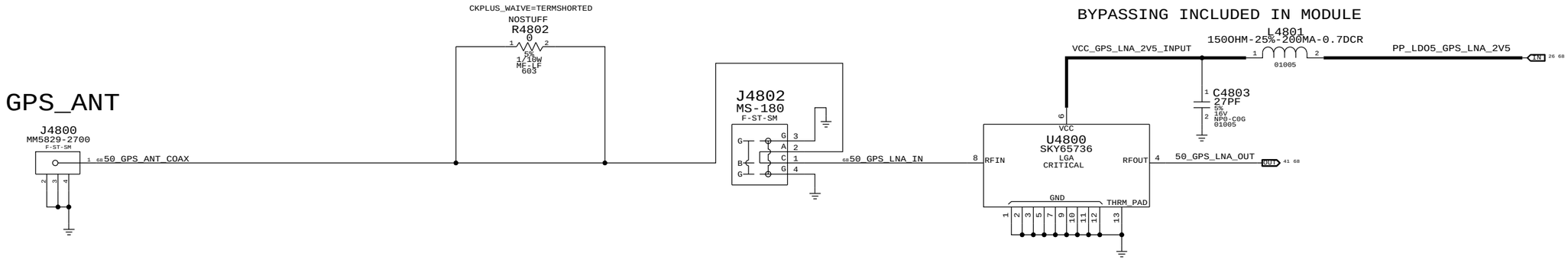
# RX DIVERSITY




## NEED TO UPDATE

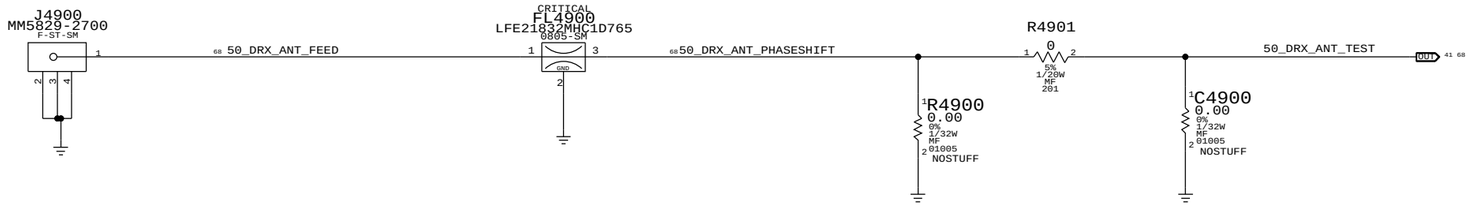
| BAND | DRX_ASM_V4 | DRX_ASM_V3 | DRX_ASM_V2 | DRX_ASM_V1 |
|---|---|---|---|---|
| B1/B4 | LOW | LOW | LOW | LOW |
| B2/25 | LOW | HIGH | LOW | LOW |
| B3 | HIGH | LOW | LOW | LOW |
| B5/6/18 | LOW | LOW | HIGH | LOW |
| B8 | LOW | LOW | LOW | HIGH |
| B13/17 | LOW | HIGH | HIGH | HIGH |
| B20 | LOW | HIGH | HIGH | LOW |
| OFF | LOW | LOW | HIGH | HIGH |
| SWITCH IS TERMINATED IN ALL OTHER POSSIBLE STATES | | | | |

# GPS

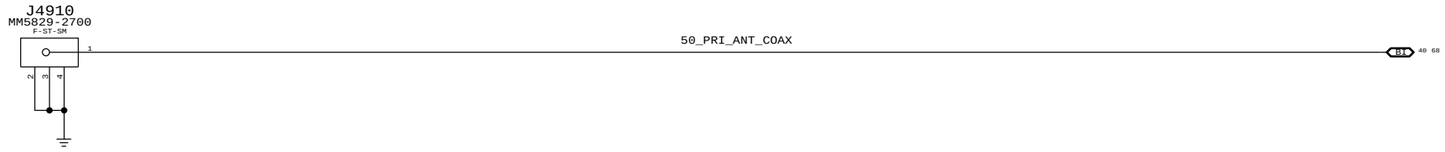


# ANTENNA FEEDS

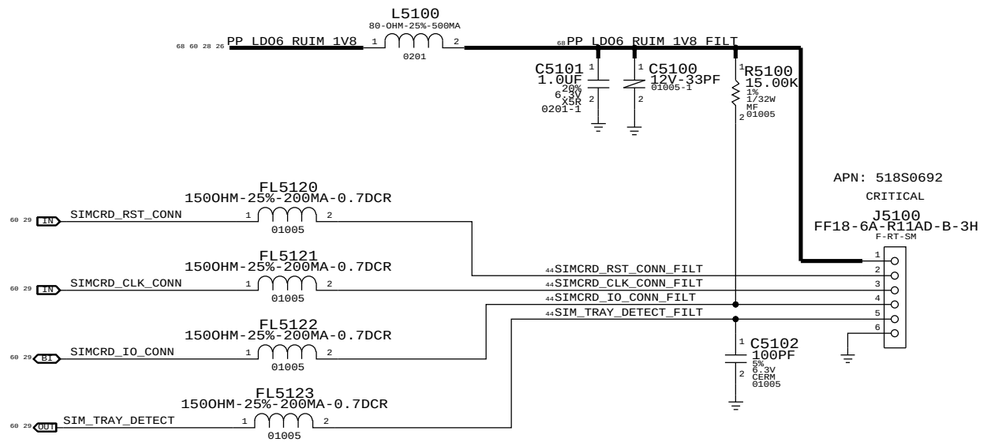
## DRX_ANT COAX



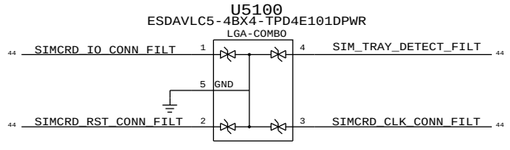

## PRI_ANT COAX



## SIM CARD FLEX CONN

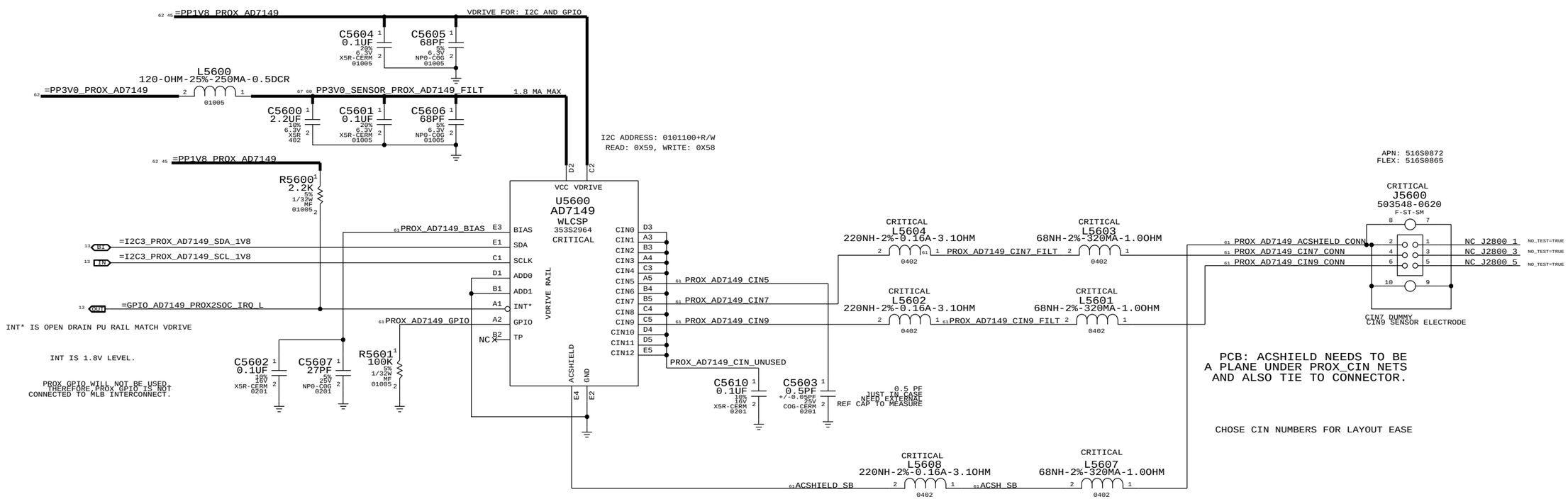



## SIM CARD ESD PROTECTION




| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 377S0130 | 377S0159 | ? | U5100 | RDAR://PROBLEM/12840016 |

# PROX SENSOR




PCB: ENSURE ACSHIELD PLANE UNDER
U3200, NO GND PLANE NEAR PROX_CIN NETS..

# WIFI/BT: MODULE

MODULE ISOLATION

XW5890 SHORT-10L-0.25MM-SM: PMU_GPIO_WLAN_REG_ON (61 57 IN) → PMU_GPIO_WLAN_REG_ON_R (46 60)
XW5891 SHORT-10L-0.25MM-SM: PMU_GPIO_BT_REG_ON (61 57 IN) → PMU_GPIO_BT_REG_ON_R (46 60)
XW5892 SHORT-10L-0.25MM-SM: PMU_GPIO_CLK_32K_WLAN (64 57 IN) → PMU_GPIO_CLK_32K_WLAN_R (46 60)
XW5893 SHORT-10L-0.25MM-SM: UART_WLAN2BB_LTE_COEX (29 25 OUT) → UART_WLAN2BB_LTE_COEX_R (46 61)
XW5894 SHORT-10L-0.25MM-SM: UART_BB2WLAN_LTE_COEX (29 25 IN) → UART_BB2WLAN_LTE_COEX_R (46 61)
XW5895 SHORT-10L-0.25MM-SM: UART2_WLAN2SOC_TX (64 5 OUT) → UART2_WLAN2SOC_TX_R (46 61 64)
XW5896 SHORT-10L-0.25MM-SM: UART2_SOC2WLAN_TX (64 5 IN) → UART2_SOC2WLAN_TX_R (46 61 64)
XW5897 SHORT-10L-0.25MM-SM: HSIC1_SOC2WLAN_HOST_RDY (64 5 IN) → HSIC1_SOC2WLAN_HOST_RDY_R (46 61 64)

CRITICAL U5810 2.4-5.0GHZ SM
LOW(2.4GHZ) 3 ← RF_G_0_DIPLEXER (69)
HIGH(5.0GHZ) 1
ANT(COMMON) 5
GND 6 4 2

CRITICAL R5811 0.00 1% 1/20W MF 0201: RF_G_0_DIPLEXER (69) ↔ RF_G_0_BAW_ANT

CRITICAL U5811 BAW-2436MHZ 885061 LGA: 4 OUT, 5 3 2 GND, 1 IN ← RF_G_0_BAW_MOD

CRITICAL L5811 10NH-3%-250MA 0201: RF_G_0_BAW_ANT ↔ RF_G_0_BAW_MOD
CRITICAL C5811 2.5NH+/-0.1NH-500MA 0201: RF_G_0_BAW_MOD ↔ RF_G_0_MATCH_MOD
CRITICAL L5810 8.2NH+/-3%-0.25A-0.7OHM 0201: RF_G_0_BAW_MOD ↔ RF_G_0_MATCH_MOD
CRITICAL C5810 0.5PF +/-0.05PF 25V C0G-CERM 201: RF_G_0_MATCH_MOD (69) → GND

CRITICAL J5810 MM4829-2702 F-ST-SM: 1 RF_G_ANT (69), 2 3 4 GND
NOSTUFF C5817 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_G_ANT ↔ GND
CRITICAL R5810 0.00 1% 1/20W MF 0201: RF_G_ANT ↔ RF_G_ANT_MATCH_T (69)
NOSTUFF C5816 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_G_ANT_MATCH_T (69) → GND

CRITICAL C5814 1.0NH+/-0.1NH-0.75A 0201: RF_A_0_DIPLEXER (69) ↔ RF_A_0_MATCH (69)
NOSTUFF C5815 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_A_0_DIPLEXER (69) → GND
CRITICAL C5813 0.2PF +/-0.05PF 25V C0G-CERM 0201: RF_A_0_MATCH (69) → GND

CRITICAL J5820 MM4829-2702 F-ST-SM: 1 RF_1_ANT (69), 2 3 4 GND
NOSTUFF C5827 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_1_ANT ↔ GND
CRITICAL R5820 0.00 1% 1/20W MF 0201: RF_1_ANT ↔ RF_1_ANT_MATCH_T (69)
NOSTUFF C5826 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_1_ANT_MATCH_T (69) → GND

CRITICAL U5820 DPX205850DT-9038A1SJ SM: 5 COM, 1 HI, 3 LO, 6 4 2 GND

CRITICAL C5821 0.00 1% 1/20W MF 0201: RF_G_1_DIPLEXER (69) ↔ RF_G_1_MATCH_MOD (69)
NOSTUFF C5822 0.2PF +/-0.1PF 25V C0G-CERM 201: RF_G_1_DIPLEXER (69) → GND
CRITICAL C5820 1.0PF +/-0.05PF 25V C0G-CERM 0201: RF_G_1_MATCH_MOD (69) → GND

CRITICAL C5824 0.8NH-+/-0.1NH-0.8MA 0201: RF_A_1_DIPLEXER (69) ↔ RF_A_1_MATCH (69)
CRITICAL C5825 0.2PF +/-0.05PF 25V C0G-CERM 0201: RF_A_1_DIPLEXER (69) → GND
NOSTUFF C5823 0.2PF +/-0.05PF 25V C0G-CERM 0201: RF_A_1_MATCH (69) → GND

62 =PPVCC_MAIN_WLAN
C5880 10UF 20% 6.3V CERM-X5R 0402-2
C5881 10UF 20% 6.3V CERM-X5R 0402-2
C5882 10UF 20% 6.3V CERM-X5R 0402-2
=PP3V3_S2R_WIFI_PA (61 62)
C5800 4.7UF 20% 6.3V X5R-CERM1 402
C5801 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL U5800 WIFI-BT-DOPPELBOCK LGA

| | | | |
|---|---|---|---|
| | | 16 | VBAT |
| | | 17 | VBAT |
| | | 70 | RF_VCC_FEM |
| | | 71 | RF_VCC_FEM |
| 60 46 PMU_GPIO_CLK_32K_WLAN_R | 33 | | CLK_32K |
| 60 46 PMU_GPIO_WLAN_REG_ON_R | 4 | | WL_REG_ON |
| 60 46 PMU_GPIO_BT_REG_ON_R | 3 | | BT_REG_ON |
| 61 JTAG_WLAN_SEL | 23 | | JTAG_SEL |
| R5800 10K 5% 1/32W MF 01005: 1 ← JTAG_WLAN_SEL, 2 → GND | | | |
| 64 61 4 BI HSIC1_WLAN_DATA | 13 | | HSIC_DATA |
| 64 61 4 BI HSIC1_WLAN_STB | 14 | | HSIC_STROBE |
| NC | 7 | | SDIO_CLK |
| NC | 6 | | SDIO_CMD |
| NC | 8 | | SDIO_DATA0 |
| NC | 9 | | SDIO_DATA1 |
| NC | 10 | | SDIO_DATA2 |
| NC | 11 | | SDIO_DATA3 |
| NC | 77 | | RF_SW_CTRL11 |
| NC | 47 | | I2SWS |
| NC | 36 | | I2SDO |
| NC | 48 | | I2SDI |
| NC | 39 | | I2SCLK |
| | 67 | | RF_A_0 |
| | 79 | | RF_A_1 |
| | 62 | | RF_G_0 |
| | 74 | | RF_G_1 |
| | | BT_GPIO5/LTE_COEX_UART_TX | 51 UART_WLAN2BB_LTE_COEX_R (46 61) |
| | | BT_GPIO4/LTE_COEX_UART_RX | 50 UART_BB2WLAN_LTE_COEX_R (46 61) |
| | | BT_GPIO1/HOSTWAKE | 55 PMU_GPIO_BT_HOST_WAKE (OUT 57) |
| | | BT_GPIO0/BTWAKE | 56 GPIO_BT_WAKE (IN 5 61) |
| | | BT_UART_RXD | 37 UART1_SOC2BT_TX (IN 5 64) |
| | | BT_UART_TXD | 38 UART1_BT2SOC_TX (OUT 5 64) |
| | | BT_UART_RTS* | 36 UART1_BT2SOC_RTS_L (OUT 5 64) |
| | | BT_UART_CTS* | 39 UART1_SOC2BT_RTS_L (IN 5 64) |
| | | BT_PCM_CLK | 41 I2S4_SOC2BT_BCLK (IN 5 64) |
| | | BT_PCM_SYNC | 42 I2S4_SOC2BT_LRCK (IN 5 64) |
| | | BT_PCM_OUT | 43 I2S4_BT2SOC_DATA (OUT 5 64) |
| | | BT_PCM_IN | 44 I2S4_SOC2BT_DATA (IN 5 64) |
| | | GPIO0/WL_HOST_WAKE | 22 PMU_GPIO_WLAN_HOST_WAKE (OUT 57) |
| | | GPIO1/HOST_READY | 20 HSIC1_SOC2WLAN_HOST_RDY_R (46 61 64) |
| | | GPIO2/WL_TCK | 27 TP_JTAG_WLAN_TCK (61 64) |
| | | GPIO3/WL_TMS | 28 JTAG_WLAN_TMS_TX_BLANK (64 61) |
| | | GPIO4/WL_TDI | 26 JTAG_WLAN_TDI_OSCAR_A (64 61) |
| | | GPIO5/WL_TDO | 24 JTAG_WLAN_TDO_OSCAR_B (64 61) |
| | | GPIO12/WL_TRST* | 25 TP_JTAG_WLAN_TRST_L (61 64) |
| | | GPIO9/AGG_CHANNEL | 19 NC |
| | | GPIO10/HSIC_DEVICE_READY | 1 HSIC1_WLAN2SOC_DEVICE_RDY (OUT 5 61 64) |
| | | GPIO11/HSIC_RESUME | 2 HSIC1_WLAN2SOC_REMOTE_WAKE (OUT 5 61 64) |
| | | GPIO15/WLAN_UART_TX | 52 UART2_WLAN2SOC_TX_R (46 61 64) |
| | | GPIO14/WLAN_UART_RX | 53 UART2_SOC2WLAN_TX_R (46 61 64) |
| | | GPIO6 | 30 NC |
| | | GPIO7 | 29 WLAN_GPIO7 |
| | | GPIO8 | 31 NC |
| | | VIO | 35 =PP1V8_S2R_VDDIO_WLAN_BT (46 62) |
| | | DUMMY | 57 NC |
| | | GND_SIGNAL | 5 12 15 18 21 32 34 40 45 54 58 59 60 61 63 64 65 66 68 69 72 73 75 76 78 80 81 82 83 84 85 86 87 88 |

R5804 0.00 1% 1/32W MF 01005: 1 ← WLAN_TX_BLANK (IN 29)
R5801 0.00 1% 1/32W MF 01005: 1 ← OSCAR2RADIO_CONTEXT_A (IN 19 29)
R5802 0.00 1% 1/32W MF 01005: 1 ← OSCAR2RADIO_CONTEXT_B (IN 19 29)
=PP1V8_S2R_VDDIO_WLAN_BT (46 62)
R5803 10K 5% 1/32W MF 01005: 1 ← =PP1V8_S2R_VDDIO_WLAN_BT, 2 → GND

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 377S0155 | 377S0104 | ? | | RDAR://PROBLEM/12840267 |

DZ6000,DZ6001,DZ6002,DZ6003,DZ6090

=PP3V0_S2R_TRISTAR
C6030 1.0UF 20% 6.3V X5R 0201-1
C6035 0.22UF 20% 6.3V X5R 0201
C6040 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
=PP3V3_ACC
C6042 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
C6032 0.22UF 20% 6.3V X5R 0201
=PP1V8_S2R_TRISTAR
C6031 0.22UF 20% 6.3V X5R 0201
C6041 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
PPVBUS_PROT
C6043 8.2PF +/-0.25PF 25V NP0-C0G 0201
C6034 1UF 10% 25V X5R 0402
C6045 1UF 10% 25V X5R 0402

U6000
CBTL1610A1UK
WLCSP

| | | | |
|---|---|---|---|
| VDD_1V8 | F3 | | |
| VDD_3V0 | F4 | | |
| ACC_PWR | D5 | | |
| DIG_DP | C3 | MIKEY_TS_P | BI |
| DIG_DN | C4 | MIKEY_TS_N | BI |
| USB1_DP | A1 | USB_BB_P | BI |
| USB1_DN | B1 | USB_BB_N | BI |
| BRICK_ID | C2 | PMU_USB_BRICKID | OUT |
| USB0_DP | A3 | USB_SOC_P | BI |
| USB0_DN | B3 | USB_SOC_N | BI |
| UART0_TX | E2 | UART6_TS_ACC_TXD | IN |
| UART0_RX | E1 | UART6_TS_ACC_RXD | OUT |
| UART1_TX | F2 | UART0_SOC_TXD | IN |
| UART1_RX | F1 | UART0_SOC_RXD | OUT |
| UART2_TX | D2 | UART3_BB2SOC_TX | IN |
| UART2_RX | D1 | UART3_SOC2BB_TX | OUT |
| JTAG_CLK | A5 | JTAG_SOC_TCK_R | |
| JTAG_DIO | B5 | JTAG_SOC_TMS_R | |
| P_IN | F6 | | |
| ACC1 | C5 | PPOUT_E75_ACC_ID1 | |
| ACC2 | E5 | PPOUT_E75_ACC_ID2 | |
| DP1 | A2 | E75_DPAIR1_P | |
| DN1 | B2 | E75_DPAIR1_N | |
| DP2 | A4 | E75_DPAIR2_P | |
| DN2 | B4 | E75_DPAIR2_N | |
| CON_DET_L | E3 | TS_E75_ACC_DET_L | |
| POW_GATE_EN* | D6 | OVP_SW_EN_L | OUT |
| SWITCH_EN | E4 | RESET_SOC_L | IN |
| HOST_RESET | B6 | TS2PMU_RESET_IN | OUT |
| SDA | D3 | I2C2_SDA_1V8 | OUT |
| SCL | D4 | I2C2_SCL_1V8 | IN |
| INT | C6 | GPIO_TS2SOC2PMU_INT | OUT |
| BYPASS | E6 | BYPASS_U5900 | |
| DVSS | F5 | | |
| DVSS | C1 | | |
| DVSS | A6 | | |

TO BB USB
ACCESSORY USB
ACCESSORY UART
AP DEBUG UART
BB DEBUG UART
(T'S OFF TO SOC UART3)

R6030 0.00 0% 1/32W MF 01005
R6031 0.00 0% 1/32W MF 01005
C6033 1.0UF 20% 6.3V X5R 0201-1

TRISTAR 2:
AS OF 10/11/12 STILL PLAN TO STUFF CAP EVEN WITH TRISTAR2
RDAR://PROBLEM/12580126

XW6000
SHORT-10L-0.25MM-SM
L81_MBUS_REF
PLACE_NEAR=U6000.F5:5MM

TRISTAR 2:
FOR PULSED CON_DET_L SUPPORT
NOSTUFF R6080, STUFF R6081

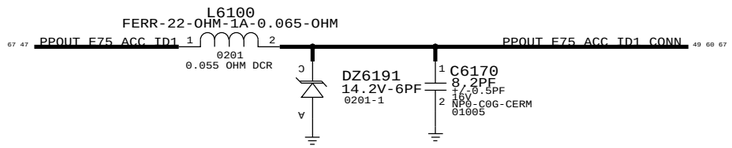
NOSTUFF R6080 0.00 0% 1/32W MF 01005
PMU_E75_ACC_DET_L
R6081 0.00 0% 1/32W MF 01005

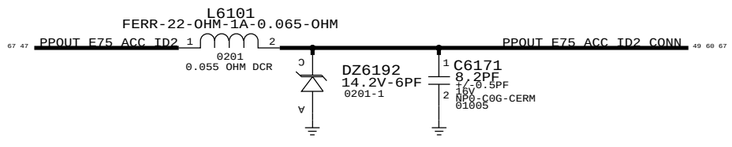
CRITICAL L6030 90-OHM-50MA TCM0605-1
CRITICAL L6031 90-OHM-50MA TCM0605-1
E75_DPAIR1_CONN_P
E75_DPAIR1_CONN_N
E75_DPAIR2_CONN_P
E75_DPAIR2_CONN_N

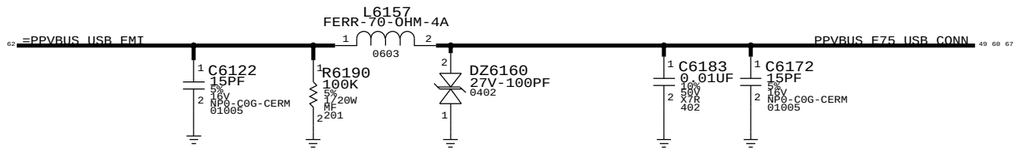
CRITICAL DZ6000 ESD0P2RF-02LS TSSLP-2-1 0.4PF
CRITICAL DZ6001 ESD0P2RF-02LS TSSLP-2-1 0.4PF
CRITICAL DZ6002 ESD0P2RF-02LS TSSLP-2-1 0.4PF
CRITICAL DZ6003 ESD0P2RF-02LS TSSLP-2-1 0.4PF

PPVCC_MAIN
NOSTUFF R6091 100K 5% 1/32W MF 01005
C6091 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005

R6090 10K 5% 1/32W MF 01005
E75_ACC_DET_R_L
FL6090 120-OHM-25%-250MA-0.5DCR 01005
E75_ACC_DET_CONN_L
NOSTUFF C6090 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
CRITICAL D6090 SM-201 DSF01S30SC
CRITICAL DZ6090 ESD0P2RF-02LS TSSLP-2-1



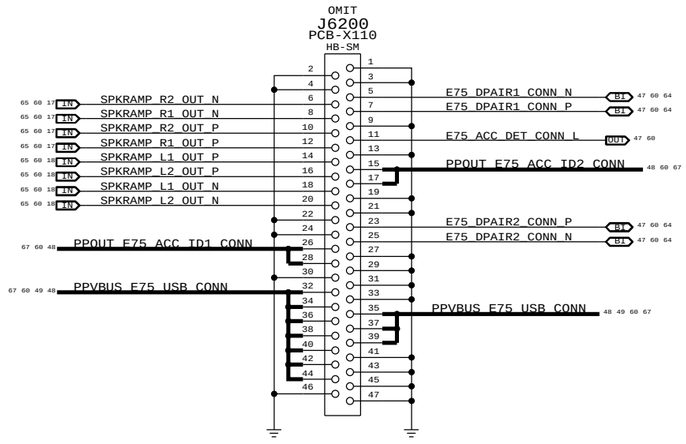




| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 377S0116 | 377S0108 | | DZ6160 | RDAR:8370432 |
| 155S0320 | 155S0513 | | L6100,L6101 | RDAR://PROBLEM/9625601 |
| 155S0741 | 155S0397 | | L6157 | RDAR://PROBLEM/11238851 |

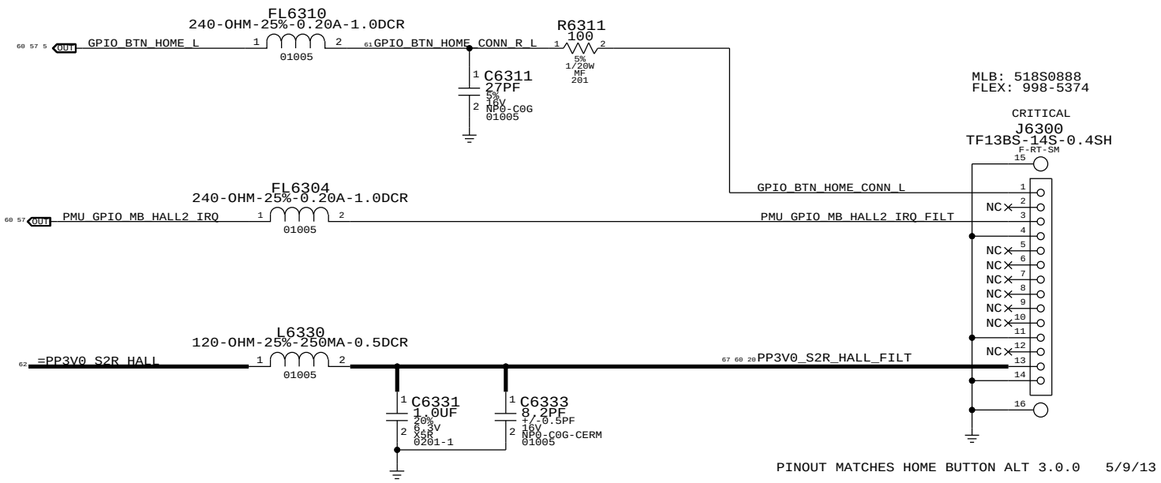
# IO FLEX HOTBAR PADS

MLB 998-5877
FLEX 998-5876

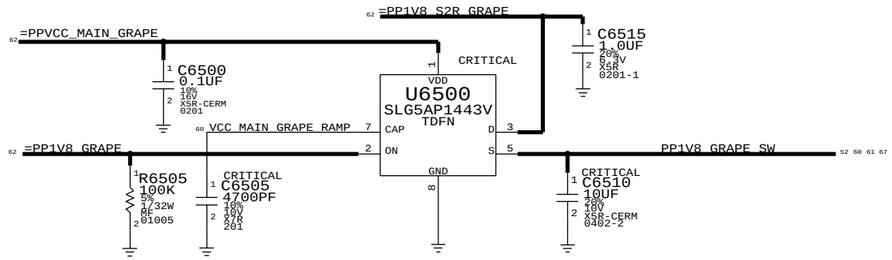



PINOUT MATCHES IO_FLEX 4.2.0  3/12/13

# HOME BUTTON FILTERS



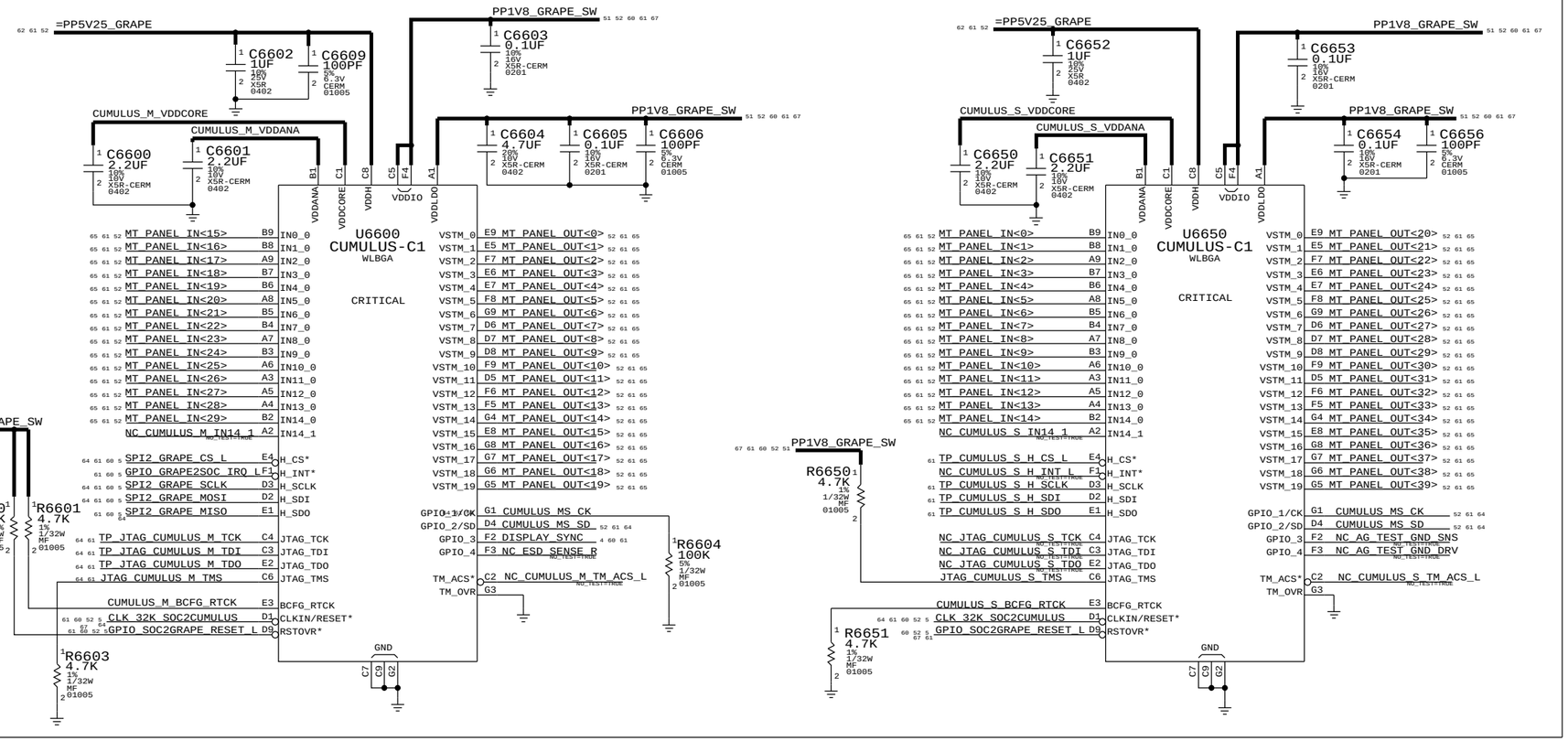
# GRAPE CONNECTOR SUPPORT




LAYOUT NOTE:
PUT THERMAL VIAS AROUND U2300 IN CASE OF SHORTED CONDITION

# CUMULUS C1 (CSP) IN MASTER-SLAVE CONFIG

## MASTER CUMULUS



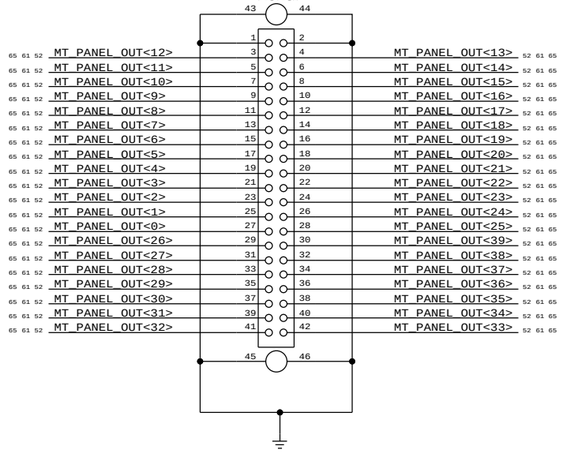

## SLAVE CUMULUS




PINOUT MATCHES GRAPE_FLEX_DRIVE_ALT 0.1.0 1/8/13

CRITICAL

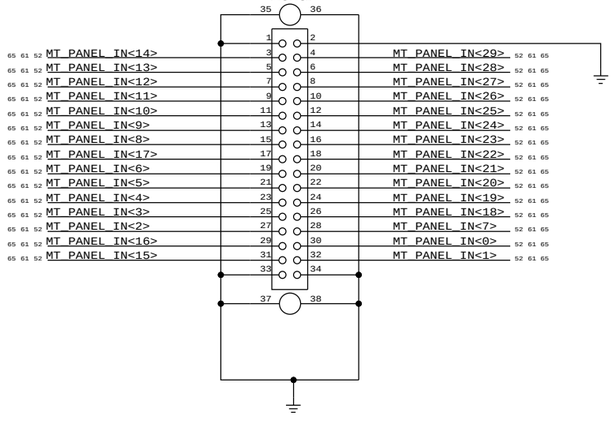
J6620
AA03-S042VA1
F-ST-SM



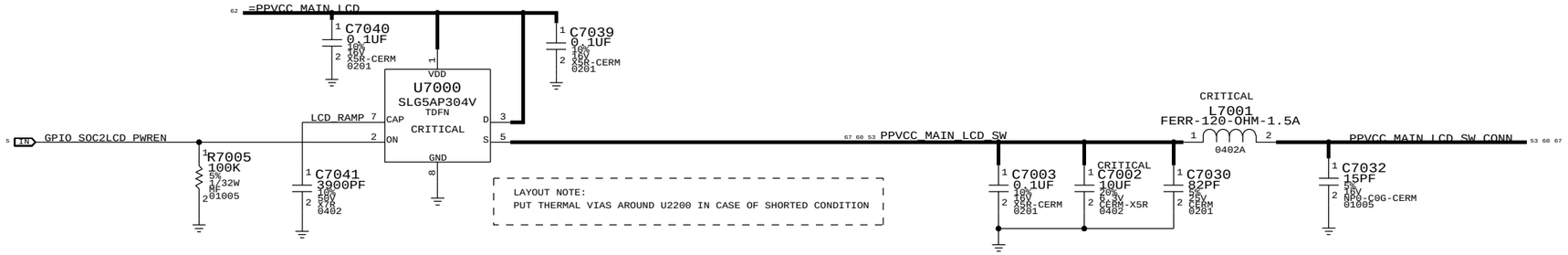

PINOUT MATCHES GRAPE_FLEX_SENSE_ALT 0.1.0 1/8/13

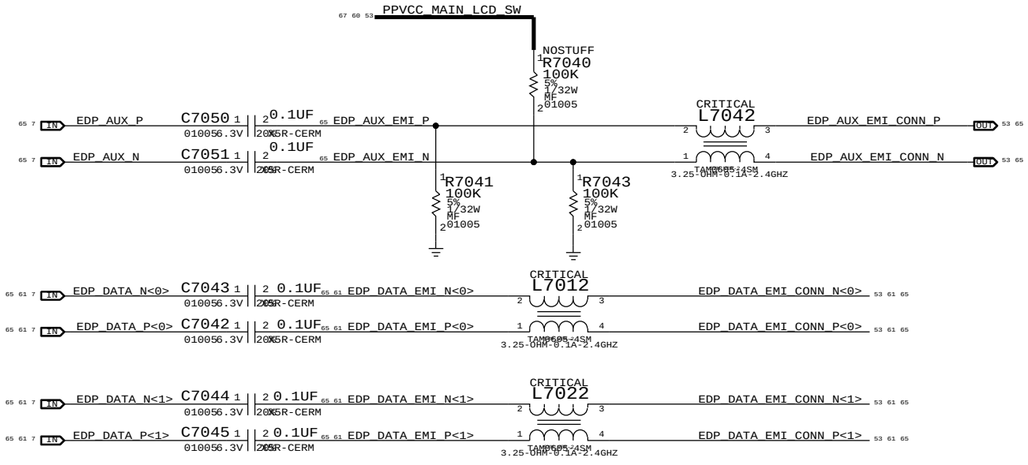
CRITICAL

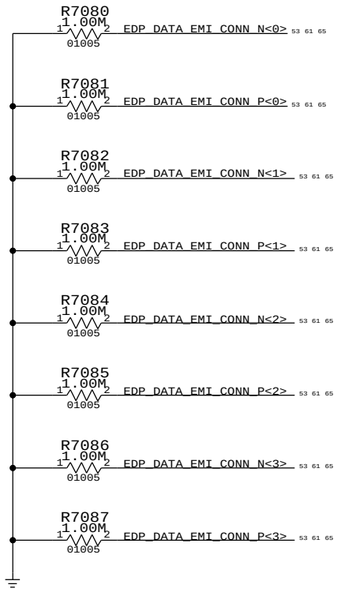
J6640
AA03-S034VA1
F-ST-SM

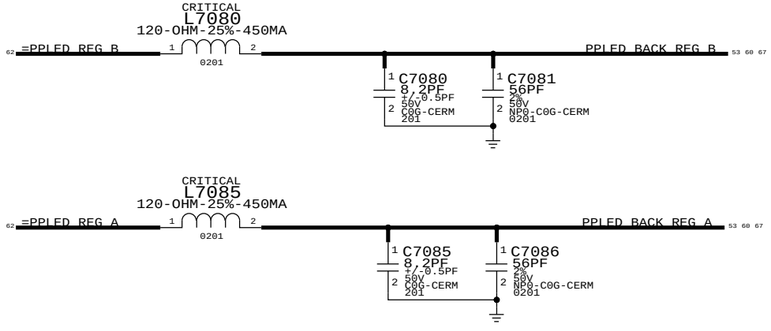


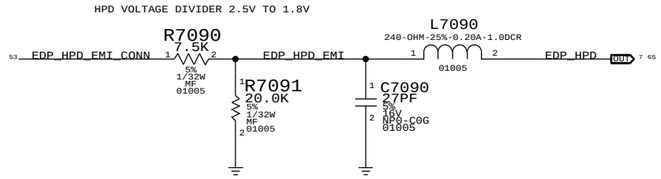
# EDP CONNECTOR SUPPORT



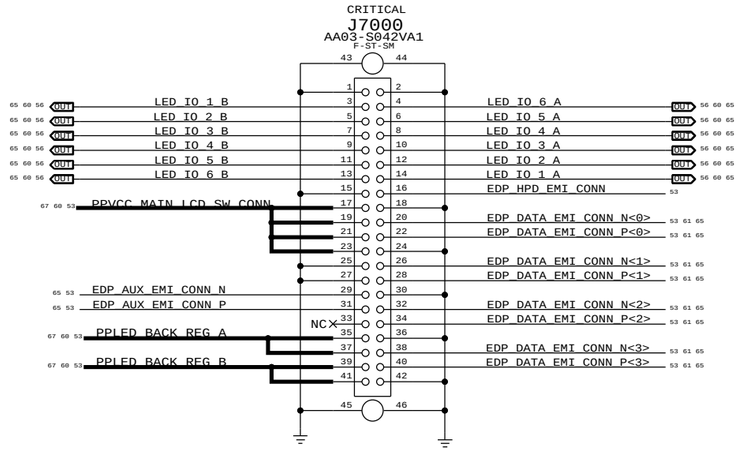



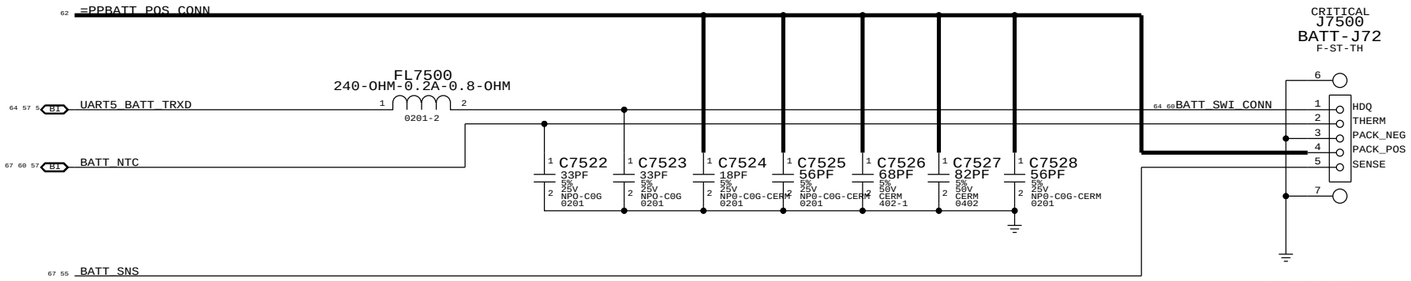

# EDP CONNECTOR

PINOUT MATCHES DISPLAY_EDP_FLEX 1.0.0 1/7/13



| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 155S0644 | 155S0823 | ? | | RDAR://PROBLEM/11282371 |

FL7500,L1920







APN:516-0254

PLACEMENT_NOTE=PLACE NEAR L8225.1

CRITICAL C8140 150UF 20% 6.3V TANT-1 B15G — ESR MAX=70MOHM
CRITICAL C8141 150UF 20% 6.3V TANT-1 B15G — ESR MAX=70MOHM

VCC_MAIN BYPASS
PLACE TWO 10UF CAP
AT EACH VDD INPUT

CRITICAL C8150–C8159 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8160–C8172 10UF 20% 6.3V CERM-X5R 0402

PPVCC_MAIN 47 55 56 57 58 60 62 67
CRITICAL C8144 1.0UF 20% 6.3V CERM 0201-1
C8142 82PF 5% 25V CERM 0201
C8143 18PF 5% 25V NPO,C0G-CERM 0201

CRITICAL L8112 2.2UH-20%-5.6A-0.03OHM PILE101D-SM DCR=30MOHM MAX

67 62 60 58 57 56 55 47 PPVCC_MAIN
55 47 OVP_SW_EN_L — R8170 4.7K 5% 1/20W MF 201

CRITICAL Q8104 FDMC6683 MLP3.3X3.3
RDSON=0.0136@VGS=-2.5V
ID=12.0A

67 62 60 55 PPBATT_VCC

ACT_DIO — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.1 MM, NET_SPACING_TYPE=ANLG

CRITICAL D8100 SOD-123W PMEG4030ER — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.20 MM, NET_SPACING_TYPE=PWR, DIDT=TRUE, SWITCH_NODE=TRUE

67 54 BATT_SNS — R8172 0 5% 1/20W MF 201 — PLACE_NEAR=U8100.R17:2MM
67 BATT_SNS_R — R8173 499 1% 1/20W MF 201 — PLACE_NEAR=U8100.R17:10MM
NOSTUFF C8149 0.022UF 10% 25V X7R 0402 — PLACE_NEAR=U8100.R17:10MM

LAYOUT NOTE -
R8172- PLACE NEAR PMU
R8149- PLACE NEAR PMU
R8173- PLACE NEAR PMU

| MOSFET | FDMC6676BZ |
|---|---|
| CHANNEL | P-TYPE |
| RDS(ON) | 27 MOHM @-4.5V |
| IMAX | 6.9 A |
| VGS MAX | +/- 25V |

67 4 USB_VBUS_DETECT — XW8114 SHORT-0201
MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM, VOLTAGE=6.0V

67 66 PMU_VCENTER
CRITICAL C8148 4.7UF 10% 35V X5R-CERM 0603 — PLACE_NEAR=U8100.F18:2MM
CRITICAL C8147 4.7UF 10% 35V X5R-CERM 0603 — PLACE_NEAR=U8100.L18:2MM
MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM, VOLTAGE=6.0V
LAYOUT NOTE: PLACE RIGHT AT THE PIN

67 60 47 PPVBUS_PROT
MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM, VOLTAGE=6.0V
CRITICAL C8145 2.2UF 10% 25V X5R-CERM 603 — PLACE_NEAR=U8100.G16:10MM
LAYOUT NOTE: PLACE RIGHT AT THE PIN

NOSTUFF R8116 470K 1% 1/20W MF 201
CRITICAL Q8123 FDMC6676BZ MLP3.3X3.3
CRITICAL DZ8120 BZT52C10LP LLP — NOTE: 10V ZENER
VBUS_PROT_G 60 — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.1MM, NET_SPACING_TYPE=ANLG
R8130 220K 1% 1/20W MF 201
67 62 60 PPVBUS_USB_DCIN

USB REVERSE VOLTAGE PROTECTION

R8146 4.7K 5% 1/20W MF 201
55 47 OVP_SW_EN_L — OVP_SW_EN_L_R
NOSTUFF C8146 0.01UF 10% 25V X5R-CERM 0201

LAYOUT NOTE:
R8146, C8146 CAN BE
ANYWHERE BET.TRISTAR
AND PMU

TP_HV_CHG_EN

62 55 =PPVCC_MAIN_CPU
62 55 =PPVCC_MAIN_GPU
62 55 =PPVCC_MAIN_SOC
67 62 60 58 57 56 55 47 PPVCC_MAIN

OMIT_TABLE
U8100 D2089A0 FCBGA SYM 1 OF 4

| | | |
|---|---|---|
| G19 | CHG_LX0 | |
| H19 | CHG_LX1 | |
| J19 | CHG_LX2 | |
| K19 | CHG_LX3 | |
| R17 | VBAT | |
| P17 | IBAT_S | |
| M19 | IBAT0 | |
| N19 | IBAT1 | |
| P19 | IBAT2 | |
| R19 | IBAT3 | |
| N17 | ACT_DIO | |
| F18–L19 | VCENTER | |
| F16–L17 | VBUS | |
| C16 | VBUS_OVP_OFF | |
| D17 | HV_CHG_DIS | |
| F1–K2 | VDD_BUCK0_01 / VDD_BUCK0_23 | |
| P1–V3 | VDD_BUCK1_01 / VDD_BUCK1_2 | |
| U8–V8 | VDD_BUCK2 | |
| A4–B4 | VDD_BUCK3 | |
| A8–B8 | VDD_BUCK4 | |
| U4–V4 | VDD_BUCK5 | |
| B1–B3 | VDD_BUCK6 | |
| T16 | VCC_MAIN_S | |
| M18–R18 | VCC_MAIN | |

USB/BAT BUCK — VCC_MAIN SWITCHED POWER

| | | |
|---|---|---|
| E1 | BUCK0_LX0 | |
| E2 | BUCK0_LX1 | |
| G1 | BUCK0_LX2 | |
| G2 | BUCK0_LX3 | |
| J1 | BUCK0_FB | |
| J2 | BUCK1_LX0 | |
| L1 | BUCK1_LX1 | |
| L2 | BUCK1_LX2 | |
| H6 | BUCK1_FB | |
| N1 | BUCK2_LX0 | |
| N2 | BUCK2_FB | |
| R1 | BUCK3_LX0 | |
| R2 | BUCK3_FB | |
| U1 | BUCK4_LX0 | |
| U2 | BUCK4_FB | |
| M6 | BUCK5_LX0 | |
| U7 | BUCK5_FB | |
| V7 | BUCK6_LX0 | |
| P7 | BUCK6_FB | |
| A5 | BUCK6_BYP0 | |
| B5 | BUCK6_BYP1 | |
| E6 | BUCK6_BYP2 | |
| A7 | VBUCK3 | |
| B7 | BUCK3_SW1 | |
| E7 | BUCK3_SW2 | |
| U5 | BUCK3_SW3 | |
| V5 | VBUCK4 | |
| P6 | BUCK4_SW1 | |
| C1 | BUCK4_SW2 | |
| C2 | VPUMP | |
| F6 | | |
| A1 | | |
| A2 | | |
| A3 | | |
| B13 | | |
| B14 | | |
| C14 | | |
| A12 | | |
| B12 | | |
| C12 | | |
| C13 | | |
| A13 | | |
| A14 | | |
| B10 | | |
| B11 | | |
| C11 | | |
| A9 | | |
| B9 | | |
| C9 | | |
| C10 | | |
| A10 | | |
| A11 | | |

CRITICAL L8100 1.0UH-3.51A-0.036OHM — 67 BUCK0_LX0 — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=0.5 MM, DIDT=TRUE, SWITCH_NODE=TRUE — PILE25201D
CRITICAL L8101 1.0UH-3.51A-0.036OHM — 67 BUCK0_LX1 — PILE25201D
CRITICAL L8102 1.0UH-3.51A-0.036OHM — 67 BUCK0_LX2 — PILE25201D
CRITICAL L8103 1.0UH-3.51A-0.036OHM — 67 BUCK0_LX3 — PILE25201D
67 BUCK0_FB — MIN_LINE_WIDTH=0.25MM, MIN_NECK_WIDTH=0.20MM
XW8101 SM
CRITICAL L8104 1.0UH-3.51A-0.036OHM — 67 BUCK1_LX0 — PILE25201D
CRITICAL L8105 1.0UH-3.51A-0.036OHM — 67 BUCK1_LX1 — PILE25201D
CRITICAL L8106 1.0UH-3.51A-0.036OHM — 67 BUCK1_LX2 — PILE25201D
67 BUCK1_FB — MIN_LINE_WIDTH=0.25MM, MIN_NECK_WIDTH=0.20MM
XW8102 SM
CRITICAL L8107 1.0UH-3.51A-0.036OHM — 67 BUCK2_LX0 — PILE25201D
XW8103 SM
CRITICAL L8108 1.0UH-3.51A-0.036OHM — 67 BUCK3_LX0 — PILE25201D
67 BUCK3_FB — MIN_LINE_WIDTH=0.25MM, MIN_NECK_WIDTH=0.20MM
XW8104 SM
CRITICAL L8109 1.0UH-3.51A-0.036OHM — 67 BUCK4_LX0 — PILE25201D
67 BUCK4_FB — MIN_LINE_WIDTH=0.25MM, MIN_NECK_WIDTH=0.20MM
XW8105 SM
CRITICAL L8110 1.0UH-3.7A-0.055OHM — 67 BUCK5_LX0 — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=0.5 MM, DIDT=TRUE, SWITCH_NODE=TRUE — PILE20161D-SM
67 BUCK5_FB — MIN_LINE_WIDTH=0.25MM, MIN_NECK_WIDTH=0.20MM
XW8106 SM
CRITICAL L8111 2.2UH-2.35A-0.073OHM — 67 BUCK6_LX0 — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=0.5 MM, DIDT=TRUE, SWITCH_NODE=TRUE — PILE25201D
67 BUCK6_FB — MIN_LINE_WIDTH=0.25MM, MIN_NECK_WIDTH=0.20MM
XW8107 SM

PPVDD_CPU 60 62 67
CRITICAL C8100–C8104 15UF 20% 4V X5R 0402
CRITICAL C8105–C8109 15UF 20% 4V X5R 0402
CRITICAL C8110 15UF 20% 4V X5R 0402
CRITICAL C8111 15UF 20% 4V X5R 0402

PPVDD_GPU 60 62 67
CRITICAL C8112–C8116 15UF 20% 4V X5R 0402
CRITICAL C8117–C8120 15UF 20% 4V X5R 0402

ADDITIONAL DISTRIBUTED 27UF (NO DERATING)
PPVDD_SOC 60 62 67
CRITICAL C8121–C8123 15UF 20% 4V X5R 0402

ADDITIONAL DISTRIBUTED 64UF (NO DERATING)
PP1V8_S2R 55 56 60 62 67
CRITICAL C8124–C8126 15UF 20% 4V X5R 0402

ADDITIONAL DISTRIBUTED 27UF (NO DERATING)
PP1V2_S2R 55 56 60 62 67
CRITICAL C8127–C8129 15UF 20% 4V X5R 0402

ADDITIONAL DISTRIBUTED 64UF (NO DERATING)
PPVDD_SRAM 60 62 67
CRITICAL C8130–C8132 15UF 20% 4V X5R 0402

ADDITIONAL DISTRIBUTED 32UF (NO DERATING)
PP3V3_S2R 60 62 67
CRITICAL C81A0–C81A3 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C81A4–C81A7 10UF 20% 6.3V CERM-X5R 0402

PP1V8_S2R 55 56 60 62 67
PP1V8_SW1 57 59 60 62 67
PP1V8_SW2 60 62 67
PP1V8_S2R_SW3 60 62 67
PP1V2_S2R 55 56 60 62 67
PP1V2_SW1 60 62 67
PP1V2_S2R_SW2 60 62 67

PMU_VPUMP
MIN_LINE_WIDTH=0.30MM, MIN_NECK_WIDTH=0.20MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM, VOLTAGE=4.6V
C8196 0.22UF 20% 6.3V X5R 0201
C8135 1.0UF 20% 6.3V X5R 0201-1
C8136 1UF 10% 6.3V CERM 402
C8137 1.0UF 20% 6.3V X5R 0201-1
C81A8 1.0UF 20% 6.3V X5R 0201-1
C8138 1.0UF 20% 6.3V X5R 0201-1
C8139 1UF 10% 6.3V CERM 402
C81A9 1.0UF 20% 6.3V X5R 0201-1

C8137 0201 OKAY IF GRAPE HAS EXT FET

62 55 =PPVCC_MAIN_CPU
CRITICAL C8175–C8181 10UF 20% 6.3V CERM-X5R 0402

62 55 =PPVCC_MAIN_GPU
CRITICAL C8182–C8186 10UF 20% 6.3V CERM-X5R 0402

62 55 =PPVCC_MAIN_SOC
CRITICAL C8187 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8188 10UF 20% 6.3V CERM-X5R 0402

NOTE: FOR NO BATTERY SITUATION

67 62 60 55 PPBATT_VCC
CRITICAL C8193 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8194 10UF 20% 6.3V CERM-X5R 0402
60 PPBATT_POS_RC — MIN_LINE_WIDTH=0.30MM, MIN_NECK_WIDTH=0.20MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM, VOLTAGE=4.7V
R8100 0.5 1% 1/16W MF 402

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 128S0339 | 128S0279 | ? | C8140,C8141 | RDAR://PROBLEM/8967213 |

# LDO INPUTS

PP1V8_S2R
1 CAP PER PIN
C8200 1UF 10% 6.3V CERM 402
C8203 1UF 10% 6.3V CERM 402
PP1V2_S2R
C8201 1UF 10% 6.3V CERM 402
PPVCC_MAIN
PPVCC_MAIN
PPVCC_MAIN
PPVCC_MAIN

CRITICAL L8225 4.7UH-3.4A-0.075OHM PILE051D-SM-COMBO-J72 DCR=106MOHM MAX
=PPVCC_MAIN_LED
CRITICAL C8226 10UF 20% 6.3V CERM-X5R 0402
CRITICAL D8228 PMEG4010BEA SOD-323
WLED_LX_A
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20 MM
NET_SPACING_TYPE=PWR
SWITCH_NODE=TRUE
(PPLED_OUT_A)
PPLED_OUT_A
CRITICAL C8250 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8251 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8252 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8253 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8254 4.7UF 10% 35V X5R-CERM 0603
C8259 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_1_A → R8270 1.00 1% 1/32W MF 01005
LED_IO_2_A → R8271 1.00 1% 1/32W MF 01005
LED_IO_3_A → R8272 1.00 1% 1/32W MF 01005
LED_IO_4_A → R8273 1.00 1% 1/32W MF 01005
LED_IO_5_A → R8274 1.00 1% 1/32W MF 01005
LED_IO_6_A → R8275 1.00 1% 1/32W MF 01005
C8271 56PF 2% 50V NP0-C0G-CERM 0201
C8270 56PF 2% 50V NP0-C0G-CERM 0201
C8273 56PF 2% 50V NP0-C0G-CERM 0201
C8272 56PF 2% 50V NP0-C0G-CERM 0201
C8275 56PF 2% 50V NP0-C0G-CERM 0201
C8274 56PF 2% 50V NP0-C0G-CERM 0201

CRITICAL L8255 4.7UH-3.4A-0.075OHM PILE051D-SM-COMBO-J72 DCR=106MOHM MAX
=PPVCC_MAIN_LED
CRITICAL C8256 10UF 20% 6.3V CERM-X5R 0402
CRITICAL D8258 PMEG4010BEA SOD-323
WLED_LX_B
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20 MM
(PPLED_OUT_B)
PPLED_OUT_B
CRITICAL C8260 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8261 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8262 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8263 4.7UF 10% 35V X5R-CERM 0603
CRITICAL C8264 4.7UF 10% 35V X5R-CERM 0603
C8269 56PF 2% 50V NP0-C0G-CERM 0201

LED_IO_1_B → R8280 1.00 1% 1/32W MF 01005
LED_IO_2_B → R8281 1.00 1% 1/32W MF 01005
LED_IO_3_B → R8282 1.00 1% 1/32W MF 01005
LED_IO_4_B → R8283 1.00 1% 1/32W MF 01005
LED_IO_5_B → R8284 1.00 1% 1/32W MF 01005
LED_IO_6_B → R8285 1.00 1% 1/32W MF 01005
C8280 56PF 2% 50V NP0-C0G-CERM 0201
C8281 56PF 2% 50V NP0-C0G-CERM 0201
C8282 56PF 2% 50V NP0-C0G-CERM 0201
C8283 56PF 2% 50V NP0-C0G-CERM 0201
C8284 56PF 2% 50V NP0-C0G-CERM 0201
C8285 56PF 2% 50V NP0-C0G-CERM 0201

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 152S1837 | 152S1789 | ? | L8225,L8255 | RDAR://PROBLEM/13487208 |

OMIT_TABLE

U8100
D2089A0
FCBGA
SYM 2 OF 4

LDO INPUT / LDO
VDD_LDO1_3_4 T18
VDD_LDO2 B16
VDD_LDO5 U9
VDD_LDO6 U10
VDD_LDO7 U14
VDD_LDO8 U15
VDD_LDO9 B15
VDD_LDO10 B17
VDD_LDO11 U16
VDD_LDO13 T17

LCD BACKLIGHT / LCM/GRAPE
WLED_LXA0 C18
WLED_LXA1 C19
VOUT_WLED_A D16
WLED1_A E14
WLED2_A F14
WLED3_A G14
WLED4_A H14
WLED5_A J14
WLED6_A J16
WLED_LXB0 E18
WLED_LXB1 E19
VOUT_WLED_B E16
WLED1_B K14
WLED2_B L14
WLED3_B M14
WLED4_B M16
WLED5_B N14
WLED6_B P14

XTAL
XTAL1 V18
XTAL2 V17

LED_IO1_A_R
LED_IO2_A_R
LED_IO3_A_R
LED_IO4_A_R
LED_IO5_A_R
LED_IO6_A_R
NET_SPACING_TYPE=PWR
SWITCH_NODE=TRUE
LED_IO1_B_R
LED_IO2_B_R
LED_IO3_B_R
LED_IO4_B_R
LED_IO5_B_R
LED_IO6_B_R

# LDO OUTPUTS

VLDO1 U19 (50MA; 2.5-3.3V) PP3V0_SPARE1
VLDO2 A16 (100MA; 1.65-1.805V; BUCK3) PP1V7_VA_VCP
VLDO3 U18 (50MA; 2.5-3.3V) PP3V0_S2R_SENSOR
VLDO4 T19 (50MA; 2.5-3.3V) PP3V0_ALS
VLDO5 V9 (1000MA; 2.5-3.6V) PP3V0_UVLO
VLDO6 V10 (150MA; 2.5-3.6V) PP3V3_ACC
VLDO7 V14 (300MA; 1.7-3.0V) PP3V0_S2R_TRISTAR
VLDO8 V15 (300MA; 1.7-3.0V) PP3V0_S2R_HALL
VLDO9 A15 (300MA; 1.2-3.0V) PP1V3_CAM
VLDO10 A17 (150MA; 0.6-1.3V) PP1V0_SOC
VLDO11 V16 (300MA; 1.7-3.0V) PP2V6_CAM_AF
VLDO13 U17 (300MA; 1.7-3.0V) PP2V9_CAM
ON_BUF T10 (5MA; 1.8V; ON BUFF) PP1V8_ALWAYS

VDD_LCM_SW C17 =PPVCC_MAIN_VDD_LCM
VDD_BOOST_LCM A18 PP6V0_LCM_HI (NOTE: 2MHZ)
BOOST_LCM_LX B19 LCM_LX
LCM_FB C15
VDD_LCM U11 PP6V0_LCM_VBOOST
VLCM1 V11 (100MA; 5.0-6.0V) PP5V25_GRAPE
VLCM2 V12 (100MA; 5.0-6.0V) NO_TEST=TRUE NC_VLCM2
LCM2_EN E8 LCM2_EN
VLCM3 U12 (5MA; 5.0-6.0V) NO_TEST=TRUE NC_VLCM3

CRITICAL L8229 2.2UH-1.05A-0.195OHM WLS201612E-SM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
CRITICAL D8230 PMEG2005AEL SOD882
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
C8212 10UF 20% 25V X5R-CERM 0603
C8210 2.2UF 20% 10V X5R-CERM 402
CRITICAL C8211 10UF 20% 6.3V X5R-CERM 0402-2

XTAL1 V18 PMU_XTAL
XTAL2 V17 PMU_EXTAL
CRITICAL Y8200 32.768K-20PPM-12.5PF 2012-1
CRITICAL C8215 18PF 5% 25V C0G-CERM 0201
CRITICAL C8216 18PF 5% 25V C0G-CERM 0201
R8250 1K 5% 1/20W MF 0201

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 197S0399 | 197S0392 | ? | Y8200 | RDAR://PROBLEM/9936684 |

# LDO BYPASS

PP3V0_SPARE1
PP1V7_VA_VCP
PP3V0_S2R_TRISTAR
PP3V0_ALS
PP3V0_UVLO
PP3V3_ACC
PP3V0_S2R_HALL
PP3V0_S2R_SENSOR
CRITICAL C8237 2.2UF 10% 6.3V X5R 0201
CRITICAL C8236 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8235 4.7UF 20% 6.3V X5R-CERM 0402
CRITICAL C8234 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8233 2.2UF 10% 6.3V X5R 0201
CRITICAL C8232 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8231 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8230 2.2UF 10% 6.3V X5R 0201

PP1V3_CAM
PP1V0_SOC
PP2V6_CAM_AF
PP2V9_CAM
PP1V8_ALWAYS
C8242 0.22UF 10% 6.3V X5R 0201
CRITICAL C8241 10UF 20% 6.3V CERM-X5R 0402
CRITICAL C8240 4.7UF 20% 6.3V X5R-CERM1 0402
CRITICAL C8239 4.7UF 20% 6.3V X5R-CERM1 0402
CRITICAL C8238 4.7UF 20% 6.3V X5R-CERM1 0402

I2C ADDRESS: 0111100X (0X78)

OMIT_TABLE

U8100
D2089A0
FCBGA
SYM 3 OF 4

BUTTON1
BUTTON2
BUTTON3
BUTTON4
ACC_DET
ACC_ID
BRICK_ID
ADC_IN7
ADC_IN31
KEEPACT
SHDN
RESET_IN1
RESET_IN2
RESET_IN3
RESET*
IRQ*
SCL
SDA
DWI_CK
DWI_DI
DWI_DO
TDEV1
TDEV2
TDEV3
TDEV4
TDEV5
TDEV6
TDEV7
TDEV8
TBAT
TCAL

ANALOG INPUT
REFRENCES
DIGITAL INPUT
32K CLK
WDOG
RESET
GPIO
I2C & DWI
TEMPERATURE
ANALOG MUX

IREF
VREF
VDD_REF
VDD_REF_A
VDD_RTC
ADC_REF
OUT_32K
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
AMUX_A0
AMUX_A1
AMUX_A2
AMUX_A3
AMUX_AY
AMUX_B0
AMUX_B1
AMUX_B2
AMUX_B3
AMUX_BY

GPIO_BTN_HOME_L
GPIO_BTN_ONOFF_L
GPIO_BTN_SRL_L
GPIO_BTN_BUTTON4
PMU_E75_ACC_DET_L
PMU_ACC_ID
PMU_USB_BRICKID_R
ADC_IN7
GPIO_SOC2PMU_KEEPACT
PMU_SHDWN (INTERNAL PULL-DOWN)
WDOG_SOC2PMU_RESET_IN (INTERNAL PULL-DOWN)
TS2PMU_RESET_IN
SOCHOT1_L
RESET_SOC_L
GPIO_PMU2SOC_IRQ_L (PULLUP INSIDE SOC)
I2C0_SCL_1V8
I2C0_SDA_1V8
DWI_AP_CLK (INTERNAL PULL-DOWN)
DWI_AP_DO (INTERNAL PULL-DOWN)
NC_DWI_AP_DI NO_TEST=TRUE
BATT_TNC
PMU_TCAL

PMU_IREF
PMU_VREF
PMU_VDD_REF
PMU_VDD_RTC
PMU_ADC_REF
PMU_OUT_32K_CLK_GPS
PMU_GPIO_CLK_32K_OSCAR
PMU_GPIO_CLK_32K_WLAN
PMU_GPIO_BT_REG_ON
PMU_GPIO_WLAN_REG_ON
PMU_GPIO_PMU2BBPMU_RST_R_L
UART5_BATT_TRXD
PMU_GPIO_BT_HOST_WAKE
PMU_GPIO_WLAN_HOST_WAKE
PMU_GPIO_BB2PMU_HOST_WAKE
PMU_GPIO_CODEC_HS_INT_L
PMU_GPIO_MB_HALL1_IRQ
GPIO_TS2SOC2PMU_INT
PMU_GPIO_MB_HALL2_IRQ
PMU_GPIO_CODEC_RST_L
NC_PMU_GPIO15 NO_TEST=TRUE
PMU_GPIO_OSCAR2PMU_HOST_WAKE
PMU_GPIO_BB_VBUS_DET
PPVDD_CPU_SOC_SENSE
PPVDD_GPU_SOC_SENSE
PPVDD_SOC_SENSE
TP_AMUX_A3
TP_AMUX_AY
PPVDD_CPU_RAIL_SENSE
PPVDD_GPU_RAIL_SENSE
PPVDD_SOC_RAIL_SENSE
TP_AMUX_B3
TP_AMUX_BY

R8398 0.00 5% 1/32W MF 01005
C8300 0.01UF 10% 6.3V X5R 01005
C8301 0.01UF 10% 6.3V X5R 01005
C8302 0.01UF 10% 6.3V X5R 01005
R8399 0 5% 1/20W MF 201
PMU_USB_BRICKID TRISTAR1 USE 6.34K
C8305 0.1UF 10% 6.3V CERM-X5R 0201
R8303 200K 1% 1/20W MF 201
C8306 0.1UF 10% 6.3V CERM-X5R 0201
C8307 1UF 10% 10V X5R 402-1
C8308 1.0UF 20% 10V X5R-CERM 0201-1
C8310 1000PF 10% 6.3V X5R-CERM 01005
R8330 1.00K 5% 1/32W MF 01005
C8340 100PF 5% 16V NP0-C0G 01005
R8340 3.92K 0.1% 0201 1/20W MF
RESISTOR FOR TEMP CALIBRATION

CRITICAL
R8327 10KOHM-1%-0.31MA 0201 PLACE_NEAR=U6800.1:10MM PLACE_SIDE=TOP
C8327 100PF 5% 16V NP0-C0G 01005
(TEMP1 - NEAR BB)

CRITICAL
R8328 10KOHM-1%-0.31MA 0201 PLACE_NEAR=U5600.D2:10MM PLACE_SIDE=TOP
C8328 100PF 5% 16V NP0-C0G 01005
(TEMP2 - NEAR PROX)

CRITICAL
R8321 10KOHM-1%-0.31MA 0201 PLACE_NEAR=U5800.3D:10MM PLACE_SIDE=TOP
C8321 100PF 5% 16V NP0-C0G 01005
(TEMP3 - TOP SIDE NEAR WIFI)

CRITICAL
R8322 10KOHM-1%-0.31MA 0201 PLACE_NEAR=J1800.1J:10MM PLACE_SIDE=TOP
C8322 100PF 5% 16V NP0-C0G 01005
(TEMP4 - TOP SIDE NEAR AJ FLEX CONN)

CRITICAL
R8323 10KOHM-1%-0.31MA 0201 PLACE_NEAR=U1600.A1:10MM PLACE_SIDE=TOP
C8323 100PF 5% 16V NP0-C0G 01005
(TEMP5 - TOP SIDE NEAR NAND)

CRITICAL
R8324 10KOHM-1%-0.31MA 0201 PLACE_NEAR=J2800.1:10MM PLACE_SIDE=TOP
C8324 100PF 5% 16V NP0-C0G 01005
(TEMP6 TOP SIDE NEAR REAR CAM)

CRITICAL
R8325 10KOHM-1%-0.31MA 0201 PLACE_NEAR=U8600.W19:10MM PLACE_SIDE=BOTTOM
C8325 100PF 5% 16V NP0-C0G 01005
(TEMP7 - BOTTOM SIDE NEAR SOC)

CRITICAL
R8326 10KOHM-1%-0.31MA 0201 PLACE_NEAR=U8100.K3:10MM PLACE_SIDE=BOTTOM
C8326 100PF 5% 16V NP0-C0G 01005
(TEMP8 - BOTTOM SIDE NEAR PMU)

PA_NTC_P
PA_NTC_N
BOARD_TEMP2_P
BOARD_TEMP2_N
BOARD_TEMP3_P
BOARD_TEMP3_N
BOARD_TEMP4_P
BOARD_TEMP4_N
BOARD_TEMP5_P
BOARD_TEMP5_N
BOARD_TEMP6_P
BOARD_TEMP6_N
BOARD_TEMP7_P
BOARD_TEMP7_N
BOARD_TEMP8_P
BOARD_TEMP8_N

PLACE XW AND CAP CLOSE TO PMU

XW8327 XW8328 XW8321 XW8322 XW8323 XW8324 XW8325 XW8326 SM

SWITCH TO GATE POWER TO SOC AND NAND. NEEDED FOR J72 ROUTING.

CRITICAL
U8360
TPS22924X
CSP
=PP1V8_S2R_EXT_SWITCH
PP1V8_SW1
PP1V8_EXT_SW
C8360 10UF 20% 10V X5R-CERM 0402-2
C8365 0.01UF 10% 6.3V X5R 01005

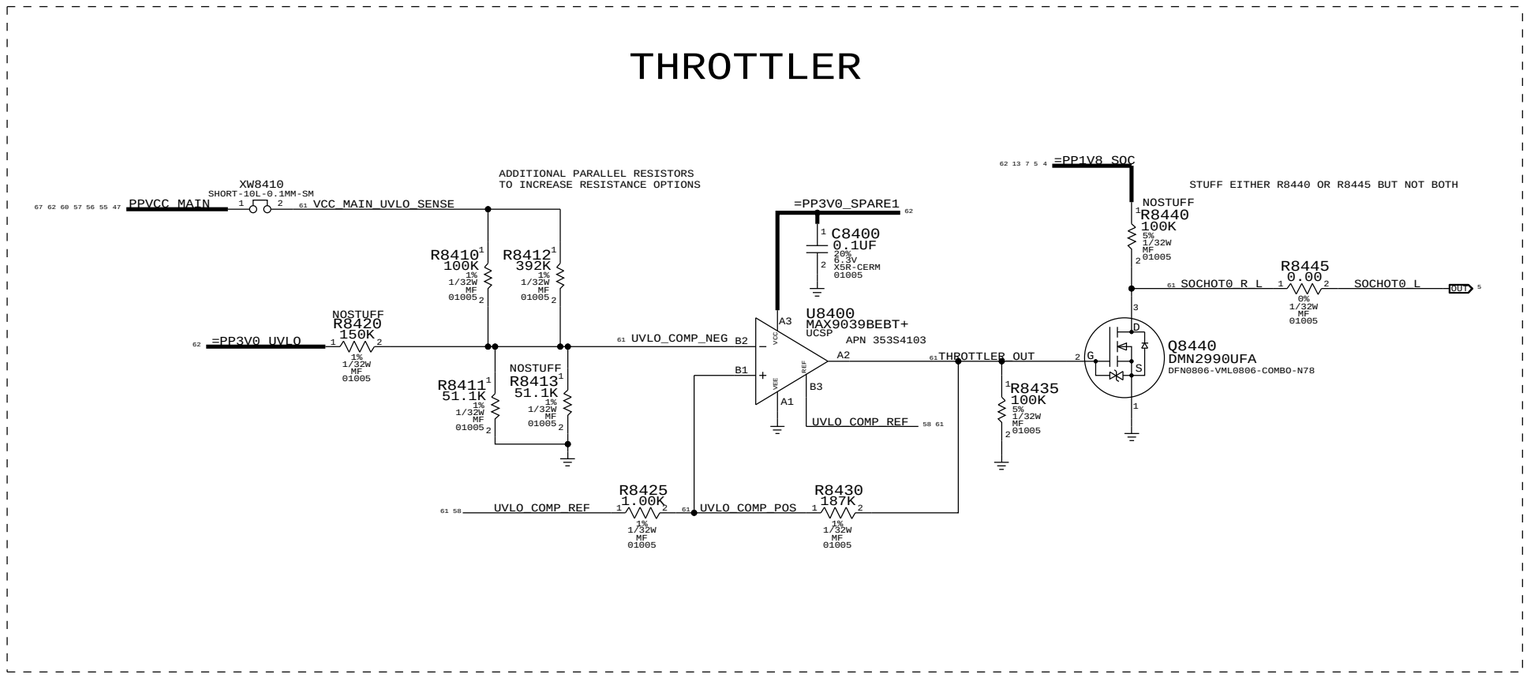
BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS
SWITCH NEEDED TO GATE POWER TO NAND AND SOC

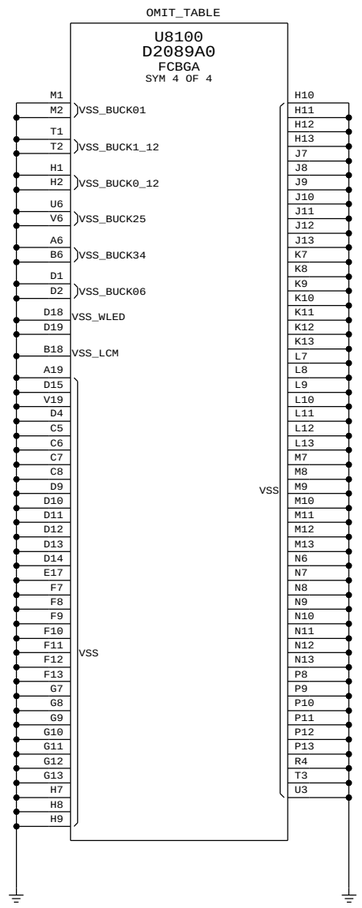
=PP3V3_S2R_SWITCH
PPVCC_MAIN
=PP1V8_NAND
VCC_MAIN_PP3V3SW_RAMP
PP3V3_SW
CRITICAL
U8350
SLG5AP1443V
TDFN
C8550 0.1UF 10% 16V X5R-CERM 0201
C8355 1.0UF 20% 6.3V X6S 0201-1
R8352 100K 5% 1/32W MF 01005
C8552 4700PF 10% 10V X7R 201
C8356 1UF 10% 10V X5R-CERM 0402-2

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 107S0150 | 107S0208 | ? | | RDAR://PROBLEM/8380367 |

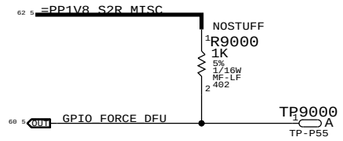
R8321,R8322,R8323,R8324,R8325,R8326

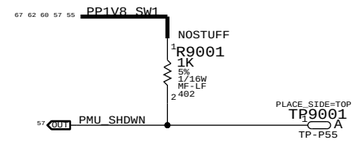
# THROTTLER



# DEBUG RESET ACCESS



# SMT TEST FIXTURE TP

## POWER

| | | |
|---|---|---|
| PPVDD_CPU | FUNC_TEST=TRUE | 55 62 67 |
| PPVDD_GPU | FUNC_TEST=TRUE | 55 62 67 |
| PPVDD_SOC | FUNC_TEST=TRUE | 55 62 67 |
| PP1V8_S2R | FUNC_TEST=TRUE | 55 56 62 67 |
| PP1V8_SW1 | FUNC_TEST=TRUE | 55 57 59 62 67 |
| PP1V8_SW1_FOREHEAD | FUNC_TEST=TRUE | 62 67 |
| PP1V8_EXT_SW | FUNC_TEST=TRUE | 57 62 67 |
| PP1V8_SW2 | FUNC_TEST=TRUE | 55 62 67 |
| PP1V8_S2R_SW3 | FUNC_TEST=TRUE | 55 62 67 |
| PP1V8_S2R_SW3_COMP | FUNC_TEST=TRUE | 62 67 |
| PP1V2_S2R | FUNC_TEST=TRUE | 55 56 62 67 |
| PP1V2_SW1 | FUNC_TEST=TRUE | 55 62 67 |
| PP1V2_S2R_SW2 | FUNC_TEST=TRUE | 55 62 67 |
| PPVDD_SRAM | FUNC_TEST=TRUE | 55 62 67 |
| PP3V3_S2R | FUNC_TEST=TRUE | 55 62 67 |
| PP3V3_SW | FUNC_TEST=TRUE | 57 62 67 |
| PP3V0_SPARE1 | FUNC_TEST=TRUE | 56 62 67 |
| PP1V7_VA_VCP | FUNC_TEST=TRUE | 56 62 67 |
| PP3V0_S2R_SENSOR | FUNC_TEST=TRUE | 56 62 67 |
| PP3V0_ALS | FUNC_TEST=TRUE | 56 62 67 |
| PP3V3_ACC | FUNC_TEST=TRUE | 56 62 67 |
| PP3V0_S2R_TRISTAR | FUNC_TEST=TRUE | 56 62 67 |
| PP3V0_S2R_HALL | FUNC_TEST=TRUE | 56 62 67 |
| PP1V3_CAM | FUNC_TEST=TRUE | 56 62 67 |
| PP1V0_SOC | FUNC_TEST=TRUE | 56 62 67 |
| PP2V6_CAM_AF | FUNC_TEST=TRUE | 56 62 67 |
| PP2V9_CAM | FUNC_TEST=TRUE | 56 62 67 |
| PP5V25_GRAPE | FUNC_TEST=TRUE | 56 60 62 67 |
| PPVCC_MAIN | FUNC_TEST=TRUE | 47 55 56 57 58 62 67 |
| PPBATT_VCC | FUNC_TEST=TRUE | 55 60 62 67 |
| PPVBUS_USB_DCIN | FUNC_TEST=TRUE | 55 62 67 |
| PP1V8_ALWAYS | FUNC_TEST=TRUE | 56 62 67 |
| PPLED_OUT_A | FUNC_TEST=TRUE | 56 62 67 |
| PPLED_OUT_B | FUNC_TEST=TRUE | 56 62 67 |
| PP6V0_LCM_VBOOST | FUNC_TEST=TRUE | 56 67 |

| | | |
|---|---|---|
| PPBATT_POS_RC | FUNC_TEST=TRUE | 55 |
| PMU_VCENTER | FUNC_TEST=TRUE | 55 67 |
| PPVBUS_PROT | FUNC_TEST=TRUE | 47 55 67 |
| VBUS_PROT_G | FUNC_TEST=TRUE | 55 |

| | | |
|---|---|---|
| PP1V2_CAM_FRONT_FILT | FUNC_TEST=TRUE | 67 |
| PP1V3_CAM_REAR_FILT | FUNC_TEST=TRUE | 23 67 |
| PP1V7_VCP | FUNC_TEST=TRUE | 15 67 |
| PP1V8_CAM_FRONT_FILT | FUNC_TEST=TRUE | 22 67 |
| PP1V8_CAM_REAR_FILT | FUNC_TEST=TRUE | 23 67 |
| PP1V8_DMIC_FILT | FUNC_TEST=TRUE | 16 67 |
| PP1V8_GRAPE_SW | FUNC_TEST=TRUE | 51 52 61 67 |

| | | |
|---|---|---|
| PP1V8_COMP | FUNC_TEST=TRUE | 24 67 |
| PP2V6_CAM_REAR_AF_FILT | FUNC_TEST=TRUE | 23 67 |
| PP2V9_AVDD_CAM_FRONT_FILT | FUNC_TEST=TRUE | 22 67 |
| PP2V9_AVDD_CAM_REAR_FILT | FUNC_TEST=TRUE | 23 67 |
| PP3V0_ALS_FILT | FUNC_TEST=TRUE | 22 67 |
| PP3V0_HP_ALS_FILT | FUNC_TEST=TRUE | 67 |
| PP3V0_IO_ALS_FILT | FUNC_TEST=TRUE | 67 |
| PP3V0_S2R_HALL_FILT | FUNC_TEST=TRUE | 20 50 67 |

| | | |
|---|---|---|
| PP3V0_GYRO | FUNC_TEST=TRUE | 19 67 |
| PP3V0_ACCEL | FUNC_TEST=TRUE | 19 67 |
| PP3V0_COMP | FUNC_TEST=TRUE | 24 67 |
| PP3V0_SENSOR_PROX_FILT | FUNC_TEST=TRUE | 67 |
| PP3V0_SENSOR_PROX_ADUX1049_FILT | FUNC_TEST=TRUE | 67 |
| PP3V0_SENSOR_PROX_AD7149_FILT | FUNC_TEST=TRUE | 45 67 |
| PP5V25_GRAPE | FUNC_TEST=TRUE | 56 60 62 67 |
| PPVCC_MAIN_LCD_SW_CONN | FUNC_TEST=TRUE | 53 67 |
| PPVCC_MAIN_LCD_SW | FUNC_TEST=TRUE | 53 67 |

| | | |
|---|---|---|
| PP_SMPS1_MSMC_1V05 | FUNC_TEST=TRUE | 26 28 68 |
| PP_SMPS2_RF1_1V3 | FUNC_TEST=TRUE | 26 28 31 68 |
| PP_SMPS3_MSME_1V8 | FUNC_TEST=TRUE | 25 26 28 29 31 |
| PP_SMPS4_RF2_2V05 | FUNC_TEST=TRUE | 26 31 68 |
| PP_SMPS5_DSP_1V05 | FUNC_TEST=TRUE | 26 68 |

| | | |
|---|---|---|
| PP_LDO1 | FUNC_TEST=TRUE | 26 68 |

| | | |
|---|---|---|
| PP3V0_UVLO | FUNC_TEST=TRUE | 56 62 67 |

| | | |
|---|---|---|
| TP_BB_TEST_MODE_0 | FUNC_TEST=TRUE | 28 |
| TP_BB_TEST_MODE_1 | FUNC_TEST=TRUE | 28 |

| | | |
|---|---|---|
| GPIO_SOC2OSCAR_DBGEN_R | FUNC_TEST=TRUE | 19 |

| | | | |
|---|---|---|---|
| TP9300 | PPBATT_VCC | PLACE_NEAR=J7500.4:10MM | 55 60 62 67 |
| TP9301 | PPBATT_VCC | PLACE_NEAR=J7500.4:10MM | 55 60 62 67 |
| TP9302 | PPBATT_VCC | PLACE_NEAR=J7500.4:10MM | 55 60 62 67 |
| TP9305 | | PLACE_NEAR=J7500.3:10MM | |
| TP9306 | | PLACE_NEAR=J7500.3:10MM | |
| TP9307 | | PLACE_NEAR=J7500.3:10MM | |
| TP9310 | PPVBUS_E75_USB_CONN | PLACE_NEAR=J6200.9:20MM | 48 49 60 67 |
| TP9311 | PPVBUS_E75_USB_CONN | PLACE_NEAR=J6200.9:20MM | 48 49 60 67 |
| TP9312 | PPVBUS_E75_USB_CONN | PLACE_NEAR=J6200.9:20MM | 48 49 60 67 |
| TP9315 | | PLACE_NEAR=TP9310.1:30MM | |
| TP9316 | | PLACE_NEAR=TP9310.1:30MM | |
| TP9317 | | PLACE_NEAR=TP9310.1:30MM | |

All: A TP-1P0-TOP

## GPIO

| | | |
|---|---|---|
| GPIO_CAM_ALS2SOC_IRQ_L_F | FUNC_TEST=TRUE | 22 |
| GPIO_FORCE_DFU | FUNC_TEST=TRUE | 5 59 |
| GPIO_GRAPE2SOC_IRQ_FILT_L | FUNC_TEST=TRUE | |
| GPIO_SOC2BB_RADIO_ON_L | FUNC_TEST=TRUE | 5 25 27 |
| GPIO_SOC2BB_RST_L | FUNC_TEST=TRUE | 5 25 27 67 |
| GPIO_SOC2GRAPE_RESET_FILT_L | FUNC_TEST=TRUE | 5 52 61 |
| GPIO_OSCAR_RESET_L | FUNC_TEST=TRUE | 5 19 67 |
| CLK_32K_SOC2CUMULUS_FILT | FUNC_TEST=TRUE | 64 |
| HP_ALS_IRQ_L_CONN_FILT | FUNC_TEST=TRUE | |

## PMU GPIO

| | | |
|---|---|---|
| PMU_GPIO_BB2PMU_HOST_WAKE | FUNC_TEST=TRUE | 25 29 57 |
| PMU_GPIO_BT_REG_ON_R | FUNC_TEST=TRUE | 46 |
| PMU_GPIO_CLK_32K_OSCAR | FUNC_TEST=TRUE | 19 57 64 |
| PMU_GPIO_CLK_32K_WLAN_R | FUNC_TEST=TRUE | 46 |
| PMU_GPIO_CODEC_HS_INT_L | FUNC_TEST=TRUE | 15 57 |
| PMU_GPIO_PMU2BBPMU_RST_L | FUNC_TEST=TRUE | 25 27 57 67 |
| PMU_GPIO_WLAN_REG_ON_R | FUNC_TEST=TRUE | 46 |
| PMU_TCAL | FUNC_TEST=TRUE | 57 |
| PMU_E75_ACC_DET_L | FUNC_TEST=TRUE | 47 57 |
| TS_E75_ACC_DET_L | FUNC_TEST=TRUE | 47 |
| PMU_GPIO_MB_HALL1_IRQ | FUNC_TEST=TRUE | 20 57 |
| PMU_GPIO_MB_HALL2_IRQ | FUNC_TEST=TRUE | 50 57 |

## AUDIO

| | | |
|---|---|---|
| CONN_HP_HEADSET_DET_FILT | FUNC_TEST=TRUE | 15 16 |
| CONN_HP_HS3_FILT | FUNC_TEST=TRUE | 15 16 60 65 |
| CONN_HP_HS3_REF_FILT | FUNC_TEST=TRUE | 15 16 60 65 |
| CONN_HP_HS3_FILT | FUNC_TEST=TRUE | 15 16 60 65 |
| CONN_HP_HS3_REF_FILT | FUNC_TEST=TRUE | 15 16 60 65 |
| CONN_HP_HS4_FILT | FUNC_TEST=TRUE | 15 16 65 |
| CONN_HP_HS4_REF_FILT | FUNC_TEST=TRUE | 15 16 65 |
| CONN_HP_LEFT_FILT | FUNC_TEST=TRUE | 15 16 65 |
| CONN_HP_RIGHT_FILT | FUNC_TEST=TRUE | 15 16 65 |
| SPKRAMP_L1_OUT_N | FUNC_TEST=TRUE | 18 49 65 |
| SPKRAMP_L1_OUT_P | FUNC_TEST=TRUE | 18 49 65 |
| SPKRAMP_R1_OUT_N | FUNC_TEST=TRUE | 17 49 65 |
| SPKRAMP_R1_OUT_P | FUNC_TEST=TRUE | 17 49 65 |
| SPKRAMP_L2_OUT_N | FUNC_TEST=TRUE | 18 49 65 |
| SPKRAMP_L2_OUT_P | FUNC_TEST=TRUE | 18 49 65 |
| SPKRAMP_R2_OUT_N | FUNC_TEST=TRUE | 17 49 65 |
| SPKRAMP_R2_OUT_P | FUNC_TEST=TRUE | 17 49 65 |

| | | |
|---|---|---|
| LEFT_CH_OUT_P | FUNC_TEST=TRUE | 15 18 65 |
| LEFT_CH_OUT_N | FUNC_TEST=TRUE | 15 18 65 |
| RIGHT_CH_OUT_P | FUNC_TEST=TRUE | 15 17 65 |
| RIGHT_CH_OUT_N | FUNC_TEST=TRUE | 15 17 65 |
| AIN3P | FUNC_TEST=TRUE | 15 |
| AIN3N | FUNC_TEST=TRUE | 15 |

| | | |
|---|---|---|
| GND_AUDIO_CODEC | FUNC_TEST=TRUE | 15 67 |
| DMIC1_FF_SCLK_FILT | FUNC_TEST=TRUE | 16 64 |
| DMIC1_FF_SD_FILT | FUNC_TEST=TRUE | 16 64 |
| L81_SPEAKER_VQ | FUNC_TEST=TRUE | 15 |

## GRAPE

| | | |
|---|---|---|
| GPIO_GRAPE2SOC_IRQ_L | FUNC_TEST=TRUE | 5 52 61 |
| GPIO_SOC2GRAPE_RESET_L | FUNC_TEST=TRUE | 5 52 61 67 |
| CLK_32K_SOC2CUMULUS | FUNC_TEST=TRUE | 5 52 61 64 |
| DISPLAY_SYNC | FUNC_TEST=TRUE | 4 52 61 |
| SPI2_GRAPE_SCLK | FUNC_TEST=TRUE | 5 52 61 64 |
| SPI2_GRAPE_MISO | FUNC_TEST=TRUE | 5 52 61 64 |
| SPI2_GRAPE_MOSI | FUNC_TEST=TRUE | 5 52 61 64 |
| SPI2_GRAPE_CS_L | FUNC_TEST=TRUE | 5 52 61 64 |
| VCC_MAIN_GRAPE_RAMP | FUNC_TEST=TRUE | 51 |

## UART

| | | |
|---|---|---|
| UART0_SOC_RXD | FUNC_TEST=TRUE | 5 47 64 |
| UART0_SOC_TXD | FUNC_TEST=TRUE | 5 47 64 |

## BACKLIGHT

| | | |
|---|---|---|
| PPLED_BACK_REG_A | FUNC_TEST=TRUE | 53 67 |
| LED_IO_1_A | FUNC_TEST=TRUE | 53 56 65 |
| LED_IO_2_A | FUNC_TEST=TRUE | 53 56 65 |
| LED_IO_3_A | FUNC_TEST=TRUE | 53 56 65 |
| LED_IO_4_A | FUNC_TEST=TRUE | 53 56 65 |
| LED_IO_5_A | FUNC_TEST=TRUE | 53 56 65 |
| LED_IO_6_A | FUNC_TEST=TRUE | 53 56 65 |

| | | |
|---|---|---|
| PPLED_BACK_REG_B | FUNC_TEST=TRUE | 53 67 |
| LED_IO_1_B | FUNC_TEST=TRUE | 53 56 65 |
| LED_IO_2_B | FUNC_TEST=TRUE | 53 56 65 |
| LED_IO_3_B | FUNC_TEST=TRUE | 53 56 65 |
| LED_IO_4_B | FUNC_TEST=TRUE | 53 56 65 |
| LED_IO_5_B | FUNC_TEST=TRUE | 53 56 65 |
| LED_IO_6_B | FUNC_TEST=TRUE | 53 56 65 |

## BATTERY

| | | |
|---|---|---|
| BATT_SWI_CONN | FUNC_TEST=TRUE | 54 64 |
| BATT_NTC | FUNC_TEST=TRUE | 54 57 60 67 |

## E75

| | | |
|---|---|---|
| E75_ACC_DET_CONN_L | FUNC_TEST=TRUE | 47 49 60 |
| PPOUT_E75_ACC_ID1_CONN | FUNC_TEST=TRUE | 48 49 60 67 |
| PPOUT_E75_ACC_ID2_CONN | FUNC_TEST=TRUE | 48 49 60 67 |
| E75_DPAIR1_CONN_P | FUNC_TEST=TRUE | 47 49 60 64 |
| E75_DPAIR1_CONN_N | FUNC_TEST=TRUE | 47 49 60 64 |
| E75_DPAIR2_CONN_P | FUNC_TEST=TRUE | 47 49 60 64 |
| E75_DPAIR2_CONN_N | FUNC_TEST=TRUE | 47 49 60 64 |
| PPVBUS_E75_USB_CONN | FUNC_TEST=TRUE | 48 49 60 67 |

## REEST JTAG/CONFIG

| | | |
|---|---|---|
| JTAG_SOC_SEL | FUNC_TEST=TRUE | 4 13 |
| JTAG_SOC_TCK | FUNC_TEST=TRUE | 4 47 64 |
| JTAG_SOC_TDI | FUNC_TEST=TRUE | 4 64 |
| TP_JTAG_SOC_TDO | FUNC_TEST=TRUE | 4 64 |
| JTAG_SOC_TMS | FUNC_TEST=TRUE | 4 47 64 |
| JTAG_SOC_TRST_L | FUNC_TEST=TRUE | 4 13 64 |
| SOC_TESTMODE | FUNC_TEST=TRUE | 4 13 |
| RESET_SOC_L | FUNC_TEST=TRUE | 4 13 25 47 57 61 67 |
| PS_HOLD_PMIC | FUNC_TEST=TRUE | 25 27 |

## BUTTONS

| | | |
|---|---|---|
| GPIO_BTN_ONOFF_L_FILT | FUNC_TEST=TRUE | 21 |
| GPIO_BTN_HOME_L | FUNC_TEST=TRUE | 5 50 57 |
| GPIO_BTN_VOL_UP_L_FILT | FUNC_TEST=TRUE | 21 |
| GPIO_BTN_VOL_DOWN_L_FILT | FUNC_TEST=TRUE | 21 |
| GPIO_BTN_SRL_L_FILT | FUNC_TEST=TRUE | 21 |

## BOARD TEMP

| | | |
|---|---|---|
| PA_NTC_P | FUNC_TEST=TRUE | 57 65 |
| BOARD_TEMP2_P | FUNC_TEST=TRUE | 57 65 |
| BOARD_TEMP3_P | FUNC_TEST=TRUE | 57 65 |
| BOARD_TEMP4_P | FUNC_TEST=TRUE | 57 65 |
| BOARD_TEMP5_P | FUNC_TEST=TRUE | 57 65 |
| BOARD_TEMP6_P | FUNC_TEST=TRUE | 57 65 |
| BOARD_TEMP7_P | FUNC_TEST=TRUE | 57 65 |
| BOARD_TEMP8_P | FUNC_TEST=TRUE | 57 65 |

## USB

| | | |
|---|---|---|
| USB_SOC_N | FUNC_TEST=TRUE | 4 47 64 |
| USB_SOC_P | FUNC_TEST=TRUE | 4 47 64 |

## CAMERA

| | | |
|---|---|---|
| ISP0_CAM_REAR_CLK_F | FUNC_TEST=TRUE | 23 64 |
| ISP0_CAM_REAR_SCL_F | FUNC_TEST=TRUE | 23 64 |
| ISP0_CAM_REAR_SDA_F | FUNC_TEST=TRUE | 23 64 |
| ISP0_CAM_REAR_SHUTDOWN_L_F | FUNC_TEST=TRUE | 23 67 |
| ISP1_CAM_FRONT_CLK_F | FUNC_TEST=TRUE | 22 64 |
| ISP1_CAM_FRONT_SCL_F | FUNC_TEST=TRUE | 22 64 |
| ISP1_CAM_FRONT_SDA_F | FUNC_TEST=TRUE | 22 64 |
| ISP1_CAM_FRONT_SHUTDOWN_L_F | FUNC_TEST=TRUE | 22 67 |

## NAND

| | | |
|---|---|---|
| FMI0_CE0_L | FUNC_TEST=TRUE | 6 14 61 66 |

## DISPLAY

| | | |
|---|---|---|
| DISPLAY_SYNC_FILT | FUNC_TEST=TRUE | |

## I2C

| | | |
|---|---|---|
| I2C3_CAM_ALS_SCL_1V8_F | FUNC_TEST=TRUE | 22 64 |
| I2C3_CAM_ALS_SDA_1V8_F | FUNC_TEST=TRUE | 22 64 |
| I2C0_HP_ALS_SCL_1V8_FILT | FUNC_TEST=TRUE | 64 |
| I2C0_HP_ALS_SDA_1V8_FILT | FUNC_TEST=TRUE | 64 |
| I2C0_SCL_1V8 | FUNC_TEST=TRUE | 5 57 64 |
| I2C0_SDA_1V8 | FUNC_TEST=TRUE | 5 57 64 |

## SIM

| | | |
|---|---|---|
| SIMCRD_RST_CONN | FUNC_TEST=TRUE | 29 44 |
| SIMCRD_CLK_CONN | FUNC_TEST=TRUE | 29 44 |
| SIMCRD_IO_CONN | FUNC_TEST=TRUE | 29 44 |
| SIM_TRAY_DETECT | FUNC_TEST=TRUE | 29 44 |
| PP_LDO6_RUIM_1V8 | FUNC_TEST=TRUE | 26 28 44 68 |

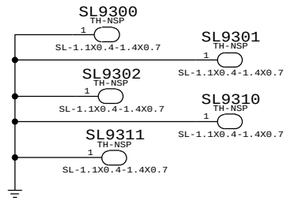
## RF FIXTURE

| | | |
|---|---|---|
| E75_DPAIR1_CONN_N | FUNC_TEST=TRUE | 47 49 60 64 |
| E75_DPAIR1_CONN_P | FUNC_TEST=TRUE | 47 49 60 64 |
| E75_DPAIR2_CONN_N | FUNC_TEST=TRUE | 47 49 60 64 |
| E75_DPAIR2_CONN_P | FUNC_TEST=TRUE | 47 49 60 64 |
| PPVBUS_E75_USB_CONN | FUNC_TEST=TRUE | 48 49 60 67 |
| PPOUT_E75_ACC_ID1_CONN | FUNC_TEST=TRUE | 48 49 60 67 |
| PPOUT_E75_ACC_ID2_CONN | FUNC_TEST=TRUE | 48 49 60 67 |
| E75_ACC_DET_CONN_L | FUNC_TEST=TRUE | 47 49 60 |
| BATT_NTC | FUNC_TEST=TRUE | 54 57 60 67 |

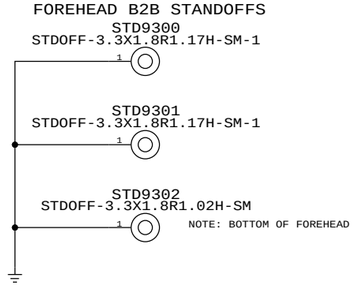
TEST POINT RULES:
CENTER TO CENTER SPACING >= 1MM
DIAMETER >= 0.5MM
EDGE TO SHIELD >=0.55MM

## PLATED THROUGH HOLES

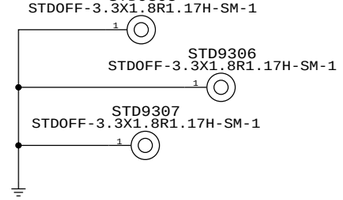
DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

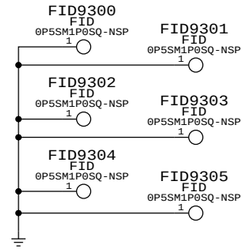



## FOREHEAD B2B STANDOFFS




## GRAPE AND DISPLAY B2B STANDOFFS



# EE CHARACTERIZATION TP

## NAND

BOTTOM SIDE PP9460 P4MM SM (PP) 1 FMI0_AD<0> PLACE_SIDE=BOTTOM PLACE_NEAR=U0600.AS2:2MM 6 14 61 66
NO_XNET_CONNECTION=TRUE
BOTTOM SIDE PP9461 P4MM SM (PP) 1 FMI0_DQS PLACE_SIDE=BOTTOM PLACE_NEAR=U0600.BS4:2MM 6 14 61 66
NO_XNET_CONNECTION=TRUE

| | | | |
|---|---|---|---|
| | FMI0_AD<0..7> | EE_TEST=TRUE FUNC_TEST=TRUE | 6 14 61 66 |
| | FMI0_CE0_L | FUNC_TEST=TRUE | 6 14 60 66 |
| | FMI0_ALE | FUNC_TEST=TRUE | 6 14 66 |
| | FMI0_CLE | FUNC_TEST=TRUE | 6 14 66 |
| | FMI0_WE_L | FUNC_TEST=TRUE | 6 14 66 |
| | FMI0_RE_L | FUNC_TEST=TRUE | 6 14 66 |
| | FMI0_DQS | FUNC_TEST=TRUE | 6 14 61 66 |
| | FMI1_AD<0> | FUNC_TEST=TRUE | 6 14 66 |
| | FMI1_CE0_L | | 6 14 66 |
| | FMI1_ALE | | 6 14 66 |
| | FMI1_CLE | | 6 14 66 |
| | FMI1_WE_L | | 6 14 66 |
| | FMI1_RE_L | | 6 14 66 |
| | FMI1_DQS | | 6 14 66 |
| | PPVREF_FMI_SOC | FUNC_TEST=TRUE | 6 66 |
| | PPVREF_FMI_NAND | FUNC_TEST=TRUE | 14 66 |

TOP SIDE PP9440 P4MM SM (PP) 1 TP_FMI_TCKC_NAND PLACE_SIDE=TOP 14
TOP SIDE PP9441 P4MM SM (PP) 1 TP_FMI_TMSC_NAND PLACE_SIDE=TOP 14
TOP SIDE PP9442 P4MM SM (PP) 1 =PP1V8_NAND PLACE_SIDE=TOP 14 57 62
TOP SIDE PP9443 P4MM SM (PP) 1 GND PLACE_SIDE=TOP

## EE

TOP SIDE PP9450 P4MM SM (PP) 1 RESET_SOC_L 4 13 25 47 57 60 67
PP9451 P4MM SM (PP) 1 TP_ANALOGMUXOUT 4
TOP SIDE PP9452 P4MM SM (PP) 1 SOCHOT0_R_L 58

| | | |
|---|---|---|
| | TP_GPIO_DFU_STATUS | FUNC_TEST=TRUE 5 |

## CAMERA

PP9470 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_CLK_P PLACE_NEAR=U0600.AM35:3MM 7 22 61 65
NO_XNET_CONNECTION=TRUE
PP9471 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_CLK_N PLACE_NEAR=U0600.AM36:3MM 7 22 61 65
NO_XNET_CONNECTION=TRUE
PP9472 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_DATA_P<0> PLACE_NEAR=U0600.AN35:3MM 7 22 61 65
NO_XNET_CONNECTION=TRUE
PP9473 P4MM SM (PP) 1 MIPI1C_CAM_FRONT_DATA_N<0> PLACE_NEAR=U0600.AN36:3MM 7 22 61 65
NO_XNET_CONNECTION=TRUE
PP9474 P4MM SM (PP) 1 MIPI0C_CAM_REAR_CLK_P PLACE_NEAR=U0600.AR31:3MM 7 23 61 65
NO_XNET_CONNECTION=TRUE
PP9475 P4MM SM (PP) 1 MIPI0C_CAM_REAR_CLK_N PLACE_NEAR=U0600.AT31:3MM 7 23 61 65
NO_XNET_CONNECTION=TRUE
PP9476 P4MM SM (PP) 1 MIPI0C_CAM_REAR_DATA_P<0> PLACE_NEAR=U0600.AR33:3MM 7 23 61 65
NO_XNET_CONNECTION=TRUE
PP9477 P4MM SM (PP) 1 MIPI0C_CAM_REAR_DATA_N<0> PLACE_NEAR=U0600.AT33:3MM 7 23 61 65
NO_XNET_CONNECTION=TRUE

FOR FRANK (SEG)

PP9400 P4MM SM (PP) 1 PPVDD_SOC_SOC_SENSE PLACE_NEAR=U0600.V31:1MM 10 57 67
PP9401 P4MM SM (PP) 1 PPVDD_CPU_SOC_SENSE PLACE_NEAR=U0600.AL31:1MM 11 57 67
PP9402 P4MM SM (PP) 1 PPVDD_GPU_SOC_SENSE PLACE_NEAR=U0600.AA7:1MM 11 57 67

## DRAM

### NEAR DRAM

PP9410 P4MM SM (PP) 1 DDR0_CK_N PLACE_NEAR=U1400.AF14:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9411 P4MM SM (PP) 1 DDR0_CK_P PLACE_NEAR=U1400.AF15:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9412 P4MM SM (PP) 1 DDR0_CKE<0> PLACE_NEAR=U1400.AF16:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9413 P4MM SM (PP) 1 DDR0_CKE<1> PLACE_NEAR=U1400.AE17:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9414 P4MM SM (PP) 1 DDR0_CA<0> PLACE_NEAR=U1400.AE21:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9415 P4MM SM (PP) 1 DDR0_DQ<2> PLACE_NEAR=U1400.B18:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9416 P4MM SM (PP) 1 DDR0_DQS_N<3> PLACE_NEAR=U1400.C8:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9417 P4MM SM (PP) 1 DDR0_DQS_P<3> PLACE_NEAR=U1400.B8:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9418 P4MM SM (PP) 1 DDR0_DQS_N<0> PLACE_NEAR=U1400.C15:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9419 P4MM SM (PP) 1 DDR0_DQS_P<0> PLACE_NEAR=U1400.B15:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

PP9420 P4MM SM (PP) 1 DDR1_CK_N PLACE_NEAR=U1400.T26:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9421 P4MM SM (PP) 1 DDR1_CK_P PLACE_NEAR=U1400.R26:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9422 P4MM SM (PP) 1 DDR1_CKE<0> PLACE_NEAR=U1400.P26:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9423 P4MM SM (PP) 1 DDR1_CKE<1> PLACE_NEAR=U1400.N25:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9424 P4MM SM (PP) 1 DDR1_CA<0> PLACE_NEAR=U1400.J25:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9425 P4MM SM (PP) 1 DDR1_CA<1> PLACE_NEAR=U1400.K26:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9426 P4MM SM (PP) 1 DDR1_CA<2> PLACE_NEAR=U1400.K25:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9427 P4MM SM (PP) 1 DDR1_CA<3> PLACE_NEAR=U1400.L25:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9428 P4MM SM (PP) 1 DDR1_CSN<0> PLACE_NEAR=U1400.N35:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

### NEAR SOC

PP9435 P4MM SM (PP) 1 DDR0_DQ<28> PLACE_NEAR=U0600.D5:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9436 P4MM SM (PP) 1 DDR0_DQS_N<3> PLACE_NEAR=U0600.A6:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE
PP9437 P4MM SM (PP) 1 DDR0_DQS_P<3> PLACE_NEAR=U0600.A5:1MM 8 12 61 66
NO_XNET_CONNECTION=TRUE

## GRAPE

CONVERT TO PROBE POINTS IF NOT ABLE TO PLACE TESTPOINT

| | | |
|---|---|---|
| | TP_JTAG_CUMULUS_M_TCK | 52 64 |
| | TP_JTAG_CUMULUS_M_TDI | 52 64 |
| | JTAG_CUMULUS_M_TMS | 52 64 |
| | TP_JTAG_CUMULUS_M_TDO | 52 64 |
| | DISPLAY_SYNC | 4 52 60 |
| | CUMULUS_MS_CK | 52 64 |
| | CUMULUS_MS_SD | 52 64 |
| | GPIO_GRAPE2SOC_IRQ_L | 5 52 60 |
| | GPIO_SOC2GRAPE_RESET_L | 5 52 60 67 |
| | CLK_32K_SOC2CUMULUS | 5 52 60 64 |
| | SPI2_GRAPE_MOSI | 5 52 60 64 |
| | SPI2_GRAPE_MISO | 5 52 60 64 |
| | SPI2_GRAPE_SCLK | 5 52 60 64 |
| | SPI2_GRAPE_CS_L | 5 52 60 64 |
| | TP_CUMULUS_S_H_CS_L | 52 |
| | TP_CUMULUS_S_H_SCLK | 52 |
| | TP_CUMULUS_S_H_SDI | 52 |
| | TP_CUMULUS_S_H_SDO | 52 |
| | =PP5V25_GRAPE | 52 62 |
| | PP1V8_GRAPE_SW | 51 52 60 67 |

GRAPE NO_TEST

| | | |
|---|---|---|
| | MT_PANEL_IN<0..29> | NO_TEST=TRUE 52 65 |
| | MT_PANEL_OUT<0..39> | NO_TEST=TRUE 52 65 |

## AUDIO

| | | |
|---|---|---|
| | L81_DMIC1_FF_SD | FUNC_TEST=TRUE 15 |

## WIFI

| | | |
|---|---|---|
| | JTAG_WLAN_TMS_TX_BLANK | FUNC_TEST=TRUE 46 64 |
| | TP_JTAG_WLAN_TCK | FUNC_TEST=TRUE 46 64 |
| | JTAG_WLAN_TDI_OSCAR_A | FUNC_TEST=TRUE 46 64 |
| | JTAG_WLAN_TDO_OSCAR_B | FUNC_TEST=TRUE 46 64 |
| | TP_JTAG_WLAN_TRST_L | FUNC_TEST=TRUE 46 64 |
| | JTAG_WLAN_SEL | FUNC_TEST=TRUE 46 |
| | UART2_SOC2WLAN_TX_R | FUNC_TEST=TRUE 46 64 |
| | UART2_WLAN2SOC_TX_R | FUNC_TEST=TRUE 46 64 |
| | UART_BB2WLAN_LTE_COEX_R | FUNC_TEST=TRUE 46 |
| | UART_WLAN2BB_LTE_COEX_R | FUNC_TEST=TRUE 46 |
| | =PP3V3_S2R_WIFI_PA | FUNC_TEST=TRUE 46 62 |
| | HSIC1_SOC2WLAN_HOST_RDY_R | FUNC_TEST=TRUE 46 64 |
| | HSIC1_WLAN2SOC_DEVICE_RDY | FUNC_TEST=TRUE 5 46 64 |
| | HSIC1_WLAN2SOC_REMOTE_WAKE | FUNC_TEST=TRUE 5 46 64 |

FOR HSIC CHARACTERIZATION

PP9480 P4MM SM (PP) 1 HSIC1_WLAN_DATA PLACE_NEAR=U0600.A27:3MM 4 46 61 64
PP9481 P4MM SM (PP) 1 HSIC1_WLAN_STB PLACE_NEAR=U0600.B27:3MM 4 46 61 64
PP9482 P4MM SM (PP) 1 HSIC1_WLAN_DATA PLACE_NEAR=U5800.13:3MM 4 46 61 64
PP9483 P4MM SM (PP) 1 HSIC1_WLAN_STB PLACE_NEAR=U5800.14:3MM 4 46 61 64

| | | |
|---|---|---|
| | PMU_GPIO_WLAN_REG_ON | FUNC_TEST=TRUE 46 57 |
| | PMU_GPIO_BT_REG_ON | FUNC_TEST=TRUE 46 57 |
| | GPIO_BT_WAKE | FUNC_TEST=TRUE 5 46 |

## BASEBAND

| | | |
|---|---|---|
| | BB_JTAG_TMS | FUNC_TEST=TRUE 5 25 28 64 |
| | BB_JTAG_TCK | FUNC_TEST=TRUE 5 25 28 64 |
| | BB_JTAG_TDI | FUNC_TEST=TRUE 5 25 28 64 |
| | BB_JTAG_TDO | FUNC_TEST=TRUE 5 25 28 64 |
| | BB_JTAG_TRST_L | FUNC_TEST=TRUE 5 25 28 64 |
| | USB_BB_DEBUG_P | FUNC_TEST=TRUE 25 28 64 |
| | USB_BB_DEBUG_N | FUNC_TEST=TRUE 25 28 64 |
| | DEBUG_RST_L | FUNC_TEST=TRUE 25 28 67 |
| | PMU_GPIO_BB_VBUS_DET | FUNC_TEST=TRUE 25 28 57 67 |

FOR HSIC CHARACTERIZATION

PP9485 P4MM SM (PP) 1 HSIC2_BB_DATA PLACE_NEAR=U0600.AJ35:3MM 4 25 28 61 64
PP9486 P4MM SM (PP) 1 HSIC2_BB_STB PLACE_NEAR=U0600.AJ36:3MM 4 25 28 61 64
PP9487 P4MM SM (PP) 1 HSIC2_BB_DATA PLACE_NEAR=U3400.C7:3MM 4 25 28 61 64
PP9488 P4MM SM (PP) 1 HSIC2_BB_STB PLACE_NEAR=U3400.B8:3MM 4 25 28 61 64

# HIGH SPEED, NO TEST

| | | |
|---|---|---|
| | DDR0_CA<0..9> | NO_TEST=TRUE 8 12 61 66 |
| | DDR0_CK_P | NO_TEST=TRUE 8 12 61 66 |
| | DDR0_CK_N | NO_TEST=TRUE 8 12 61 66 |
| | DDR0_CA<0..9> | NO_TEST=TRUE 8 12 61 66 |
| | DDR0_CKE<0..1> | NO_TEST=TRUE 8 12 61 66 |
| | DDR0_CSN<0..1> | NO_TEST=TRUE 8 12 66 |
| | DDR0_DM<0..3> | NO_TEST=TRUE 8 12 66 |
| | DDR0_DQ<0..31> | NO_TEST=TRUE 8 12 61 66 |
| | DDR0_DQS_P<0..3> | NO_TEST=TRUE 8 12 61 66 |
| | DDR0_DQS_N<0..3> | NO_TEST=TRUE 8 12 61 66 |
| | DDR1_CA<0..9> | NO_TEST=TRUE 8 12 61 66 |
| | DDR1_CK_P | NO_TEST=TRUE 8 12 61 66 |
| | DDR1_CK_N | NO_TEST=TRUE 8 12 61 66 |
| | DDR1_CA<0..9> | NO_TEST=TRUE 8 12 61 66 |
| | DDR1_CKE<0..1> | NO_TEST=TRUE 8 12 61 66 |
| | DDR1_CSN<0..1> | NO_TEST=TRUE 8 12 66 |
| | DDR1_DM<0..3> | NO_TEST=TRUE 8 12 66 |
| | DDR1_DQ<0..31> | NO_TEST=TRUE 8 12 66 |
| | DDR1_DQS_P<0..3> | NO_TEST=TRUE 8 12 66 |
| | DDR1_DQS_N<0..3> | NO_TEST=TRUE 8 12 66 |

| | | |
|---|---|---|
| | MIPI0C_CAM_REAR_CLK_P | NO_TEST=TRUE 7 23 61 65 |
| | MIPI0C_CAM_REAR_CLK_N | NO_TEST=TRUE 7 23 61 65 |
| | MIPI0C_CAM_REAR_DATA_P<0..1> | NO_TEST=TRUE 7 23 61 65 |
| | MIPI0C_CAM_REAR_DATA_N<0..1> | NO_TEST=TRUE 7 23 61 65 |
| | MIPI0C_CAM_REAR_CLK_FILT_P | NO_TEST=TRUE 23 65 |
| | MIPI0C_CAM_REAR_CLK_FILT_N | NO_TEST=TRUE 23 65 |
| | MIPI0C_CAM_REAR_DATA_FILT_P<0..3> | NO_TEST=TRUE 23 65 |
| | MIPI0C_CAM_REAR_DATA_FILT_N<0..3> | NO_TEST=TRUE 23 65 |
| | MIPI1C_CAM_FRONT_CLK_P | NO_TEST=TRUE 7 22 61 65 |
| | MIPI1C_CAM_FRONT_CLK_N | NO_TEST=TRUE 7 22 61 65 |
| | MIPI1C_CAM_FRONT_DATA_P<0> | NO_TEST=TRUE 7 22 61 65 |
| | MIPI1C_CAM_FRONT_DATA_N<0> | NO_TEST=TRUE 7 22 61 65 |
| | MIPI1C_CAM_FRONT_CLK_FILT_P | NO_TEST=TRUE 22 65 |
| | MIPI1C_CAM_FRONT_CLK_FILT_N | NO_TEST=TRUE 22 65 |
| | MIPI1C_CAM_FRONT_DATA_FILT_P<0> | NO_TEST=TRUE 22 65 |
| | MIPI1C_CAM_FRONT_DATA_FILT_N<0> | NO_TEST=TRUE 22 65 |

| | | |
|---|---|---|
| | EDP_DATA_P<0..3> | NO_TEST=TRUE 7 53 65 |
| | EDP_DATA_N<0..3> | NO_TEST=TRUE 7 53 65 |
| | EDP_DATA_EMI_P<0..3> | NO_TEST=TRUE 53 65 |
| | EDP_DATA_EMI_N<0..3> | NO_TEST=TRUE 53 65 |
| | EDP_DATA_EMI_CONN_P<0..3> | NO_TEST=TRUE 53 65 |
| | EDP_DATA_EMI_CONN_N<0..3> | NO_TEST=TRUE 53 65 |

# POWER, NO TEST

| | | |
|---|---|---|
| | PP6V0_LCM_HI | NO_TEST=TRUE 56 67 |
| | SW_CHGA | NO_TEST=TRUE 55 67 |
| | WLED_LX_A | NO_TEST=TRUE 56 67 |
| | WLED_LX_B | NO_TEST=TRUE 56 67 |
| | L81_PVCP | NO_TEST=TRUE 15 65 |
| | L81_NVCP | NO_TEST=TRUE 15 65 |

CHARGE PUMP OUTPUTS

| | | |
|---|---|---|
| | L81_FLYC | NO_TEST=TRUE 15 65 |
| | L81_FLYN | NO_TEST=TRUE 15 65 |
| | L81_FLYP | NO_TEST=TRUE 15 65 |
| | THROTTLER_OUT | NO_TEST=TRUE 58 |
| | UVLO_COMP_NEG | NO_TEST=TRUE 58 |
| | UVLO_COMP_POS | NO_TEST=TRUE 58 |
| | UVLO_COMP_REF | NO_TEST=TRUE 58 |
| | VCC_MAIN_UVLO_SENSE | NO_TEST=TRUE 58 |

# NO TEST DUE TO LAYOUT

I2C3 TP AT ALS FILTER SIDE

| | | |
|---|---|---|
| | I2C3_SCL_1V8 | NO_TEST=TRUE 5 13 22 64 |
| | I2C3_SDA_1V8 | NO_TEST=TRUE 5 13 22 64 |
| | MAX98304_L1_IN_N | NO_TEST=TRUE 18 65 |
| | MAX98304_L1_IN_P | NO_TEST=TRUE 18 65 |
| | MAX98304_R1_IN_N | NO_TEST=TRUE 17 65 |
| | MAX98304_R1_IN_P | NO_TEST=TRUE 17 65 |
| | MAX98304_L2_IN_N | NO_TEST=TRUE 18 65 |
| | MAX98304_L2_IN_P | NO_TEST=TRUE 18 65 |
| | MAX98304_R2_IN_N | NO_TEST=TRUE 17 65 |
| | MAX98304_R2_IN_P | NO_TEST=TRUE 17 65 |
| | GPIO_BTN_HOME_CONN_R_L | NO_TEST=TRUE 50 |

# NO TEST ON PROX

| | | |
|---|---|---|
| | PROX_AD7149_CIN5 | NO_TEST=TRUE 45 |
| | PROX_AD7149_CIN7 | NO_TEST=TRUE 45 |
| | PROX_AD7149_CIN9 | NO_TEST=TRUE 45 |
| | PROX_AD7149_CIN7_FILT | NO_TEST=TRUE 45 |
| | PROX_AD7149_CIN9_FILT | NO_TEST=TRUE 45 |
| | PROX_AD7149_CIN7_CONN | NO_TEST=TRUE 45 |
| | PROX_AD7149_CIN9_CONN | NO_TEST=TRUE 45 |
| | PROX_AD7149_ACSHIELD_CONN | NO_TEST=TRUE 45 |
| | PROX_AD7149_BIAS | NO_TEST=TRUE 45 |
| | ACSHIELD_SB | NO_TEST=TRUE 45 |
| | ACSH_SB | NO_TEST=TRUE 45 |
| | PROX_AD7149_GPIO | NO_TEST=TRUE 45 |

# POWER CONNECTIONS

## BUCK0

67 60 55 PPVDD_CPU (MAKE_BASE=TRUE) = =PPVDD_CPU 11

## BUCK1

67 60 55 PPVDD_GPU (MAKE_BASE=TRUE) = =PPVDD_GPU 11

## BUCK2

67 60 55 PPVDD_SOC (MAKE_BASE=TRUE) = =PPVDD_SOC 10

## BUCK3

67 60 56 55 PP1V8_S2R (MAKE_BASE=TRUE) = =PP1V8_S2R_MISC 5 59
= =PP1V8_S2R_VDDIO_WLAN_BT 46
= =PP1V8_S2R_TRISTAR 47
= =PP1V8_S2R_DDR 12
= =PP1V8_S2R_GRAPE 51
= =PP1V8_S2R_EXT_SWITCH 57

## BUCK3_SW

67 60 59 57 55 PP1V8_SW1 (MAKE_BASE=TRUE) = =PP1V8_AUDIO 15
XWC130 SM 1 2 PP1V8_SW1_FOREHEAD 60 62 67
67 62 60 PP1V8_SW1_FOREHEAD (MAKE_BASE=TRUE) = =PP1V8_DMIC 16
= =PP1V8_CAM_FRONT 22
= =PP1V8_CAM_REAR 23
= =PP1V8_PROX_AD7149 45

67 60 57 PP1V8_EXT_SW (MAKE_BASE=TRUE) = =PP1V8_VDDIO18_SOC 9 10
= =PP1V8_SOC 4 5 7 13 58
= =PP1V8_MIPI_SOC 7
= =PP1V8_EDP_SOC 7
= =PP1V8_NAND_SOC 6
= =PP1V8_NAND 14 57 61
= =PP1V8_PLL_SOC 4
= =PP1V8_EEPROM 5

67 60 55 PP1V8_SW2 (MAKE_BASE=TRUE) = =PP1V8_GRAPE 51

67 60 55 PP1V8_S2R_SW3 (MAKE_BASE=TRUE) = =PP1V8_S2R_GYRO 19
= =PP1V8_S2R_ACCEL 19
= =PP1V8_S2R_OSCAR 19
XWC133 SM 1 2 PP1V8_S2R_SW3_COMP 60 62 67
67 62 60 PP1V8_S2R_SW3_COMP (MAKE_BASE=TRUE) = =PP1V8_S2R_COMP 24

## BUCK4

67 60 56 55 PP1V2_S2R (MAKE_BASE=TRUE) = =PP1V2_S2R_DDR 12
= =PP1V2_S2R_DDR_SOC 8

## BUCK4_SW

67 60 55 PP1V2_SW1 (MAKE_BASE=TRUE) = =PP1V2_VDDQ_DDR 12
= =PP1V2_VDDIOD_SOC 8 9
= =PP1V2_HSIC_SOC 4

67 60 55 PP1V2_S2R_SW2 (MAKE_BASE=TRUE) = =PP1V2_S2R_OSCAR 19

## BUCK5

67 60 55 PPVDD_SRAM (MAKE_BASE=TRUE) = =PPVDD_SRAM_CPU 10
= =PPVDD_SRAM_SOC 10

## BUCK6

67 60 55 PP3V3_S2R (MAKE_BASE=TRUE) = =PP3V3_S2R_SWITCH 57
= =PP3V3_S2R_WIFI_PA 46 61

67 60 57 PP3V3_SW (MAKE_BASE=TRUE) = =PP3V3_EDP_PU
= =PP3V3_NAND 14
= =PP3V3_USB_SOC 4

## LDO1

67 60 56 PP3V0_SPARE1 (MAKE_BASE=TRUE) = =PP3V0_SPARE1 58

## LDO2

67 60 56 PP1V7_VA_VCP (MAKE_BASE=TRUE) = =PP1V7_VA_VCP 15

## LDO3

67 60 56 PP3V0_S2R_SENSOR (MAKE_BASE=TRUE) = =PP3V0_S2R_GYRO 19
= =PP3V0_S2R_ACCEL 19
= =PP3V0_S2R_COMP 24

## LDO4

67 60 56 PP3V0_ALS (MAKE_BASE=TRUE) = =PP3V0_ALS 22
= =PP3V0_PROX_AD7149 45

## LDO5

67 60 56 PP3V0_UVLO (MAKE_BASE=TRUE) = =PP3V0_UVLO 58

## LDO6

67 60 56 PP3V3_ACC (MAKE_BASE=TRUE) = =PP3V3_ACC 47

## LDO7

67 60 56 PP3V0_S2R_TRISTAR (MAKE_BASE=TRUE) = =PP3V0_S2R_TRISTAR 47

## LDO8

67 60 56 PP3V0_S2R_HALL (MAKE_BASE=TRUE) = =PP3V0_S2R_HALL 50

## LDO9

BACKUP RAIL. CAN BE BOOSTED TO MEET 1.1V MIN ON CAMERA IF NEEDED.

67 60 56 PP1V3_CAM (MAKE_BASE=TRUE) = =PP1V3_CAM_REAR 23

## LDO10

67 60 56 PP1V0_SOC (MAKE_BASE=TRUE) = =PP1V0_USB_SOC 4
= =PP1V0_MIPI_SOC 7
= =PP1V0_EDP_PAD_DVDD_SOC 7

## LDO011

67 60 56 PP2V6_CAM_AF (MAKE_BASE=TRUE) = =PP2V6_CAM_REAR_AF 23

## LDO013

67 60 56 PP2V9_CAM (MAKE_BASE=TRUE) = =PP2V9_CAM_FRONT 22
= =PP2V9_CAM_REAR 23

## VLCM1

67 60 56 PP5V25_GRAPE (MAKE_BASE=TRUE) = =PP5V25_GRAPE 52 61

## CHARGER MAIN

67 60 58 57 56 55 47 PPVCC_MAIN (MAKE_BASE=TRUE) = =PPVCC_MAIN_AUDIO 15
= =PPVCC_MAIN_LED 56
= =PPVCC_MAIN_CPU 55
= =PPVCC_MAIN_GPU 55
= =PPVCC_MAIN_SOC 55
= =PPVCC_MAIN_GRAPE 51
= =PPVCC_MAIN_LCD 53
= =PPVCC_MAIN_VDD_LCM 56
= =PPVCC_MAIN_WLAN 46

## BATTERY

67 60 55 PPBATT_VCC (MAKE_BASE=TRUE) = =PPBATT_POS_CONN 54
= =PPBATT_VCC_BB 25 26 34 35 36 37 38 39 40
= =PPBATT_AUDIO 17 18

## USB POWER INPUT

67 60 55 PPVBUS_USB_DCIN (MAKE_BASE=TRUE) = =PPVBUS_USB_EMI 48

## ON_BUF

67 60 56 PP1V8_ALWAYS (MAKE_BASE=TRUE) = =PP1V8_ALWAYS 5

## BACKLIGHT BOOST

67 60 56 PPLED_OUT_A (MAKE_BASE=TRUE) = =PPLED_REG_A 53

67 60 56 PPLED_OUT_B (MAKE_BASE=TRUE) = =PPLED_REG_B 53

# Clock Signal Constraints

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| CLK_50S | * | 45_OHM_SE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| CLK | * | * | 3:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | |
|---|---|---|---|
| B6 | CLK_50S | CLK | CLK_32K_SOC2CUMULUS 5 52 60 61 |
| B5 | CLK_50S | CLK | CLK_32K_SOC2CUMULUS_FILT 60 |
| B4 | CLK_50S | CLK | CUMULUS_MS_CK 52 61 |
| B3 | CLK_50S | CLK | CUMULUS_MS_SD 52 61 |
| | | | |
| B12 | CLK_50S | CLK | PMU_GPIO_CLK_32K_WLAN 46 57 |
| B11 | CLK_50S | CLK | PMU_GPIO_CLK_32K_OSCAR 19 57 60 |
| B7 | CLK_50S | CLK | PMU_OUT_32K_CLK_GPS 57 68 |
| | | | |
| B9 | CLK_50S | CLK | ISP1_CAM_FRONT_CLK_R 7 |
| B8 | CLK_50S | CLK | ISP1_CAM_FRONT_CLK 7 22 |
| B10 | CLK_50S | CLK | ISP1_CAM_FRONT_CLK_F 22 60 |
| | | | |
| B2 | CLK_50S | CLK | ISP0_CAM_REAR_CLK_R 7 |
| A10 | CLK_50S | CLK | ISP0_CAM_REAR_CLK 7 23 |
| A11 | CLK_50S | CLK | ISP0_CAM_REAR_CLK_F 23 60 |

# UART

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| UART_50S | * | 45_OHM_SE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| UART | * | * | 3:1_SPACING |
| UART | UART | * | 2:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | |
|---|---|---|---|
| B14 | UART_50S | UART | UART0_SOC_RXD 5 47 60 |
| B13 | UART_50S | UART | UART0_SOC_TXD 5 47 60 |
| B16 | UART_50S | UART | UART3_SOC2BB_RTS_L 5 25 29 |
| B15 | UART_50S | UART | UART3_BB2SOC_RTS_L 5 25 29 |
| B17 | UART_50S | UART | UART3_SOC2BB_TX 5 25 29 47 |
| B18 | UART_50S | UART | UART3_BB2SOC_TX 5 25 29 47 |
| B19 | UART_50S | UART | UART4_OSCAR2SOC_RXD 5 19 |
| B20 | UART_50S | UART | UART4_SOC2OSCAR_TXD 5 19 |
| B21 | UART_50S | UART | UART1_SOC2BT_RTS_L 5 46 |
| B22 | UART_50S | UART | UART1_BT2SOC_RTS_L 5 46 |
| B23 | UART_50S | UART | UART1_SOC2BT_TX 5 46 |
| B24 | UART_50S | UART | UART1_BT2SOC_TX 5 46 |
| B25 | UART_50S | UART | UART2_SOC2WLAN_TX 5 46 |
| B26 | UART_50S | UART | UART2_WLAN2SOC_TX 5 46 |
| B27 | UART_50S | UART | UART2_SOC2WLAN_TX_R 46 61 |
| B28 | UART_50S | UART | UART2_WLAN2SOC_TX_R 46 61 |
| B29 | UART_50S | UART | UART6_TS_ACC_RXD 5 47 |
| B30 | UART_50S | UART | UART6_TS_ACC_TXD 5 47 |
| B31 | | UART | UART5_BATT_TRXD 5 54 57 |
| B32 | | UART | BATT_SWI_CONN 54 60 |

# I2S

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| I2S_50S | * | 45_OHM_SE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| I2S | * | * | 3:1_SPACING |
| I2S | I2S | * | 2:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | |
|---|---|---|---|
| A37 | I2S_50S | CLK | I2S0_CODEC_ASP_MCK_R 5 15 |
| A38 | I2S_50S | CLK | I2S0_CODEC_ASP_MCK 5 |
| A40 | I2S_50S | I2S | I2S0_CODEC_ASP_BCLK 5 15 |
| A43 | I2S_50S | I2S | I2S0_CODEC_ASP_LRCK 5 15 |
| A42 | I2S_50S | I2S | I2S0_CODEC_ASP_DIN 5 15 |
| A41 | I2S_50S | I2S | I2S0_CODEC_ASP_DOUT 5 15 |
| A39 | I2S_50S | I2S | I2S0_CODEC_ASP_SDOUT 15 |
| | | | |
| A61 | I2S_50S | I2S | NC_I2S1_MCK 5 |
| A65 | I2S_50S | I2S | I2S1_CODEC_XSP_BCLK 5 15 |
| A64 | I2S_50S | I2S | I2S1_CODEC_XSP_LRCK 5 15 |
| A59 | I2S_50S | I2S | I2S1_CODEC_XSP_DIN 5 15 |
| A63 | I2S_50S | I2S | I2S1_CODEC_XSP_DOUT 5 15 |
| A60 | I2S_50S | I2S | I2S1_CODEC_XSP_SDOUT 15 |
| | | | |
| A234 | I2S_50S | CLK | NC_I2S2_MCK_R |
| A235 | I2S_50S | CLK | NC_I2S2_MCK 5 |
| A276 | I2S_50S | I2S | NC_I2S2_BCLK 5 |
| A277 | I2S_50S | I2S | NC_I2S2_LRCK 5 |
| A278 | I2S_50S | I2S | NC_I2S2_DIN 5 |
| A279 | I2S_50S | I2S | NC_I2S2_DOUT 5 |
| | | | |
| A280 | I2S_50S | I2S | NC_I2S4_MCK 5 |
| A281 | I2S_50S | I2S | I2S4_SOC2BT_BCLK 5 46 |
| A280 | I2S_50S | I2S | I2S4_SOC2BT_LRCK 5 46 |
| A282 | I2S_50S | I2S | I2S4_SOC2BT_DATA 5 46 |
| A283 | I2S_50S | I2S | I2S4_BT2SOC_DATA 5 46 |

# DWI

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DWI | * | * | 2:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | |
|---|---|---|---|
| A152 | | DWI | DWI_AP_CLK 5 57 |
| A224 | | DWI | NC_DWI_AP_DI 57 |
| A156 | | DWI | DWI_AP_DO 5 57 |

# I2C

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| I2C_50S | * | 45_OHM_SE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| I2C | * | * | 1.5:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | |
|---|---|---|---|
| B1 | I2C_50S | I2C | I2C0_SDA_1V8 5 57 60 |
| B0 | I2C_50S | I2C | I2C0_SCL_1V8 5 57 60 |
| B1 | I2C_50S | I2C | I2C3_CAM_ALS_SDA_1V8_F 22 60 |
| B0 | I2C_50S | I2C | I2C3_CAM_ALS_SCL_1V8_F 22 60 |
| B1 | I2C_50S | I2C | I2C0_HP_ALS_SDA_1V8_FILT 60 |
| B0 | I2C_50S | I2C | I2C0_HP_ALS_SCL_1V8_FILT 60 |
| | | | |
| B13 | I2C_50S | I2C | I2C1_SOC2OSCAR_SWDCLK_1V8 5 19 |
| B12 | I2C_50S | I2C | I2C1_SOC2OSCAR_SWDIO_1V8 5 19 |
| | | | |
| B3 | I2C_50S | I2C | I2C2_SDA_1V8 5 47 |
| B2 | I2C_50S | I2C | I2C2_SCL_1V8 5 47 |
| | | | |
| B15 | I2C_50S | I2C | I2C3_SDA_1V8 5 13 22 61 |
| B14 | I2C_50S | I2C | I2C3_SCL_1V8 5 13 22 61 |
| | | | |
| | | | |
| B11 | I2C_50S | I2C | DMIC1_FF_SD_FILT 16 60 |
| B10 | I2C_50S | I2C | DMIC1_FF_SCLK_FILT 16 60 |
| B17 | I2C_50S | I2C | DMIC1_FF_SD 15 16 |
| B16 | I2C_50S | I2C | DMIC1_FF_SCLK 15 16 |
| | | | |
| B21 | I2C_50S | I2C | SEP_I2C0_SCL 5 |
| B20 | I2C_50S | I2C | SEP_I2C0_SDA 5 |
| | | | |
| B6 | I2C_50S | I2C | ISP0_CAM_REAR_SCL 7 23 |
| B5 | I2C_50S | I2C | ISP0_CAM_REAR_SDA 7 23 |
| B18 | I2C_50S | I2C | ISP0_CAM_REAR_SCL_F 23 60 |
| B19 | I2C_50S | I2C | ISP0_CAM_REAR_SDA_F 23 60 |
| | | | |
| B23 | I2C_50S | I2C | ISP1_CAM_FRONT_SCL 7 22 |
| B24 | I2C_50S | I2C | ISP1_CAM_FRONT_SDA 7 22 |
| B25 | I2C_50S | I2C | ISP1_CAM_FRONT_SCL_F 22 60 |
| B26 | I2C_50S | I2C | ISP1_CAM_FRONT_SDA_F 22 60 |

# SPI

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| SPI_50S | * | 45_OHM_SE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SPI | * | * | 2:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | |
|---|---|---|---|
| B30 | SPI_50S | SPI | SPI3_CODEC_MISO 5 15 |
| B31 | SPI_50S | SPI | SPI3_CODEC_MOSI 5 15 |
| B33 | SPI_50S | SPI | SPI3_CODEC_SCLK 5 15 |
| B34 | SPI_50S | SPI | SPI3_CODEC_CS_L 5 15 |
| | | | |
| | | | |
| B35 | SPI_50S | SPI | SPI2_GRAPE_MISO 5 52 60 61 64 |
| B36 | SPI_50S | SPI | SPI2_GRAPE_MOSI 5 52 60 61 64 |
| B37 | SPI_50S | SPI | SPI2_GRAPE_SCLK 5 52 60 61 64 |
| B38 | SPI_50S | SPI | SPI2_GRAPE_CS_L 5 52 60 61 64 |
| | | | |
| | | | |
| B35 | SPI_50S | SPI | SPI2_GRAPE_MISO 5 52 60 61 64 |
| B36 | SPI_50S | SPI | SPI2_GRAPE_MOSI 5 52 60 61 64 |
| B37 | SPI_50S | SPI | SPI2_GRAPE_SCLK 5 52 60 61 64 |
| B38 | SPI_50S | SPI | SPI2_GRAPE_CS_L 5 52 60 61 64 |
| | | | |
| B27 | SPI_50S | SPI | SPI_OSCAR_MISO 19 24 |
| B28 | SPI_50S | SPI | SPI_OSCAR_MOSI 19 24 |
| B29 | SPI_50S | SPI | SPI_OSCAR_SCLK 19 24 |
| B32 | SPI_50S | SPI | SPI_OSCAR_MISO_GYRO 19 |
| B31 | SPI_50S | SPI | SPI_OSCAR_MISO_ACCEL 19 |
| B30 | SPI_50S | SPI | SPI_OSCAR_MISO_COMP1 24 |
| | | | |
| B24 | SPI_50S | SPI | SPI_OSCAR_MOSI_R 19 |
| B25 | SPI_50S | SPI | SPI_OSCAR_SCLK_R 19 |
| B26 | SPI_50S | SPI | SPI_OSCAR2ACCEL_CS_L 19 |
| B33 | SPI_50S | SPI | SPI_OSCAR2GYRO_CS_L 19 |
| B39 | SPI_50S | | SPI_OSCAR2COMPASS_CS_L 19 24 |

# JTAG

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| JTAG | * | * | 2:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | |
|---|---|---|---|
| B14 | | JTAG | JTAG_SOC_TCK 4 47 60 |
| B13 | | JTAG | JTAG_SOC_TMS 4 47 60 |
| B15 | | JTAG | JTAG_SOC_TDI 4 60 |
| B12 | | JTAG | TP_JTAG_SOC_TDO 4 60 |
| B16 | | RST | JTAG_SOC_TRST_L 4 13 60 |
| B10 | | JTAG | NC_JTAG_SOC_TRTCK 4 |
| B19 | | JTAG | BB_JTAG_TMS 5 25 28 61 |
| B18 | | JTAG | BB_JTAG_TCK 5 25 28 61 |
| B17 | | JTAG | BB_JTAG_TDO 5 25 28 61 |
| B21 | | JTAG | BB_JTAG_TDI 5 25 28 61 |
| B20 | | RST | BB_JTAG_TRST_L 5 25 28 61 |
| B23 | | JTAG | JTAG_WLAN_TMS_TX_BLANK 46 61 |
| B22 | | JTAG | TP_JTAG_WLAN_TCK 46 61 |
| B24 | | JTAG | JTAG_WLAN_TDO_OSCAR_B 46 61 |
| B25 | | JTAG | JTAG_WLAN_TDI_OSCAR_A 46 61 |
| B26 | | RST | TP_JTAG_WLAN_TRST_L 46 61 |
| B27 | | JTAG | TP_JTAG_CUMULUS_M_TCK 52 61 |
| B28 | | JTAG | TP_JTAG_CUMULUS_M_TDI 52 61 |
| B29 | | JTAG | JTAG_CUMULUS_M_TMS 52 61 |
| B30 | | JTAG | TP_JTAG_CUMULUS_M_TDO 52 61 |

# USB

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| USB_90D | * | 90_OHM_DIFF |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| USB | * | * | 4:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | |
|---|---|---|---|
| B6 | USB_90D | USB | USB_SOC_P 4 47 60 |
| B5 | USB_90D | USB | USB_SOC_N 4 47 60 |
| B34 | USB_90D | USB | USB_BB_P 25 47 |
| B33 | USB_90D | USB | USB_BB_N 25 47 |
| B36 | USB_90D | USB | USB_BB_DEBUG_P 25 28 61 |
| B35 | USB_90D | USB | USB_BB_DEBUG_N 25 28 61 |
| | | | |
| B39 | USB_90D | USB | E75_DPAIR1_CONN_P 47 49 60 |
| B38 | USB_90D | USB | E75_DPAIR1_CONN_N 47 49 60 |
| B41 | USB_90D | USB | E75_DPAIR2_CONN_P 47 49 60 |
| B40 | USB_90D | USB | E75_DPAIR2_CONN_N 47 49 60 |
| B43 | USB_90D | USB | E75_DPAIR1_P 47 |
| B42 | USB_90D | USB | E75_DPAIR1_N 47 |
| B45 | USB_90D | USB | E75_DPAIR2_P 47 |
| B44 | USB_90D | USB | E75_DPAIR2_N 47 |

# HSIC

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| HSIC | * | 45_OHM_SE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| HSIC | * | * | 4:1_SPACING |
| HSIC | GND | * | 1.5:1_SPACING |
| HSIC_RDY | * | * | 2:1_SPACING |
| HSIC_RDY | GND | * | 1.5:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | |
|---|---|---|---|
| B101 | HSIC | HSIC | HSIC1_WLAN_DATA 4 46 61 |
| B104 | HSIC | HSIC | HSIC1_WLAN_STB 4 46 61 |
| B103 | HSIC | HSIC | HSIC2_BB_DATA 4 25 28 61 |
| B102 | HSIC | HSIC | HSIC2_BB_STB 4 25 28 61 |
| B107 | HSIC | HSIC | NC_HSIC0_DATA 4 |
| B106 | HSIC | HSIC | NC_HSIC0_STB 4 |
| | | | |
| B105 | HSIC | HSIC_RDY | HSIC1_WLAN2SOC_REMOTE_WAKE 5 46 61 |
| B108 | HSIC | HSIC_RDY | HSIC1_WLAN2SOC_DEVICE_RDY 5 46 61 |
| B227 | HSIC | HSIC_RDY | HSIC1_SOC2WLAN_HOST_RDY 5 46 |
| B279 | HSIC | HSIC_RDY | HSIC1_SOC2WLAN_HOST_RDY_R 46 61 |
| | | | |
| B100 | HSIC | HSIC_RDY | HSIC2_BB2SOC_REMOTE_WAKE 5 29 |
| B109 | HSIC | HSIC_RDY | HSIC2_BB2SOC_DEVICE_RDY 5 25 29 |
| B106 | HSIC | HSIC_RDY | HSIC2_SOC2BB_HOST_RDY 5 25 29 |

## MIPI

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| MIPI_90D | * | 90_OHM_DIFF |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MIPI0C | * | * | 4:1_SPACING |
| MIPI1C | * | * | 4:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_CLK_P | 7 23 61 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_CLK_N | 7 23 61 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_DATA_P<0> | 7 23 61 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_DATA_N<0> | 7 23 61 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_DATA_P<1> | 7 23 61 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_DATA_N<1> | 7 23 61 |
| | MIPI_90D | MIPI0C | NC_MIPI0C_CAM_REAR_DATA_P<2> | 7 |
| | MIPI_90D | MIPI0C | NC_MIPI0C_CAM_REAR_DATA_N<2> | 7 |
| | MIPI_90D | MIPI0C | NC_MIPI0C_CAM_REAR_DATA_P<3> | 7 |
| | MIPI_90D | MIPI0C | NC_MIPI0C_CAM_REAR_DATA_N<3> | 7 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_CLK_FILT_P | 23 61 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_CLK_FILT_N | 23 61 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_DATA_FILT_P<0> | 23 61 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_DATA_FILT_N<0> | 23 61 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_DATA_FILT_P<1> | 23 61 |
| | MIPI_90D | MIPI0C | MIPI0C_CAM_REAR_DATA_FILT_N<1> | 23 61 |
| | MIPI_90D | MIPI0C | NC_MIPI0C_CAM_REAR_DATA_FILT_P<2> | |
| | MIPI_90D | MIPI0C | NC_MIPI0C_CAM_REAR_DATA_FILT_N<2> | |
| | MIPI_90D | MIPI0C | NC_MIPI0C_CAM_REAR_DATA_FILT_P<3> | |
| | MIPI_90D | MIPI0C | NC_MIPI0C_CAM_REAR_DATA_FILT_N<3> | |
| | MIPI_90D | MIPI1C | MIPI1C_CAM_FRONT_CLK_P | 7 22 61 |
| | MIPI_90D | MIPI1C | MIPI1C_CAM_FRONT_CLK_N | 7 22 61 |
| | MIPI_90D | MIPI1C | MIPI1C_CAM_FRONT_DATA_P<0> | 7 22 61 |
| | MIPI_90D | MIPI1C | MIPI1C_CAM_FRONT_DATA_N<0> | 7 22 61 |
| | MIPI_90D | MIPI1C | NC_MIPI1C_CAM_FRONT_DATA_P<1> | 7 |
| | MIPI_90D | MIPI1C | NC_MIPI1C_CAM_FRONT_DATA_N<1> | 7 |
| | MIPI_90D | MIPI1C | MIPI1C_CAM_FRONT_CLK_FILT_P | 22 61 |
| | MIPI_90D | MIPI1C | MIPI1C_CAM_FRONT_CLK_FILT_N | 22 61 |
| | MIPI_90D | MIPI1C | MIPI1C_CAM_FRONT_DATA_FILT_P<0> | 22 61 |
| | MIPI_90D | MIPI1C | MIPI1C_CAM_FRONT_DATA_FILT_N<0> | 22 61 |
| | MIPI_90D | MIPI1C | NC_MIPI0D_DPCLK | 7 |
| | MIPI_90D | MIPI1C | NC_MIPI0D_DNCLK | 7 |
| | MIPI_90D | MIPI1C | NC_MIPI0D_DPDATA0 | 7 |
| | MIPI_90D | MIPI1C | NC_MIPI0D_DNDATA0 | 7 |
| | MIPI_90D | MIPI1C | NC_MIPI0D_DPDATA1 | 7 |
| | MIPI_90D | MIPI1C | NC_MIPI0D_DNDATA1 | 7 |
| | MIPI_90D | MIPI1C | NC_MIPI0D_DPDATA2 | 7 |
| | MIPI_90D | MIPI1C | NC_MIPI0D_DNDATA2 | 7 |
| | MIPI_90D | MIPI1C | NC_MIPI0D_DPDATA3 | 7 |
| | MIPI_90D | MIPI1C | NC_MIPI0D_DNDATA3 | 7 |
| | MIPI_90D | MIPI0C | MIPI_CAM0_CLKCON_P | |
| | MIPI_90D | MIPI0C | MIPI_CAM0_CLKCON_N | |
| | MIPI_90D | MIPI0C | MIPI_CAM0_D0CON_P | |
| | MIPI_90D | MIPI0C | MIPI_CAM0_D0CON_N | |
| | MIPI_90D | MIPI0C | MIPI_CAM0_D1CON_P | |
| | MIPI_90D | MIPI0C | MIPI_CAM0_D1CON_N | |
| | MIPI_90D | MIPI0C | MIPI_CAM0_D2CON_P | |
| | MIPI_90D | MIPI0C | MIPI_CAM0_D2CON_N | |
| | MIPI_90D | MIPI0C | MIPI_CAM0_D3CON_P | |
| | MIPI_90D | MIPI0C | MIPI_CAM0_D3CON_N | |
| | MIPI_90D | MIPI1C | MIPI_CAM1_CLKCON_P | |
| | MIPI_90D | MIPI1C | MIPI_CAM1_CLKCON_N | |
| | MIPI_90D | MIPI1C | MIPI_CAM1_D0CON_P | |
| | MIPI_90D | MIPI1C | MIPI_CAM1_D0CON_N | |
| | MIPI_90D | MIPI1C | MIPI_CAM1_D1CON_P | |
| | MIPI_90D | MIPI1C | MIPI_CAM1_D1CON_N | |

DEV

## BACKLIGHT

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| LED | * | LED |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| LEDA | * | * | 2.4:1_SPACING |
| LEDB | * | * | 2.4:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| | LED | LEDA | LED_IO1_A_R | 56 |
| | LED | LEDB | LED_IO1_B_R | 56 |
| | LED | LEDA | LED_IO2_A_R | 56 |
| | LED | LEDB | LED_IO2_B_R | 56 |
| | LED | LEDA | LED_IO3_A_R | 56 |
| | LED | LEDB | LED_IO3_B_R | 56 |
| | LED | LEDA | LED_IO4_A_R | 56 |
| | LED | LEDB | LED_IO4_B_R | 56 |
| | LED | LEDA | LED_IO5_A_R | 56 |
| | LED | LEDB | LED_IO5_B_R | 56 |
| | LED | LEDA | LED_IO6_A_R | 56 |
| | LED | LEDB | LED_IO6_B_R | 56 |
| | LED | LEDA | LED_IO_1_A | 53 56 60 |
| | LED | LEDB | LED_IO_1_B | 53 56 60 |
| | LED | LEDA | LED_IO_2_A | 53 56 60 |
| | LED | LEDB | LED_IO_2_B | 53 56 60 |
| | LED | LEDA | LED_IO_3_A | 53 56 60 |
| | LED | LEDB | LED_IO_3_B | 53 56 60 |
| | LED | LEDA | LED_IO_4_A | 53 56 60 |
| | LED | LEDB | LED_IO_4_B | 53 56 60 |
| | LED | LEDA | LED_IO_5_A | 53 56 60 |
| | LED | LEDB | LED_IO_5_B | 53 56 60 |
| | LED | LEDA | LED_IO_6_A | 53 56 60 |
| | LED | LEDB | LED_IO_6_B | 53 56 60 |

## AUDIO/SPEAKER

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| AUDIO | * | * | 3:1_SPACING |
| AUDIO | AUDIO | * | 2:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| | SPKR_DIFF | SPEAKER | AUDIO | SPKRAMP_L1_OUT_P | 18 49 60 |
| | SPKR_DIFF | SPEAKER | AUDIO | SPKRAMP_L1_OUT_N | 18 49 60 |
| | SPKR_DIFF | SPEAKER | AUDIO | SPKRAMP_L2_OUT_P | 18 49 60 |
| | SPKR_DIFF | SPEAKER | AUDIO | SPKRAMP_L2_OUT_N | 18 49 60 |
| | SPKR_DIFF | SPEAKER | AUDIO | SPKRAMP_R1_OUT_P | 17 49 60 |
| | SPKR_DIFF | SPEAKER | AUDIO | SPKRAMP_R1_OUT_N | 17 49 60 |
| | SPKR_DIFF | SPEAKER | AUDIO | SPKRAMP_R2_OUT_P | 17 49 60 |
| | SPKR_DIFF | SPEAKER | AUDIO | SPKRAMP_R2_OUT_N | 17 49 60 |
| | | USB_90D | USB | MIKEY_TS_P | 15 47 |
| | | USB_90D | USB | MIKEY_TS_N | 15 47 |
| MAXIMUM_NECK_LENGTH=0.5 MM MIN_NECK_WIDTH=0.06 MM | | USB_90D | USB | L81_MBUS_P | 15 |
| | | USB_90D | USB | L81_MBUS_N | 15 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | LEFT_CH_OUT_P | 15 18 60 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | LEFT_CH_OUT_N | 15 18 60 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | RIGHT_CH_OUT_P | 15 17 60 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | RIGHT_CH_OUT_N | 15 17 60 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | MAX98304_L1_IN_P | 18 61 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | MAX98304_L1_IN_N | 18 61 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | MAX98304_R1_IN_P | 17 61 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | MAX98304_R1_IN_N | 17 61 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | MAX98304_L2_IN_P | 18 61 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | MAX98304_L2_IN_N | 18 61 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | MAX98304_R2_IN_P | 17 61 |
| | SPKR_DIFF | AUDIO_DIFF | AUDIO | MAX98304_R2_IN_N | 17 61 |
| | | AUDIO_DIFF | AUDIO | SPKR_L1_VSNS_P | |
| | | AUDIO_DIFF | AUDIO | SPKR_L1_VSNS_N | |
| | | AUDIO_DIFF | AUDIO | SPKR_R1_VSNS_P | |
| | | AUDIO_DIFF | AUDIO | SPKR_R1_VSNS_N | |
| MAXIMUM_NECK_LENGTH=15 MM | | PWR_0P5MM | AUDIO | CODEC_HP_HS3 | 15 |
| | | PWR_0P5MM | AUDIO | CODEC_HP_HS4 | 15 |
| | | PWR_0P5MM | AUDIO | CONN_HP_HS3_FILT | 15 16 60 |
| | | PWR_0P5MM | AUDIO | CONN_HP_HS4_FILT | 15 16 60 |
| | | PWR_0P2MM | AUDIO | CODEC_HP_LEFT | 15 |
| | | PWR_0P2MM | AUDIO | CODEC_HP_RIGHT | 15 |
| | | PWR_0P2MM | AUDIO | CONN_HP_LEFT_FILT | 15 16 60 |
| | | PWR_0P2MM | AUDIO | CONN_HP_RIGHT_FILT | 15 16 60 |
| | PP_PWR | PWR | | L81_NVCP | 15 61 |
| | PP_PWR | PWR | | L81_PVCP | 15 61 |
| | PP_PWR | PWR | | L81_FLYP | 15 61 |
| | PP_PWR | PWR | | L81_FLYN | 15 61 |
| | PP_PWR | PWR | | L81_FLYC | 15 61 |
| | PP_PWR | PWR | | SPEAKER_VQ | |
| | PP_PWR | PWR | | L81_FILT | 15 |
| | | PWR_0P1MM | AUDIO | HP_MIC_POS | 15 |
| | | PWR_0P1MM | AUDIO | HP_MIC_NEG | 15 |
| | | PWR_0P1MM | AUDIO | L81_AIN2_POS | 15 |
| | | PWR_0P1MM | AUDIO | L81_AIN2_NEG | 15 |
| | | PWR_0P1MM | AUDIO | CODEC_HP_HS3_REF | 15 |
| | | PWR_0P1MM | AUDIO | CODEC_HP_HS4_REF | 15 |
| | | PWR_0P1MM | AUDIO | CONN_HP_HS3_REF_FILT | 15 16 60 |
| | | PWR_0P1MM | AUDIO | CONN_HP_HS4_REF_FILT | 15 16 60 |

## XTAL

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| CRYSTAL | * | * | 5:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| | | CRYSTAL | XTAL_SOC_24M_I | 4 |
| | | CRYSTAL | XTAL_SOC_24M_O | 4 |
| | | CRYSTAL | SOC_24M_O | 4 |
| | | CRYSTAL | PMU_XTAL | 56 |
| | | CRYSTAL | PMU_EXTAL | 56 |

## EMBEDDED DISPLAYPORT

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| EDP_90D | * | 90_OHM_DIFF |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| EDP_50S | * | 45_OHM_SE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| EDP | * | * | 4:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| | EDP_90D | EDP | EDP_AUX_P | 7 53 |
| | EDP_90D | EDP | EDP_AUX_N | 7 53 |
| | EDP_50S | EDP | EDP_HPD | 7 53 |
| EDP | EDP_90D | EDP | EDP_DATA_P<0> | 7 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_N<0> | 7 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_P<1> | 7 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_N<1> | 7 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_P<2> | 7 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_N<2> | 7 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_P<3> | 7 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_N<3> | 7 53 61 |
| | EDP_90D | EDP | EDP_AUX_EMI_P | 53 |
| | EDP_90D | EDP | EDP_AUX_EMI_N | 53 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_P<0> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_N<0> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_P<1> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_N<1> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_P<2> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_N<2> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_P<3> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_N<3> | 53 61 |
| | EDP_90D | EDP | EDP_AUX_EMI_CONN_P | 53 |
| | EDP_90D | EDP | EDP_AUX_EMI_CONN_N | 53 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_CONN_P<0> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_CONN_N<0> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_CONN_P<1> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_CONN_N<1> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_CONN_P<2> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_CONN_N<2> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_CONN_P<3> | 53 61 |
| EDP | EDP_90D | EDP | EDP_DATA_EMI_CONN_N<3> | 53 61 |

## TEMP SENSORS

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| BOARD_TEMP | * | TEMP_SENSE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| BOARD_TEMP | * | * | 3:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| MIN_NECK_WIDTH=0.053 MM | BOARD_TEMP | BOARD_TEMP | PA_NTC_P | 57 60 |
| MIN_NECK_WIDTH=0.053 MM | BOARD_TEMP | BOARD_TEMP | PA_NTC_N | 57 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP2_P | 57 60 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP2_N | 57 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP3_P | 57 60 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP3_N | 57 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP4_P | 57 60 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP4_N | 57 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP5_P | 57 60 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP5_N | 57 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP6_P | 57 60 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP6_N | 57 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP7_P | 57 60 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP7_N | 57 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP8_P | 57 60 |
| | BOARD_TEMP | BOARD_TEMP | BOARD_TEMP8_N | 57 |

## GRAPE

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| GRAPE | * | GRAPE_SE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GRAPE | * | * | 2:1_SPACING |

NET_TYPE

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| | GRAPE | GRAPE | MT_PANEL_IN<0..29> | 52 61 |
| | GRAPE | GRAPE | MT_PANEL_OUT<0..39> | 52 61 |

## DDR

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| DDR_50S | * | DRAM_SE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DDR | * | * | 3:1_SPACING |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| DDR_90D | * | DRAM_DIFF |

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| | DDR_50S | DDR | DDR0_CA<0> | 8 12 61 |
| | DDR_50S | DDR | DDR0_CA<9..1> | 8 12 61 |
| | DDR_50S | DDR | DDR0_DM<3..0> | 8 12 61 |
| | DDR_90D | DDR | DDR0_CK_P | 8 12 61 |
| | DDR_90D | DDR | DDR0_CK_N | 8 12 61 |
| | DDR_50S | DDR | DDR0_CKE<1..0> | 8 12 61 |
| | DDR_50S | DDR | DDR0_CSN<1..0> | 8 12 61 |
| | | DDR | DDR0_CA_ZQ_SOC | 8 |
| | | DDR | DDR0_DQ_ZQ_SOC | 8 |
| | | DDR | DDR0_ZQ_DRAM | 12 |
| | DDR_50S | DDR | DDR0_DQ<1..0> | 8 12 61 |
| | DDR_50S | DDR | DDR0_DQ<2> | 8 12 61 |
| | DDR_50S | DDR | DDR0_DQ<7..3> | 8 12 61 |
| | DDR_90D | DDR | DDR0_DQS_P<0> | 8 12 61 |
| | DDR_90D | DDR | DDR0_DQS_N<0> | 8 12 61 |
| | DDR_50S | DDR | DDR0_DQ<15..8> | 8 12 61 |
| | DDR_90D | DDR | DDR0_DQS_P<1> | 8 12 61 |
| | DDR_90D | DDR | DDR0_DQS_N<1> | 8 12 61 |
| | DDR_50S | DDR | DDR0_DQ<23..16> | 8 12 61 |
| | DDR_90D | DDR | DDR0_DQS_P<2> | 8 12 61 |
| | DDR_90D | DDR | DDR0_DQS_N<2> | 8 12 61 |
| | DDR_50S | DDR | DDR0_DQ<27..25> | 8 12 61 |
| | DDR_50S | DDR | DDR0_DQ<28> | 8 12 61 |
| | DDR_50S | DDR | DDR0_DQ<31..29> | 8 12 61 |
| | DDR_90D | DDR | DDR0_DQS_P<3> | 8 12 61 |
| | DDR_90D | DDR | DDR0_DQS_N<3> | 8 12 61 |
| | DDR_50S | DDR | DDR1_CA<3..0> | 8 12 61 |
| | DDR_50S | DDR | DDR1_CA<9..4> | 8 12 61 |
| | DDR_50S | DDR | DDR1_DM<3..0> | 8 12 61 |
| | DDR_90D | DDR | DDR1_CK_P | 8 12 61 |
| | DDR_90D | DDR | DDR1_CK_N | 8 12 61 |
| | DDR_50S | DDR | DDR1_CKE<1..0> | 8 12 61 |
| | DDR_50S | DDR | DDR1_CSN<0> | 8 12 61 |
| | DDR_50S | DDR | DDR1_CSN<1> | 8 12 61 |
| | | DDR | DDR1_CA_ZQ_SOC | 8 |
| | | DDR | DDR1_DQ_ZQ_SOC | 8 |
| | | DDR | DDR1_ZQ_DRAM | 12 |
| | DDR_50S | DDR | DDR1_DQ<7..0> | 8 12 61 |
| | DDR_90D | DDR | DDR1_DQS_P<0> | 8 12 61 |
| | DDR_90D | DDR | DDR1_DQS_N<0> | 8 12 61 |
| | DDR_50S | DDR | DDR1_DQ<15..8> | 8 12 61 |
| | DDR_90D | DDR | DDR1_DQS_P<1> | 8 12 61 |
| | DDR_90D | DDR | DDR1_DQS_N<1> | 8 12 61 |
| | DDR_50S | DDR | DDR1_DQ<23..16> | 8 12 61 |
| | DDR_90D | DDR | DDR1_DQS_P<2> | 8 12 61 |
| | DDR_90D | DDR | DDR1_DQS_N<2> | 8 12 61 |
| | DDR_50S | DDR | DDR1_DQ<31..24> | 8 12 61 |
| | DDR_90D | DDR | DDR1_DQS_P<3> | 8 12 61 |
| | DDR_90D | DDR | DDR1_DQS_N<3> | 8 12 61 |

## VREF (DDR/FMI)

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| VREF | * | * | 5:1_SPACING |

| VOLTAGE | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| MIN_NECK_WIDTH=0.15 MM | | | | |
| 0.6V | PP_PWR | PWR | PPVREF_DDR0_CA_SOC | 8 |
| 0.6V | PP_PWR | PWR | PPVREF_DDR0_DQ_SOC | 8 |
| 0.6V | PP_PWR | PWR | PPVREF_DDR1_CA_SOC | 8 |
| 0.6V | PP_PWR | PWR | PPVREF_DDR1_DQ_SOC | 8 |
| 0.6V | PP_PWR | PWR | PPVREF_DDR0_CA_DRAM | 12 |
| 0.6V | PP_PWR | PWR | PPVREF_DDR0_DQ_DRAM | 12 |
| 0.6V | PP_PWR | PWR | PPVREF_DDR1_CA_DRAM | 12 |
| 0.6V | PP_PWR | PWR | PPVREF_DDR1_DQ_DRAM | 12 |
| 0.9V | PP_PWR | VREF | PPVREF_FMI_SOC | 6 61 |
| 0.9V | PP_PWR | VREF | PPVREF_FMI_NAND | 14 61 |

## NAND

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| NAND_50S | * | 45_OHM_SE |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| NAND | * | * | 3:1_SPACING |

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| | FMI0_AD_CTRL_PP | NAND_50S | NAND | FMI0_AD<0> | 6 14 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_AD<1> | 6 14 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_AD<2> | 6 14 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_AD<3> | 6 14 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_AD<4> | 6 14 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_AD<5> | 6 14 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_AD<6> | 6 14 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_AD<7> | 6 14 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_ALE | 6 14 61 |
| | FMI0_CE | NAND_50S | NAND | FMI0_CE0_L | 6 14 60 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_CLE | 6 14 61 |
| | | NAND_50S | NAND | FMI0_DQS | 6 14 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_RE_L | 6 14 61 |
| | FMI0_AD_CTRL | NAND_50S | NAND | FMI0_WE_L | 6 14 61 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_AD<0> | 6 14 61 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_AD<1> | 6 14 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_AD<2> | 6 14 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_AD<3> | 6 14 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_AD<4> | 6 14 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_AD<5> | 6 14 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_AD<6> | 6 14 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_AD<7> | 6 14 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_ALE | 6 14 61 |
| | FMI1_CE | NAND_50S | NAND | FMI1_CE0_L | 6 14 61 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_CLE | 6 14 61 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_DQS | 6 14 61 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_RE_L | 6 14 61 |
| | FMI1_AD_CTRL | NAND_50S | NAND | FMI1_WE_L | 6 14 61 |

## NAND DEV

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | |
|---|---|---|---|
| | NAND_50S | NAND | FMI0_AD_BUF<0> |
| | NAND_50S | NAND | FMI0_AD_BUF<1> |
| | NAND_50S | NAND | FMI0_AD_BUF<2> |
| | NAND_50S | NAND | FMI0_AD_BUF<3> |
| | NAND_50S | NAND | FMI0_AD_BUF<4> |
| | NAND_50S | NAND | FMI0_AD_BUF<5> |
| | NAND_50S | NAND | FMI0_AD_BUF<6> |
| | NAND_50S | NAND | FMI0_AD_BUF<7> |
| | NAND_50S | NAND | FMI0_ALE_BUF |
| | NAND_50S | NAND | FMI0_CE0_BUF_L |
| | NAND_50S | NAND | FMI0_CLE_BUF |
| | NAND_50S | NAND | FMI0_DQS_BUF |
| | NAND_50S | NAND | FMI0_DQSN_BUF |
| | NAND_50S | NAND | FMI0_REP_BUF |
| | NAND_50S | NAND | FMI0_RE_BUF_L |
| | NAND_50S | NAND | FMI0_WE_BUF_L |
| | NAND_50S | NAND | FMI1_AD_BUF<0> |
| | NAND_50S | NAND | FMI1_AD_BUF<1> |
| | NAND_50S | NAND | FMI1_AD_BUF<2> |
| | NAND_50S | NAND | FMI1_AD_BUF<3> |
| | NAND_50S | NAND | FMI1_AD_BUF<4> |
| | NAND_50S | NAND | FMI1_AD_BUF<5> |
| | NAND_50S | NAND | FMI1_AD_BUF<6> |
| | NAND_50S | NAND | FMI1_AD_BUF<7> |
| | NAND_50S | NAND | FMI1_ALE_BUF |
| | NAND_50S | NAND | FMI1_CE0_BUF_L |
| | NAND_50S | NAND | FMI1_CLE_BUF |
| | NAND_50S | NAND | FMI1_DQS_BUF |
| | NAND_50S | NAND | FMI1_DQSN_BUF |
| | NAND_50S | NAND | FMI1_REP_BUF |
| | NAND_50S | NAND | FMI1_RE_BUF_L |
| | NAND_50S | NAND | FMI1_WE_BUF_L |

## PWR

| VOLTAGE | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| | | | BUCKS | |
| 4.7V | PP_PWR | PWR | BUCK0_LX0 | 55 |
| 4.7V | PP_PWR | PWR | BUCK0_LX1 | 55 |
| 4.7V | PP_PWR | PWR | BUCK0_LX2 | 55 |
| 4.7V | PP_PWR | PWR | BUCK0_LX3 | 55 |
| 1.1V | PP_PWR | PWR | BUCK0_FB | 55 |
| 4.7V | PP_PWR | PWR | BUCK1_LX0 | 55 |
| 4.7V | PP_PWR | PWR | BUCK1_LX1 | 55 |
| 4.7V | PP_PWR | PWR | BUCK1_LX2 | 55 |
| 1.1V | PP_PWR | PWR | BUCK1_FB | 55 |
| 4.7V | PP_PWR | PWR | BUCK2_LX0 | 55 |
| 1.0V | PP_PWR | PWR | BUCK2_FB | 55 |
| 4.7V | PP_PWR | PWR | BUCK3_LX0 | 55 |
| 1.8V | PP_PWR | PWR | BUCK3_FB | 55 |
| 4.7V | PP_PWR | PWR | BUCK4_LX0 | 55 |
| 1.2V | PP_PWR | PWR | BUCK4_FB | 55 |
| 4.7V | PP_PWR | PWR | BUCK5_LX0 | 55 |
| 1.0V | PP_PWR | PWR | BUCK5_FB | 55 |
| 4.7V | PP_PWR | PWR | BUCK6_LX0 | 55 |
| 3.3V | PP_PWR | PWR | BUCK6_FB | 55 |
| | | | RAILS | |
| 1.1V | MIN_NECK_WIDTH=0.15 MM PWR_15MM | PWR | PPVDD_CPU | 55 60 62 |
| 1.1V | MIN_NECK_WIDTH=0.15 MM PWR_10MM | PWR | PPVDD_GPU | 55 60 62 |
| 1.0V | MIN_NECK_WIDTH=0.15 MM PWR_2MM | PWR | PPVDD_SOC | 55 60 62 |
| 1.8V | MAXIMUM_NECK_LENGTH=5 MM PP_PWR | PWR | PP1V8_S2R | 55 56 60 62 |
| 1.8V | MAX_LINE_WIDTH=0.6 MM PWR_0P5MM | PWR | PP1V8_SW1 | 55 57 59 60 62 |
| 1.8V | MAXIMUM_NECK_LENGTH=10 MM PWR_0P5MM | PWR | PP1V8_SW1_FOREHEAD | 60 62 |
| 1.8V | MIN_NECK_WIDTH=0.15 MM PP_PWR | PWR | PP1V8_EXT_SW | 57 60 62 |
| 1.8V | PWR_0P1MM | PWR | PP1V8_SW2 | 55 60 62 |
| 1.8V | PP_PWR | PWR | PP1V8_S2R_SW3 | 55 60 62 |
| 1.8V | MAX_LINE_WIDTH=0.5 MM MAXIMUM_NECK_LENGTH=10 MM PWR_0P3MM | PWR | PP1V8_S2R_SW3_COMP | 60 62 |
| 1.2V | MAXIMUM_NECK_LENGTH=5 MM PP_PWR | PWR | PP1V2_S2R | 55 56 60 62 |
| 1.2V | PWR_1MM | PWR | PP1V2_SW1 | 55 60 62 |
| 1.2V | MAXIMUM_NECK_LENGTH=15 MM PP_PWR | PWR | PP1V2_S2R_SW2 | 55 60 62 |
| 3.3V | MIN_NECK_WIDTH=0.1 MM PWR_1MM | PWR | PPVDD_SRAM | 55 60 62 |
| 3.3V | PWR_1P2MM | PWR | PP3V3_S2R | 55 60 62 |
| 3.3V | MAXIMUM_NECK_LENGTH=15 MM PP_PWR | PWR | PP3V3_SW | 57 60 62 |
| | | | LDOS | |
| 3.0V | MAXIMUM_NECK_LENGTH=20 MM PP_PWR | PWR | PP3V0_SPARE1 | 56 60 62 |
| 1.7V | PP_PWR | PWR | PP1V7_VA_VCP | 56 60 62 |
| 3.0V | MAX_LINE_WIDTH=0.5 MM MAXIMUM_NECK_LENGTH=10 MM PWR_0P3MM | PWR | PP3V0_S2R_SENSOR | 56 60 62 |
| 3.0V | MAXIMUM_NECK_LENGTH=10 MM PWR_0P3MM | PWR | PP3V0_ALS | 56 60 62 |
| 3.0V | PWR_0P4MM | PWR | PP3V0_UVLO | 56 60 62 |
| 3.3V | PP_PWR | PWR | PP3V3_ACC | 56 60 62 |
| 3.0V | PWR_0P3MM | PWR | PP3V0_S2R_TRISTAR | 56 60 62 |
| 3.0V | PWR_0P3MM | PWR | PP3V0_S2R_HALL | 56 60 62 |
| 1.3V | MAXIMUM_NECK_LENGTH=7 MM PP_PWR | PWR | PP1V3_CAM | 56 60 62 |
| 1.0V | MAXIMUM_NECK_LENGTH=15 MM PP_PWR | PWR | PP1V0_SOC | 56 60 62 |
| 2.6V | MAXIMUM_NECK_LENGTH=45 MM PP_PWR | PWR | PP2V6_CAM_AF | 56 60 62 |
| 2.9V | MAXIMUM_NECK_LENGTH=40 MM PP_PWR | PWR | PP2V9_CAM | 56 60 62 |
| 5.25V | MAXIMUM_NECK_LENGTH=5 MM PP_PWR | PWR | PP5V25_GRAPE | 56 60 62 |
| | | | INPUT/MAIN/ALWAYS | |
| 4.7V | MIN_NECK_WIDTH=0.15 MM PWR_15MM | PWR | PPVCC_MAIN | 47 55 56 57 58 60 62 |
| 4.7V | MAXIMUM_NECK_LENGTH=15 MM PWR_10MM | PWR | PPBATT_VCC | 55 60 62 |
| 6.0V | PWR_2MM | PWR | PPVBUS_USB_DCIN | 55 60 62 |
| 1.8V | MAX_LINE_WIDTH=0.6 MM PWR_0P2MM | PWR | PP1V8_ALWAYS | 56 60 62 |
| 4.7V | PWR_10MM | PWR | PPBATT_AUDIO_AMP | |
| | | | PMU | |
| 20.4V | PP_PWR | PWR | WLED_LX_B | 56 61 |
| 20.4V | PP_PWR | PWR | WLED_LX_A | 56 61 |
| 20.4V | MAX_LINE_WIDTH=0.6 MM PWR_0P5MM | PWR | PPLED_OUT_A | 56 60 62 |
| 20.4V | MAX_LINE_WIDTH=0.6 MM PWR_0P5MM | PWR | PPLED_OUT_B | 56 60 62 |
| 20.4V | PWR_PMU | PWR | PPLED_BACK_REG_A | 53 60 |
| 20.4V | PWR_PMU | PWR | PPLED_BACK_REG_B | 53 60 |
| 6.0V | PP_PWR | PWR | PP6V0_LCM_VBOOST | 56 60 |
| 6.0V | PWR_0P2MM | PWR | PPVBUS_PROT | 47 55 60 |
| 6.0V | PP_PWR | PWR | PMU_VCENTER | 55 60 |
| 6.0V | PP_PWR | PWR | PP6V0_LCM_HI | 56 61 |
| 20.4V | PP_PWR | PWR | LCM_LX | 56 |
| 4.7V | PP_PWR | PWR | SW_CHGA | 55 61 |
| 6.0V | PWR_0P2MM | PWR | USB_VBUS_DETECT | 4 55 |
| 6.0V | PWR_0P2MM | PWR | USB_VBUS_DETECT_R | 4 |
| 6.0V | | PWR | PMU_GPIO_BB_VBUS_DET | 25 28 57 61 |

| VOLTAGE | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| 1.8V | PP_PWR | PWR | PP1V8_PLL_SOC_F | 4 |
| 1.8V | PP_PWR | PWR | PP1V8_EDP_AVDD_AUX | 7 |
| 0.4V | PP_PWR | PWR | TP_PP0V4_MIPI0D | 7 |
| 0.4V | PP_PWR | PWR | TP_PP0V4_MIPI1D | 7 |
| 1.8V | PWR_0P2MM | PWR | PP1V8_XTAL | 9 |
| 1.8V | PP_PWR | PWR | PP1V8_VDD_ANA_TMPSADC | 10 |
| 1.2V | PP_PWR | PWR | PPVDDI_NAND | 14 |
| 1.8V | PP_PWR | PWR | PP1V8_DMIC_FILT | 16 60 |
| 3.0V | PP_PWR | PWR | PP3V0_HP_ALS_FILT | 60 |
| 8.75V | PP_PWR | PWR | SPKR_L1_SWITCH | |
| 8.75V | PP_PWR | PWR | SPKR_R1_SWITCH | |
| 1.8V | PP_PWR | PWR | PPDVDD_SPKRAMP | |
| 1.7V | PP_PWR | PWR | PP1V7_VCP | 15 60 |
| 4.2V | PP_PWR | PWR | PPVCC_VPROG_CP | 15 |
| 4.2V | PP_PWR | PWR | PPVCC_VPROG_MB | |
| 4.2V | PP_PWR | PWR | PPVCC_VPROG_MB_F | 15 |
| 4.7V | PWR_1MM | PWR | PPVCC_MAIN_LCD_SW | 53 60 |
| 4.7V | PWR_1MM | PWR | PPVCC_MAIN_LCD_SW_CONN | 53 60 |
| 4.7V | PWR_1MM | PWR | PPVCC_MAIN_GRAPE_FILT | |
| 5.25V | PP_PWR | PWR | PP5V25_GRAPE_FILT | |
| 1.8V | PP_PWR | PWR | PP1V8_GRAPE_SW | 51 52 60 61 |
| 1.8V | PP_PWR | PWR | PP1V8_GRAPE_FILT | |
| 3.0V | PP_PWR | PWR | PP3V0_GYRO | 19 60 |
| 3.0V | PP_PWR | PWR | PP3V0_ACCEL | 19 60 |
| 3.0V | PWR_0P3MM | PWR | PP3V0_S2R_HALL_FILT | 20 50 60 |
| 1.2V | PWR_0P3MM | PWR | PP1V2_CAM_FRONT_FILT | 60 |
| 1.8V | PP_PWR | PWR | PP1V8_CAM_FRONT_FILT | 22 60 |
| 2.9V | PP_PWR | PWR | PP2V9_AVDD_CAM_FRONT_FILT | 22 60 |
| 3.0V | PWR_0P3MM | PWR | PP3V0_ALS_FILT | 22 60 |
| 2.6V | PP_PWR | PWR | PP2V6_CAM_REAR_AF_FILT | 23 60 |
| 1.28V | PP_PWR | PWR | PP1V3_CAM_REAR_FILT | 23 60 |
| 1.8V | PP_PWR | PWR | PP1V8_CAM_REAR_FILT | 23 60 |
| 1.28V | PP_PWR | PWR | PP1V3_CAM_REAR | |
| 2.8V | PP_PWR | PWR | PP2V9_AVDD_CAM_REAR_FILT | 23 60 |
| 3.0V | PP_PWR | PWR | PP3V0_COMP | 24 60 |
| 1.8V | PP_PWR | PWR | PP1V8_COMP | 24 60 |
| 3.0V | PP_PWR | PWR | PP3V0_SENSOR_PROX_FILT | 60 |
| 3.0V | PP_PWR | PWR | PP3V0_SENSOR_PROX_ADUX1049_FILT | 60 |
| 3.0V | PP_PWR | PWR | PPAVDD_SENSOR_PROX_ADUX1049 | |
| 3.0V | PP_PWR | PWR | PP3V0_SENSOR_PROX_AD7149_FILT | 45 60 |
| 6.0V | PWR_2MM | PWR | PPVBUS_E75_USB_CONN | 48 49 60 |
| 3.3V | PP_PWR | PWR | PPOUT_E75_ACC_ID1_CONN | 48 49 60 |
| 3.3V | PP_PWR | PWR | PPOUT_E75_ACC_ID2_CONN | 48 49 60 |
| 3.3V | PP_PWR | PWR | PPOUT_E75_ACC_ID1 | 47 48 |
| 3.3V | PP_PWR | PWR | PPOUT_E75_ACC_ID2 | 47 48 |
| 3.0V | PP_PWR | PWR | PP3V0_IO_ALS_FILT | 60 |
| | | ANLG | BATT_NTC | 54 57 60 |
| | MAXIMUM_NECK_LENGTH=20 MM PP_PWR | ANLG | BATT_SNS | 54 55 |
| | MAXIMUM_NECK_LENGTH=5 MM PP_PWR | ANLG | BATT_SNS_R | 55 |

## GND

| VOLTAGE | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| 0V | MAX_LINE_WIDTH=0.6 MM GND | GND | GND_AUDIO_CODEC | 15 60 |
| 0V | MAX_LINE_WIDTH=0.6 MM GND | GND | GND_AVDD_CAM_FRONT | 22 |
| 0V | MAX_LINE_WIDTH=0.6 MM GND | GND | GND_PP1V8_CAM_FRONT | 22 |
| 0V | MAX_LINE_WIDTH=0.6 MM GND | GND | GND_PP2V9_CAM_FRONT | 22 |
| 0V | MAX_LINE_WIDTH=0.6 MM GND | GND | GND_COMP | 24 |
| 0V | GND | GND | GND_PMU | |
| 0V | GND | GND | GND_SPKR_AMP_L1 | |
| 0V | GND | GND | GND_SPKR_AMP_L2 | |
| 0V | GND | GND | GND_SPKR_AMP_R1 | |
| 0V | GND | GND | GND_SPKR_AMP_R2 | |

## RST

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| RST | * | * | 3:1_SPACING |

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| | | RST | BB_TRST_L | |
| | | RST | DBG_RST | DEV |
| | | RST | DEBUG_RST_L | 25 28 61 |
| | | RST | GSM_TXBURST_IND | |
| | | RST | RST_AP_1V8_L | |
| | | RST | RESET_SOC_L | 4 13 25 47 57 60 61 |
| | | RST | GPIO_SOC2BB_RST_L | 5 25 27 60 |
| | | RST | RST_BB_PMU_L | |
| | | RST | RST_BT_L | |
| | | RST | RST_DET_L | |
| | | RST | GPIO_SOC2GRAPE_RESET_L | 5 52 60 61 |
| | | RST | PMU_GPIO_CODEC_RST_L | 15 57 |
| | | RST | TS2PMU_RESET_IN | 47 57 |
| | | RST | GPIO_BB2SOC_RESET_DET_L | 5 25 29 |
| | | RST | SIMCRD_RST | |
| | | RST | WDOG_SOC | 4 13 |
| | | RST | WDOG_SOC2PMU_RESET_IN | 13 57 |
| | | RST | GPIO_OSCAR_RESET_L | 5 19 60 |
| | | RST | ISP1_CAM_FRONT_SHUTDOWN_L | 7 22 |
| | | RST | ISP0_CAM_REAR_SHUTDOWN_L | 7 23 |
| | | RST | ISP1_CAM_FRONT_SHUTDOWN_L_F | 22 60 |
| | | RST | ISP0_CAM_REAR_SHUTDOWN_L_F | 23 60 |
| | | RST | PMU_GPIO_PMU2BBPMU_RST_L | 25 27 57 60 |
| | | RST | PMU_GPIO_PMU2BBPMU_RST_R_L | 57 |
| | | RST | JTAG_AP_TRST_L | |
| | | RST | GPIO_BB_RST_L | |
| | | RST | RST_PMU_IN | |
| | | RST | UD881_RST | DEV |
| | | RST | UD882_RST | DEV |

## PMU SENSE

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| PMU_SENSE | * | * | 3:1_SPACING |
| PMU_SENSE | GND | * | 1.5:1_SPACING |

| VOLTAGE | PHYSICAL | SPACING | | |
|---|---|---|---|---|
| 1.1V | PWR_SENSE | PMU_SENSE | PPVDD_CPU_SOC_SENSE | 11 57 61 |
| 1.1V | PWR_SENSE | PMU_SENSE | PPVDD_GPU_SOC_SENSE | 11 57 61 |
| 1.0V | PWR_SENSE | PMU_SENSE | PPVDD_SOC_SOC_SENSE | 10 57 61 |
| 1.1V | PWR_SENSE | PMU_SENSE | PPVDD_CPU_RAIL_SENSE | 11 57 |
| 1.1V | PWR_SENSE | PMU_SENSE | PPVDD_GPU_RAIL_SENSE | 11 57 |
| 1.0V | PWR_SENSE | PMU_SENSE | PPVDD_SOC_RAIL_SENSE | 10 57 |
| 1.05V | MIN_NECK_WIDTH=0.053 MM PWR_SENSE | PMU_SENSE | ADC_SMPS1_MSMC_1V05 | |
| 1.8V | MIN_NECK_WIDTH=0.053 MM PWR_SENSE | PMU_SENSE | ADC_SMPS3_MSME_1V8 | |

# RF

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| RF_50S | * | 50_OHM_RF |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| RF_100D | * | 100_OHM_RF |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| 100_RF | * | * | 100_RF_CLEAR_SPACING |
| 50_RF | * | * | 50_RF_SPACING |
| 50_RF_CLEAR | * | * | 50_RF_CLEAR_SPACING |
| RF_60 | * | * | 1.2:1_SPACING |

| | VOLTAGE | NET_TYPE PHYSICAL | SPACING | | |
|---|---|---|---|---|---|
| 3 | 4.7V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_BATT_VCC_2G_FEM | 40 |
| 4 | 3.8V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_PA | 34 35 36 37 38 39 40 |
| 37 | 1.8V | MIN_NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM | PWR_RF | PP_LVS1 | 26 28 |
| 5 | 1.3V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_RF1_1V3_DRX_FE | 31 |
| 6 | 4.7V UNDEFINED | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_VREG | 26 |
| 8 | 2.05V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_RF2_2V05_DRX_BB | 31 |
| 9 | 4.7V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_BATT_VCC_PA_DCDC | |
| 538 | 1.8V | MIN_NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM | PWR_RF | PP_LDO1 | 26 60 |
| 611 | 1.8V | MAX_LINE_WIDTH=1 MM PWR_0P1MM | PWR_RF | PP_LDO2_XO_HS_1V8 | 26 28 |
| 612 | 1.8V | MAX_LINE_WIDTH=1 MM PWR_0P1MM | PWR_RF | PP_LDO3_AMUX_1V8 | 26 27 28 |
| 613 | 3.3V | MAX_LINE_WIDTH=1 MM PWR_0P25MM | PWR_RF | PP_LDO4_VDDA_3V3 | 26 28 |
| 614 | 2.5V | MIN_NECK_WIDTH=0.06 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM | PWR_RF | PP_LDO5_GPS_LNA_2V5 | 26 42 |
| 615 | 1.8V | MAXIMUM_NECK_LENGTH=5 MM MIN_NECK_WIDTH=0.15 MM MAX_LINE_WIDTH=1 MM PWR_0P3MM | PWR_RF | PP_LDO6_RUIM_1V8 | 26 28 44 60 |
| 2309 | 1.8V | MIN_NECK_WIDTH=0.15 MM MAX_LINE_WIDTH=1 MM PWR_0P3MM | PWR_RF | PP_LDO6_RUIM_1V8_FILT | 44 |
| 617 | 1.8V | MAX_LINE_WIDTH=1 MM PWR_0P25MM | PWR_RF | PP_LDO7_DAC_1V8 | 26 28 |
| 618 | 1.2V | MAXIMUM_NECK_LENGTH=9 MM MAX_LINE_WIDTH=1 MM PWR_0P3MM | PWR_RF | PP_LDO8_VDDPX_1V2 | 26 28 |
| 619 | 1.05V | MAX_LINE_WIDTH=1 MM PWR_0P75MM | PWR_RF | PP_LDO9_PLL_1V05 | 26 28 |
| 620 | 1.05V | MAX_LINE_WIDTH=1 MM PWR_0P75MM | PWR_RF | PP_LDO10_ADSP_1V05 | 26 28 |
| 621 | 1.05V | MAX_LINE_WIDTH=1 MM PWR_0P75MM | PWR_RF | PP_LDO11_MDSP_FW_1V05 | 26 28 |
| 622 | 1.05V | MAX_LINE_WIDTH=1 MM PWR_0P75MM | PWR_RF | PP_LDO12_MDSP_SW_1V05 | 26 28 |
| 623 | 2.95V | MAX_LINE_WIDTH=1 MM PWR_0P1MM | PWR_RF | PP_LDO13_VDDPX_2V95 | 26 28 |
| 627 | 2.65V | MAXIMUM_NECK_LENGTH=4 MM MAX_LINE_WIDTH=1 MM PWR_0P1MM | PWR_RF | PP_LDO14_2V65 | 26 33 40 41 |
| 626 | 1.05V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_VSW_S1 | 26 |
| 627 | 1.05V | MAX_LINE_WIDTH=1 MM PWR_0P75MM | PWR_RF | PP_SMPS1_MSMC_1V05 | 26 28 60 |
| 625 | 1.3V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_VSW_S2 | 26 |
| 629 | 1.3V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_SMPS2_RF1_1V3 | 26 28 31 60 |
| 628 | 1.8V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_VSW_S3 | 26 |
| 630 | 1.8V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_RF1_1V8_DIG | 31 |
| 2718 | 1.8V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_SMPS3_MSME_1V8_FILT | 29 |
| 630 | 2.05V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_VSW_S4 | 26 |
| 631 | 2.05V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_SMPS4_RF2_2V05 | 26 31 60 |
| 633 | 1.05V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_VSW_S5 | 26 |
| 634 | 1.05V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_SMPS5_DSP_1V05 | 26 60 |
| 2234 | 4.7V | MAX_LINE_WIDTH=1 MM PWR_RF | PWR_RF | PP_BATT_VCC_PA_DCDC_IN2 | |

| | NET_TYPE PHYSICAL | SPACING | | |
|---|---|---|---|---|
| 2001 | 45_OHM_SE | RF_60 | 50_HSIC_CAL | 28 |
| 640 | RF_50S | 50_RF_CLEAR | 50_XCVR_B13_B17_B20_TX | 30 33 |
| 641 | RF_50S | 50_RF | 50_XCVR_2G_LB_TX | 30 40 |
| 642 | RF_50S | 50_RF_CLEAR | 50_XCVR_B8_TX | 30 33 |
| 643 | RF_50S | 50_RF_CLEAR | 50_XCVR_B5_B18_TX | 30 33 |
| 644 | RF_50S | 50_RF_CLEAR | 50_XCVR_B2_B25_TX | 30 32 |
| 645 | RF_50S | 50_RF | 50_XCVR_2G_HB_TX | 30 40 |
| 646 | RF_50S | 50_RF_CLEAR | 50_XCVR_B3_B4_TX | 30 32 |
| 647 | RF_50S | 50_RF_CLEAR | 50_XCVR_B1_TX | 30 32 |
| 648 | RF_50S | 50_RF | 50_PDET_IN | 30 |
| 649 | RF_50S | 50_RF_CLEAR | 50_PDET_PAD_OUT | 30 |
| 650 | RF_50S | 50_RF_CLEAR | 50_PDET_PAD_IN | 30 40 |
| 651 | RF_50S | 50_RF_CLEAR | 50_B1_TX_SAW_IN | 32 33 |
| 654 | RF_50S | 50_RF_CLEAR | 50_B3_B4_TX_SAW_IN | 32 33 |
| 653 | RF_50S | 50_RF_CLEAR | 50_B2_B25_TX_SAW_IN | 32 33 |
| 727 | RF_50S | 50_RF_CLEAR | 50_B1_TX_SAW_OUT | 33 34 |
| 728 | RF_50S | 50_RF_CLEAR | 50_B2_TX_SAW_OUT | 33 35 |
| 729 | RF_50S | 50_RF_CLEAR | 50_B3_TX_SAW_OUT | 33 35 |
| 730 | RF_50S | 50_RF_CLEAR | 50_B4_TX_SAW_OUT | 33 34 |
| 731 | RF_50S | 50_RF_CLEAR | 50_B5_TX_SAW_OUT | 33 37 |
| 732 | RF_50S | 50_RF_CLEAR | 50_B8_TX_SAW_OUT | 33 37 |
| 733 | RF_50S | 50_RF_CLEAR | 50_B13_TX_SAW_OUT | 33 38 |
| 734 | RF_50S | 50_RF_CLEAR | 50_B17_TX_SAW_OUT | 33 38 |
| 735 | RF_50S | 50_RF_CLEAR | 50_B20_TX_SAW_OUT | 33 36 |
| 631 | RF_50S | 50_RF_CLEAR | 50_PCS_RX | |
| 636 | RF_50S | 50_RF | 50_PCS_RX_MATCH | |
| 637 | RF_50S | 50_RF_CLEAR | 50_DCS_RX | |
| 635 | RF_50S | 50_RF_CLEAR | 50_DCS_RX_MATCH | |

| | NET_TYPE PHYSICAL | SPACING | | |
|---|---|---|---|---|
| 580 | RF_50S | 50_RF_CLEAR | 50_B1_TX_PAD_IN | 34 |
| 587 | RF_50S | 50_RF_CLEAR | 50_B4_TX_PAD_IN | 34 |
| 588 | RF_50S | 50_RF_CLEAR | 50_B1_B4_DPLX_ANT | 34 |
| 589 | RF_50S | 50_RF_CLEAR | 50_B1_B4_ANT | 34 40 |
| 2228 | RF_50S | 50_RF_CLEAR | 50_B1_B4_ANT_PHASESHIFT | 34 |
| 585 | RF_50S | 50_RF_CLEAR | 50_B2_TX_PAD_IN | 35 |
| 584 | RF_50S | 50_RF_CLEAR | 50_B3_TX_PAD_IN | 35 |
| 591 | RF_50S | 50_RF_CLEAR | 50_B2_DUPLX_RX | 32 35 |
| 590 | RF_50S | 50_RF_CLEAR | 50_B3_DUPLX_RX | 32 35 |
| 592 | RF_50S | 50_RF_CLEAR | 50_B2_DPLX_ANT | 35 |
| 583 | RF_50S | 50_RF_CLEAR | 50_B3_DPLX_ANT | 35 |
| 2105 | RF_50S | 50_RF_CLEAR | 50_B2_ANT | 35 40 |
| 586 | RF_50S | 50_RF_CLEAR | 50_B3_ANT | 35 40 |
| 593 | RF_50S | 50_RF_CLEAR | 50_B2_RX_BALUN | 32 |
| 582 | RF_50S | 50_RF_CLEAR | 50_B3_RX_BALUN | 32 |
| 2226 | RF_50S | 50_RF_CLEAR | 50_B2_ANT_PHASESHIFT | 35 |
| 2227 | RF_50S | 50_RF_CLEAR | 50_B3_ANT_PHASESHIFT | 35 |
| 596 | RF_50S | 50_RF_CLEAR | 50_B20_TX_PAD_IN | 36 |
| 597 | RF_50S | 50_RF_CLEAR | 50_B20_DPLX_ANT | 36 |
| 595 | RF_50S | 50_RF_CLEAR | 50_B20_ANT | 36 40 |
| 2229 | RF_50S | 50_RF_CLEAR | 50_B20_ANT_PHASESHIFT | |
| 2107 | RF_50S | 50_RF_CLEAR | 50_B5_TX_PAD_IN | 37 |
| 2101 | RF_50S | 50_RF_CLEAR | 50_B8_TX_PAD_IN | 37 |
| 2104 | RF_50S | 50_RF_CLEAR | 50_B5_DPLX_ANT | 37 |
| 2103 | RF_50S | 50_RF_CLEAR | 50_B8_DPLX_ANT | 37 |
| 2102 | RF_50S | 50_RF_CLEAR | 50_B5_ANT | 37 40 |
| 2105 | RF_50S | 50_RF_CLEAR | 50_B8_ANT | 37 40 |
| 2106 | RF_50S | 50_RF_CLEAR | 50_B5_ANT_PHASESHIFT | |
| 2224 | RF_50S | 50_RF_CLEAR | 50_B8_ANT_PHASESHIFT | 37 |
| 2253 | RF_50S | 50_RF_CLEAR | 50_B7_ANT | 36 40 |
| 2254 | RF_50S | 50_RF_CLEAR | 50_B7_BALUN_IN_RX | |
| 2255 | RF_50S | 50_RF_CLEAR | 50_B7_DPLX_ANT | 36 |
| 2256 | RF_50S | 50_RF_CLEAR | 50_B7_DUPLX_RX | 32 36 |
| 2257 | RF_50S | 50_RF_CLEAR | 50_B7_TX_PAD_IN | 36 |
| 2258 | RF_50S | 50_RF_CLEAR | 50_B7_TX_SAW_IN | 36 |
| 2259 | RF_50S | 50_RF_CLEAR | 50_B7_TX_SAW_OUT | 36 |
| 2262 | RF_50S | 50_RF_CLEAR | 50_XCVR_B7_TX | 30 36 |
| 2123 | RF_50S | 50_RF_CLEAR | 50_B13_TX_PAD_IN | 38 |
| 2124 | RF_50S | 50_RF_CLEAR | 50_B17_TX_PAD_IN | 38 |
| 2126 | RF_50S | 50_RF_CLEAR | 50_B13_DPLX_ANT | 38 |
| 2125 | RF_50S | 50_RF_CLEAR | 50_B17_DPLX_ANT | 38 |
| 2127 | RF_50S | 50_RF_CLEAR | 50_B13_LPF_IN | 38 |
| 2130 | RF_50S | 50_RF_CLEAR | 50_B13_ANT | 38 40 |
| 2129 | RF_50S | 50_RF_CLEAR | 50_B17_ANT | 38 40 |
| 2232 | RF_50S | 50_RF_CLEAR | 50_B13_ANT_PHASESHIFT | |
| 2233 | RF_50S | 50_RF_CLEAR | 50_B17_ANT_PHASESHIFT | 38 |
| 2135 | RF_50S | 50_RF_CLEAR | 50_XCVR_2G_LB_TX_MATCH | |
| 2134 | RF_50S | 50_RF_CLEAR | 50_XCVR_2G_HB_TX_MATCH | 40 |
| 2132 | RF_50S | 50_RF_CLEAR | 50_2G_LB_PA_IN | 40 |
| 2133 | RF_50S | 50_RF_CLEAR | 50_2G_HB_PA_IN | 40 |
| 2225 | RF_50S | 50_RF_CLEAR | 50_PRI_ANT_ASM | 40 |
| 2140 | RF_50S | 50_RF_CLEAR | 50_DRX_ANT_TEST | 41 43 |
| 2221 | RF_50S | 50_RF_CLEAR | 50_DRX_ANT_PHASESHIFT | 43 |
| 2222 | RF_50S | 50_RF_CLEAR | 50_DRX_ANT_FEED | 43 |
| 2157 | RF_50S | 50_RF_CLEAR | 50_COUPLER_TERM | |
| 2156 | RF_50S | 50_RF_CLEAR | 50_DIVERSITY_SWITCH_MATCH | 41 |
| 2159 | RF_50S | 50_RF_CLEAR | 50_GPS_LNA_OUT | 41 42 |
| 2158 | RF_50S | 50_RF_CLEAR | 50_GPS_ANT_COAX | 42 |
| 2160 | RF_50S | 50_RF_CLEAR | 50_GPS_ANT_MATCH | |
| 2162 | RF_50S | 50_RF_CLEAR | 50_GPS_ANT_TEST | |
| 2220 | RF_50S | 50_RF_CLEAR | 50_GPS_LNA_IN | 42 |
| 2260 | RF_50S | 50_RF_CLEAR | 50_PRI-ANT_COUPLER | |
| 2261 | RF_50S | 50_RF_CLEAR | 50_PRI-ANT_PHASE | |
| 2240 | RF_50S | 50_RF_CLEAR | 50_PRI_ANT_TEST | |
| 2239 | RF_50S | 50_RF_CLEAR | 50_PRI_ANT_TEST_IN | |
| 2238 | RF_50S | 50_RF_CLEAR | 50_PRI_ANT_COAX | 40 43 |
| 2236 | RF_50S | 50_RF_CLEAR | 50_ANT2_TERM | |
| 2235 | RF_50S | 50_RF_CLEAR | 50_DRX_ANT_TERM | |
| 2237 | RF_60 | | 2G_FEM_S0 | 29 40 |
| 2238 | RF_60 | | 2G_FEM_S1 | 25 29 40 |
| 2239 | RF_60 | | 2G_FEM_S2 | 29 33 40 |
| 2240 | RF_60 | | 2G_FEM_S3 | 29 33 40 |
| 2241 | RF_60 | | 2G_FEM_S4 | 25 29 40 |
| 2242 | RF_60 | | 2G_FEM_S5 | 29 40 |
| 2243 | RF_60 | | 2G_FEM_S6 | 29 40 |
| 2244 | RF_60 | | BB_PDM | 29 39 |
| 2245 | RF_60 | | BB_PDM_FILT | 39 |
| 2246 | RF_60 | | DCDC_ADJ | 39 |
| 2247 | RF_60 | | PA_R1 | 29 34 35 36 37 38 |

| | NET_TYPE PHYSICAL | SPACING | | |
|---|---|---|---|---|
| 1279 | RF_60 | | WTR_GP_DATA0 | 29 30 |
| 1274 | RF_60 | | WTR_GP_DATA1 | 29 30 |
| 1277 | RF_60 | | BB_ERROR_FLAG | 25 29 |
| 1275 | RF_60 | | PA_ON_B1_B4 | 29 34 |
| 1276 | RF_60 | | PA_ON_B2_B3 | 29 35 |
| 1272 | RF_60 | | PA_ON_B5_B8 | 29 37 |
| 1273 | RF_60 | | PA_ON_B7_B20 | 29 36 |
| 1271 | RF_60 | | PA_ON_B13_B17 | 29 38 |
| 1281 | RF_60 | | PA_BS | 29 34 35 36 37 38 |
| 1285 | RF_60 | | LAT_SW1_CTL | 25 29 |
| 1286 | RF_60 | | PS_HOLD | 27 29 |
| 1284 | RF_60 | | WTR_RF_ON | 25 29 30 |
| 1283 | RF_60 | | WTR_RX_ON | 25 29 30 |
| 1282 | RF_60 | | DCDC_MODE | 29 39 |
| 1287 | RF_60 | | DCDC_ENABLE | |
| 1288 | RF_60 | | DRX_ASM_V1 | 29 41 |
| 1290 | RF_60 | | DRX_ASM_V2 | 29 41 |
| 1291 | RF_60 | | DRX_ASM_V3 | 29 41 |
| 1289 | RF_60 | | DRX_ASM_V4 | 29 41 |
| 1280 | RF_60 | | 19P2M_CLK_EN | 27 28 |
| 1278 | RF_60 | | PMIC_RESOUT_L | 25 27 28 |
| 1285 | RF_60 | | PMIC_SSBI | 25 27 28 |

| | NET_TYPE PHYSICAL | SPACING | | |
|---|---|---|---|---|
| 1107 | RF_DIFF | RF_DIFF | RF_60 | TX_BB_Q_P 29 30 |
| 1109 | RF_DIFF | RF_DIFF | RF_60 | TX_BB_Q_N 29 30 |
| 1108 | RF_DIFF | RF_DIFF | RF_60 | DRX_BB_Q_P 29 30 |
| 1110 | RF_DIFF | RF_DIFF | RF_60 | DRX_BB_Q_N 29 30 |
| 1112 | RF_DIFF | RF_DIFF | RF_60 | GPS_BB_Q_P 29 30 |
| 1111 | RF_DIFF | RF_DIFF | RF_60 | GPS_BB_Q_N 29 30 |
| 1113 | RF_DIFF | RF_DIFF | RF_60 | PRX_BB_Q_P 29 30 |
| 1114 | RF_DIFF | RF_DIFF | RF_60 | PRX_BB_Q_N 29 30 |
| 1115 | RF_DIFF | RF_DIFF | RF_60 | DRX_BB_I_P 29 30 |
| 1116 | RF_DIFF | RF_DIFF | RF_60 | DRX_BB_I_N 29 30 |
| 1117 | RF_DIFF | RF_DIFF | RF_60 | GPS_BB_I_P 29 30 |
| 1118 | RF_DIFF | RF_DIFF | RF_60 | GPS_BB_I_N 29 30 |
| 1119 | RF_DIFF | RF_DIFF | RF_60 | PRX_BB_I_P 29 30 |
| 1120 | RF_DIFF | RF_DIFF | RF_60 | PRX_BB_I_N 29 30 |
| 1122 | RF_DIFF | RF_DIFF | RF_60 | TX_BB_I_P 29 30 |
| 1121 | RF_DIFF | RF_DIFF | RF_60 | TX_BB_I_N 29 30 |
| 1169 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B13_B17_B20_PRX_P 30 33 |
| 1170 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B13_B17_B20_PRX_N 30 33 |
| 1171 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B8_PRX_P 30 32 |
| 1172 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B8_PRX_N 30 32 |
| 1173 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B5_B18_PRX_P 30 32 |
| 1174 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B5_B18_PRX_N 30 32 |
| 1175 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B2_B25_PRX_P 30 32 |
| 1176 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B2_B25_PRX_N 30 32 |
| 1177 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B3_PRX_P 30 32 |
| 1178 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B3_PRX_N 30 32 |
| 1179 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_DCS_PCS_PRX_P |
| 1181 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_DCS_PCS_PRX_N |
| 1182 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B1_B4_PRX_P 30 32 |
| 1180 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B1_B4_PRX_N 30 32 |
| 1184 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B8_B20_DRX_P 30 41 |
| 1183 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B8_B20_DRX_N 30 41 |
| 1185 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B5_B18_B13_B17_DRX_P 30 41 |
| 1187 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B5_B18_B13_B17_DRX_N 30 41 |
| 1186 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B2_B25_B3_DRX_P 30 41 |
| 1189 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B2_B25_B3_DRX_N 30 41 |
| 1190 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B1_B4_DRX_P 30 41 |
| 1188 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B1_B4_DRX_N 30 41 |
| 1192 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_GPS_RX_P 30 41 |
| 1191 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_GPS_RX_N 30 41 |
| 1195 | RF_DIFF | RF_100D | 100_RF | 100_B13_DUPLX_RX_P 33 38 |
| 1193 | RF_DIFF | RF_100D | 100_RF | 100_B13_DUPLX_RX_N 33 38 |
| 1194 | RF_DIFF | RF_100D | 100_RF | 100_B17_DUPLX_RX_P 33 38 |
| 1197 | RF_DIFF | RF_100D | 100_RF | 100_B17_DUPLX_RX_N 33 38 |
| 1196 | RF_DIFF | RF_100D | 100_RF | 100_B20_DUPLX_RX_P 33 36 |
| 1199 | RF_DIFF | RF_100D | 100_RF | 100_B20_DUPLX_RX_N 33 36 |
| 1198 | RF_DIFF | RF_100D | 100_RF | 100_DCS_PCS_RX_FILTER_P |
| 1200 | RF_DIFF | RF_100D | 100_RF | 100_DCS_PCS_RX_FILTER_N |
| 1205 | RF_DIFF | RF_100D | 100_RF | 100_B1_B4_DUPLX_RX_P 32 34 |
| 1206 | RF_DIFF | RF_100D | 100_RF | 100_B1_B4_DUPLX_RX_N 32 34 |
| 1207 | RF_DIFF | RF_100D | 100_RF | 100_B8_DUPLX_RX_P 32 37 |
| 1210 | RF_DIFF | RF_100D | 100_RF | 100_B8_DUPLX_RX_N 32 37 |
| 1211 | RF_DIFF | RF_100D | 100_RF | 100_B5_B18_DUPLX_RX_P 32 37 |
| 1209 | RF_DIFF | RF_100D | 100_RF | 100_B5_B18_DUPLX_RX_N 32 37 |
| 1165 | RF_DIFF | RF_100D | 100_RF | 100_B7_PRX_BALUN_OUT_P 32 |
| 1164 | RF_DIFF | RF_100D | 100_RF | 100_B7_PRX_BALUN_OUT_N 32 |
| 1163 | RF_DIFF | RF_100D | 100_RF | 100_B7_PRX_MATCH_P 32 |
| 1167 | RF_DIFF | RF_100D | 100_RF | 100_B7_PRX_MATCH_N 32 |
| 1208 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B7_PRX_P 30 32 |
| 1166 | RF_DIFF | RF_100D | 100_RF | 100_XCVR_B7_PRX_N 30 32 |
| 1349 | | | RF_CLK | SLEEP_CLK_32K 25 27 28 |
| 1352 | | | RF_CLK | 19P2M_WTR 27 30 |
| 1353 | | | RF_CLK | 19P2M_MDM 25 27 28 |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| 50_RF_SPACING | TOP,BOTTOM | 0.178 MM | ? |
| 50_RF_SPACING | ISL3 | 0.130 MM | ? |
| 50_RF_SPACING | * | 0.092 MM | ? |
| 50_RF_CLEAR_SPACING | TOP,BOTTOM | 0.178 MM | ? |
| 50_RF_CLEAR_SPACING | ISL3 | 0.130 MM | ? |
| 50_RF_CLEAR_SPACING | * | 0.138 MM | ? |
| 100_RF_CLEAR_SPACING | TOP,BOTTOM | 0.143 MM | ? |
| 100_RF_CLEAR_SPACING | * | 0.118 MM | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GND | 50_RF | * | 50_RF_CLEAR_SPACING |
| GND | 50_RF_CLEAR | * | 50_RF_CLEAR_SPACING |
| GND | 100_RF | * | 100_RF_CLEAR_SPACING |
| GND | RF_60 | * | 1.2:1_SPACING |
| GND | PWR_RF | * | 1.2:1_SPACING |
| PWR_RF | PWR_RF | * | 1.2:1_SPACING |
| RF_CLK | * | * | 3:1_SPACING |
| RF_CLK | GND | * | 1.2:1_SPACING |

NC_PMU_OUT_32K_CLK_GPS == PMU_OUT_32K_CLK_GPS
NO_TEST=TRUE
MAKE_BASE=TRUE
IN 57 64

RF

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| WIFI_50S | * | 50_OHM_RF |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| WIFI | * | * | 4:1_SPACING |