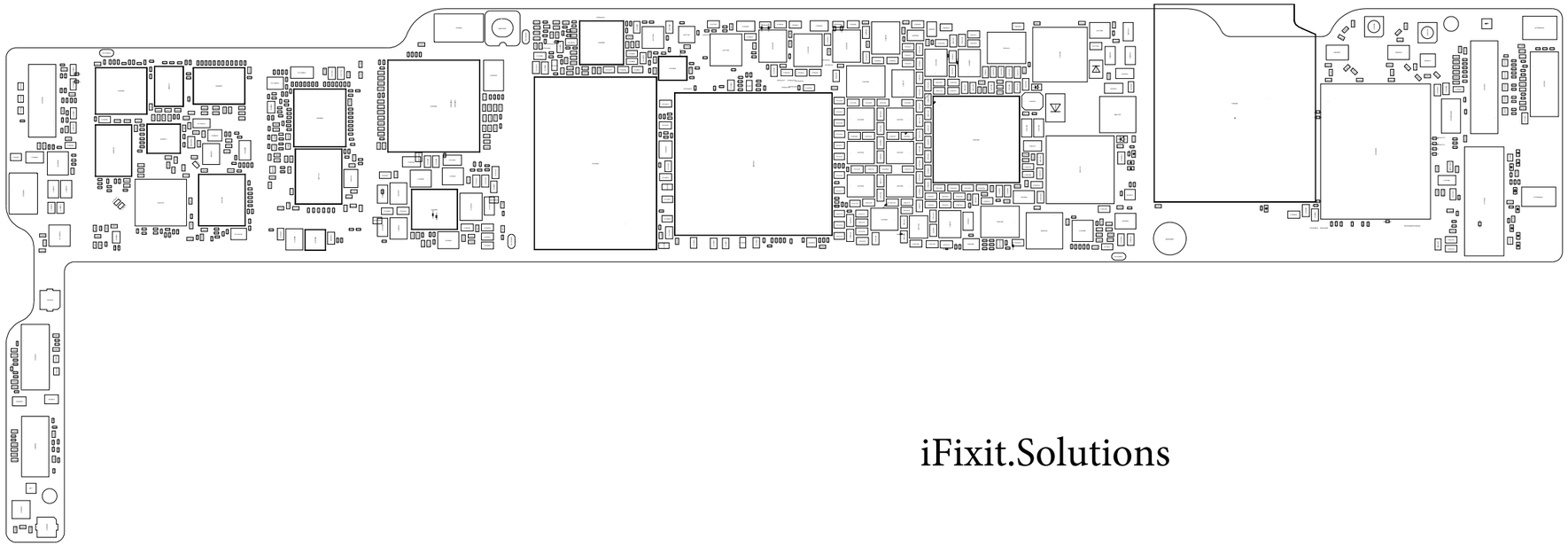

iFixit.Solutions

TOP SIDE ASSEMBLY

APPLE				TITLE PCBF, X200 MLB (C1)
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ORIG DIV	DESIGNER HURLEY	DATE 01/08/13	SCALE 1:1	DRAWING NUMBER 820-4124-A

NOTES:
ARTWORK VIEWED FROM COMPONENT SIDE. PCB SHALL CONFORM TO STANDARDS AS DEFINED IN APPLE SPECIFICATION 062-0031 (DOUBLE-SIDED BOARDS) OR 062-0073 (MULTI-LAYER BOARDS) AS APPLICABLE.

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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X200 MLB-C1

LAST_MODIFIED=Tue Oct 29 15:52:27 2013

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0002535199	PRODUCTION RELEASED	2014-01-13

SCH AND BOARD PART NUMBERS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-0886	1	SCH,MLB-C1,X200	SCH1	
820-4124	1	PCBF,MLB-C1,X200	PCB1	

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	N/A	N/A
2	2	BLOCK DIAGRAM: SYSTEM	J85_MLB_C1	04/02/2013
3	4	BOM TABLES	J72_MLB_C1	11/26/2012
4	6	SOC: MAIN	N/A	04/18/2011
5	7	SOC: I/OS	N/A	05/05/2011
6	8	SOC: NAND	N/A	04/18/2011
7	9	SOC: DP,MIPI	MLB	05/04/2012
8	10	SOC: SRAM, IO PWRS	N/A	04/18/2011
9	11	SOC: VDD, SRAM, CPU, GPU PWRS	N/A	04/18/2011
10	12	SOC: MISC & ALIASES	N/A	04/11/2011
11	13	IO: TRISTAR	N/A	N/A
12	14	NAND STORAGE	MLB	05/04/2012
13	17	TOUCH: SUPPORT CKT & CONN	N/A	06/21/2010
14	18	AUDIO: HP FLEX CONN	N/A	03/31/2011
15	19	AUDIO: L81 CODEC	KAVITHA	01/18/2012
16	20	AUDIO: CS35L19A AMPS	KAVITHA	01/18/2012
17	21	BUTTON: CONN	N/A	N/A
18	22	VIDEO: EDP SUPPORT & CONN	J85 MLB_C1	12/05/2012
19	24	SENSOR: OSCAR	J72_MLB_C1	11/26/2012
20	26	CAMERA: FF-ALS CONN & FILTERS	J85 MLB_C1	12/03/2012
21	27	SENSOR: ACCEL, COMPASS, GYRO	N/A	N/A
22	28	SENSOR: PROX	J85 MLB_C1	12/05/12
23	29	CAMERA: REAR CONN & FILTERS	N/A	N/A
24	30	CELL:AP INTERFACE & DEBUG CONNECTORS	RADIO_MLB_C0	10/29/2013
25	32	CELL: BASEBAND PMU (1 0F 2)	RADIO_MLB_C0	10/29/2013
26	33	CELL: BASEBAND PMU (2 OF 2)	RADIO_MLB_C0	10/29/2013
27	34	CELL: BASEBAND (1 OF 2)	RADIO_MLB_C0	10/29/2013
28	35	CELL: BASEBAND (2 OF 2)	RADIO_MLB_C0	10/29/2013
29	36	CELL: RF TRANSCEIVER (1 0F 2)	RADIO_MLB_C0	10/29/2013
30	37	CELL: RF TRANSCEIVER (2 OF 2)	RADIO_MLB_C0	10/29/2013
31	38	CELL: RX MATCHING	RADIO_MLB_C0	10/29/2013
32	39	CELL: RF TRANSCEIVER (3 OF 4)	RADIO_MLB_C0	10/29/2013
33	40	CELL: PENTABAND PA	RADIO_MLB_C0	10/29/2013
34	41	CELL: BAND 2/3 PAD	RADIO_MLB_C0	10/29/2013
35	42	CELL: BAND 7/20 PAD	RADIO_MLB_C0	10/29/2013
36	43	CELL: BAND 5/8 PAD	RADIO_MLB_C0	10/29/2013
37	44	CELL: 2G PA	RADIO_MLB_C0	10/29/2013
38	45	CELL: PA DCDC CONVERTER	RADIO_MLB_C0	10/29/2013
39	46	CELL: ASM AND HB LTE FRONT-END	RADIO_MLB_C0	10/29/2013
40	47	CELL: RX DIVERSITY	RADIO_MLB_C0	10/29/2013
41	48	CELL: GPS	RADIO_MLB_C0	10/29/2013
42	49	CELL: ANTENNA FEEDS	RADIO_MLB_C0	10/29/2013
43	57	IO: FILTERS & HOTBAR CONN	N/A	04/18/2011
44	58	WIFI/BT: MODULE	WIFI_DEV	05/20/2013
45	75	POWER: BATTERY CONNECTOR	N/A	N/A
46	81	PMU: ANYA PAGE 1	J72_MLB_C1	11/26/2012
47	82	PMU: ANYA PAGE 2	J85 MLB_C1	12/03/2012
48	83	PMU: ANYA PAGE 3	J72_MLB_C1	11/26/2012
49	84	PMU: ANYA PAGE 4	J72_MLB_C1	11/26/2012
50	85	POWER: PP1V8_SW	J85 MLB_C1	11/26/2012
51	90	SEP: EEPROM & SOC DEBUG	J72_MLB_C1	11/26/2012
52	93	TEST: TP/HOLES/FIDUCIALS	J85 MLB_C1	12/03/12
53	94	TEST: EE TP/PP	J72_MLB_C1	11/26/2012
54	121	POWER: ALIASES	J72_MLB_C1	11/26/2012

DRAWING

DRAWING TITLE: SCH,MLB-C1,X200

Apple Inc.

DRAWING NUMBER: 051-0886 SIZE: D

REVISION: A.0.0

BRANCH

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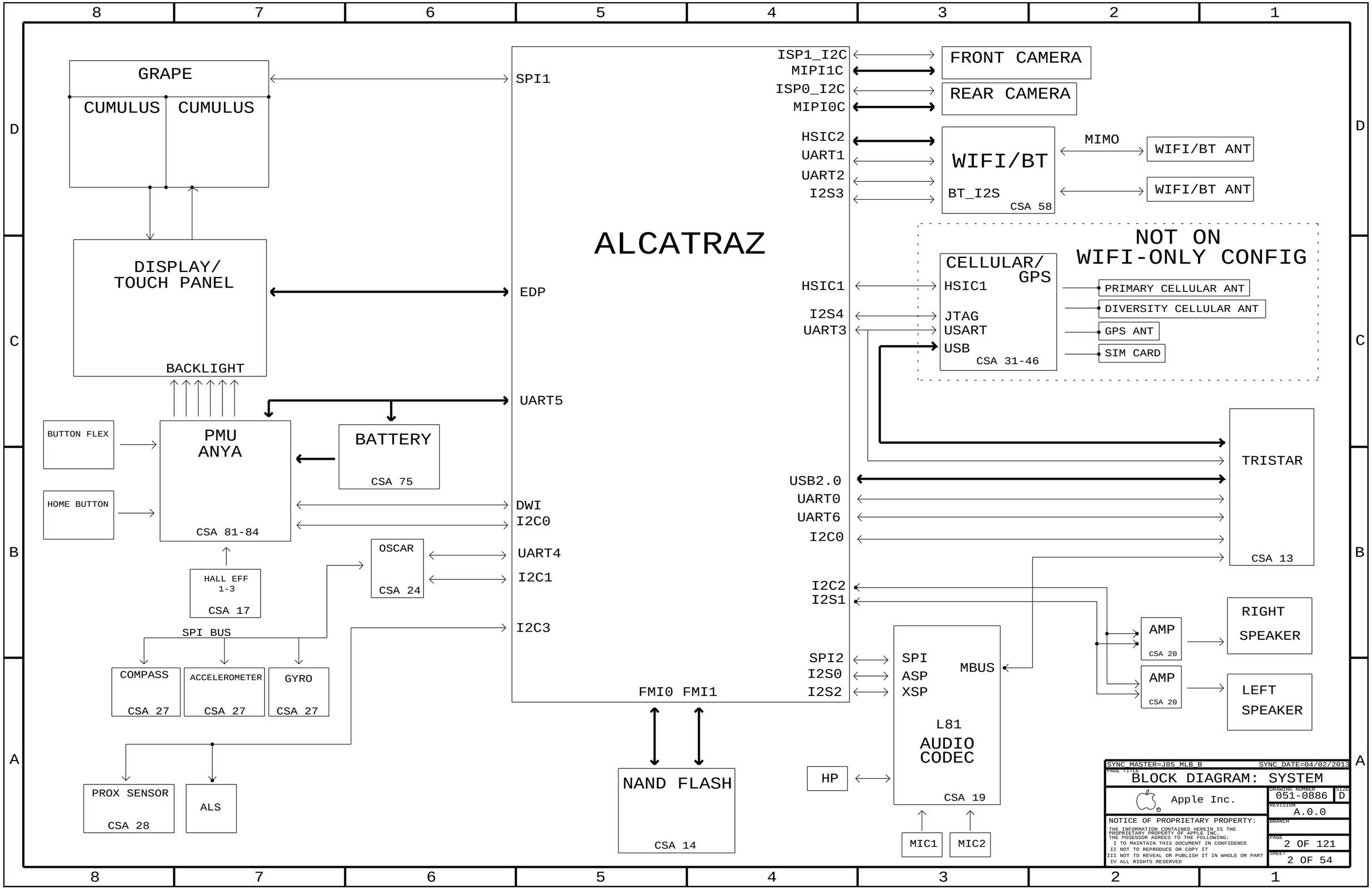
GRAPE
CUMULUS
CUMULUS
SPI1
DISPLAY/
TOUCH PANEL
BACKLIGHT
EDP
UART5
BUTTON FLEX
PMU
ANYA
CSA 81-84
BATTERY
CSA 75
HOME BUTTON
DWI
I2C0
HALL EFF
1-3
CSA 17
OSCAR
CSA 24
UART4
I2C1
SPI BUS
I2C3
COMPASS
CSA 27
ACCELEROMETER
CSA 27
GYRO
CSA 27
PROX SENSOR
CSA 28
ALS
ALCATRAZ
FMI0 FMI1
NAND FLASH
CSA 14
ISP1_I2C
MIPI1C
ISP0_I2C
MIPI0C
FRONT CAMERA
REAR CAMERA
HSIC2
UART1
UART2
I2S3
WIFI/BT
BT_I2S
CSA 58
MIMO
WIFI/BT ANT
WIFI/BT ANT
NOT ON
WIFI-ONLY CONFIG
CELLULAR/
GPS
HSIC1
HSIC1
I2S4
UART3
JTAG
USART
USB
CSA 31-46
PRIMARY CELLULAR ANT
DIVERSITY CELLULAR ANT
GPS ANT
SIM CARD
TRISTAR
CSA 13
USB2.0
UART0
UART6
I2C0
I2C2
I2S1
AMP
CSA 20
AMP
CSA 20
RIGHT
SPEAKER
LEFT
SPEAKER
SPI2
I2S0
I2S2
SPI
ASP
XSP
MBUS
L81
AUDIO
CODEC
CSA 19
HP
MIC1
MIC2
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SYNC DATE=04/02/2013
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BLOCK DIAGRAM: SYSTEM
Apple Inc.
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD
32GB_PROD
64GB_PROD
128GB_PROD

DEVELOPMENT_JTAG_TAP
JTAG_DAP
MLB (WDOG TO PMU)

WIFI BOM OPTIONS

ANDGATE_TI
FERRITE_TY
FERRITE_TDK

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-6207	1	FENCE,TALL,MLB,X221	PD_FENCE_MLB	CRITICAL	
806-7613	1	FENCE,RADIO,MLB,C BRD,X221	PD_CAN_RADIO	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	EEEE FOR 639-5393 (X200C1 GOOD)	FNJD	CRITICAL	EEEE_X200C_GOOD
825-7639	1	EEEE FOR 639-5394 (X200C1 BETTER)	FNJ5	CRITICAL	EEEE_X200C_BETTER
825-7639	1	EEEE FOR 639-5385 (X200C1 BEST)	FNJ9	CRITICAL	EEEE_X200C_BEST
825-7639	1	EEEE FOR 639-5386 (X200C1 BEST+)	FNJH	CRITICAL	EEEE_X200C_BEST+
825-7639	1	EEEE FOR 639-5387 (X200C1 ULTIMATE)	FNJ6	CRITICAL	EEEE_X200C_ULTIMATE
825-7639	1	EEEE FOR 639-5388 (X200C1 GOOD IVS)	FNJ8	CRITICAL	EEEE_X200C_GOOD_IVS
825-7639	1	EEEE FOR 639-5389 (X200C1 BETTER IVS)	FNJF	CRITICAL	EEEE_X200C_BETTER_IVS
825-7639	1	EEEE FOR 639-5390 (X200C1 BEST IVS)	FNJC	CRITICAL	EEEE_X200C_BEST_IVS
825-7639	1	EEEE FOR 639-5391 (X200C1 BEST+ IVS)	FNJ7	CRITICAL	EEEE_X200C_BEST+_IVS
825-7639	1	EEEE FOR 639-5392 (X200C1 ULTIMATE IVS)	FNJG	CRITICAL	EEEE_X200C_ULTIMATE_IVS

WIFI

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0223	339S0213		U5800	

GYRO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1192	1	GYRO, ST MICRO	U2720	CRITICAL	GYRO_STMICRO
338S1218	1	GYRO, INVENSENSE	U2720	CRITICAL	GYRO_INVENSENSE
132S0391	1	CAP 0.01UF 25V 0201	C2726	CRITICAL	GYRO_STMICRO
132S0288	1	CAP 0.1UF 16V 0201	C2726	CRITICAL	GYRO_INVENSENSE

338S1158 OLD GYRO - ST MICRO

OLDER INVENSENSE P/N 338S1135
OLD INVENSENSE P/N 338S1200 (3/22/13)

ACCEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1163	1	IC,ACCEL,3-AXIS,DIG,BMA282,LGA14	U2700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

338S1233 ST MICRO - DISQUAL'ED
338S1114 OLD ACCEL - ST MICRO
338S1191 OLD ACCEL - ST MICRO

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0207	1	H6P + 1GB ELPIDA	U0652	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0208	339S0207		U0652	HYNIX DDR

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0656	1	IC,PMU,ANYA,D2089A1,OTPXX,FCCSP342	U8100	CRITICAL	

FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0921	1	TOS,19NM,PPN1.5,C,DDP,16GB	U1400	16GB
335S0922	1	TOS,19NM,PPN1.5,C,QDP,32GB	U1400	32GB
335S0923	1	TOS,19NM,PPN1.5,C,ODP,64GB	U1400	64GB
335S0929	1	TOS,19NM,PPN1.5,C,12DP,64GB	U1400	96GB
335S0924	1	TOS,19NM,PPN1.5,C,16DP,128GB	U1400	128GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0930	335S0921	16GB	U1400	HYNIX 20NM PPN1.5 16GB
335S0931	335S0922	32GB	U1400	HYNIX 20NM PPN1.5 32GB
335S0932	335S0923	64GB	U1400	HYNIX 20NM PPN1.5 64GB

U2200

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S4272	1	IC,SLG5AP1423V,PWR SW,GREENFET3,4A,TDFN8	U2200	

NOTE: FOLLOWING J72, U2200 USES 353S3672 FOOTPRINT (353S4272 HAS SMALLER PADS DUE TO NEW DFM RULES)

4.3UF CAP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657		C1009,C1015,...	RDAR #13988471

SYNC_MASTER=J72_MLB_C SYNC_DATE=11/26/2012

PAGE TITLE
BOM TABLES

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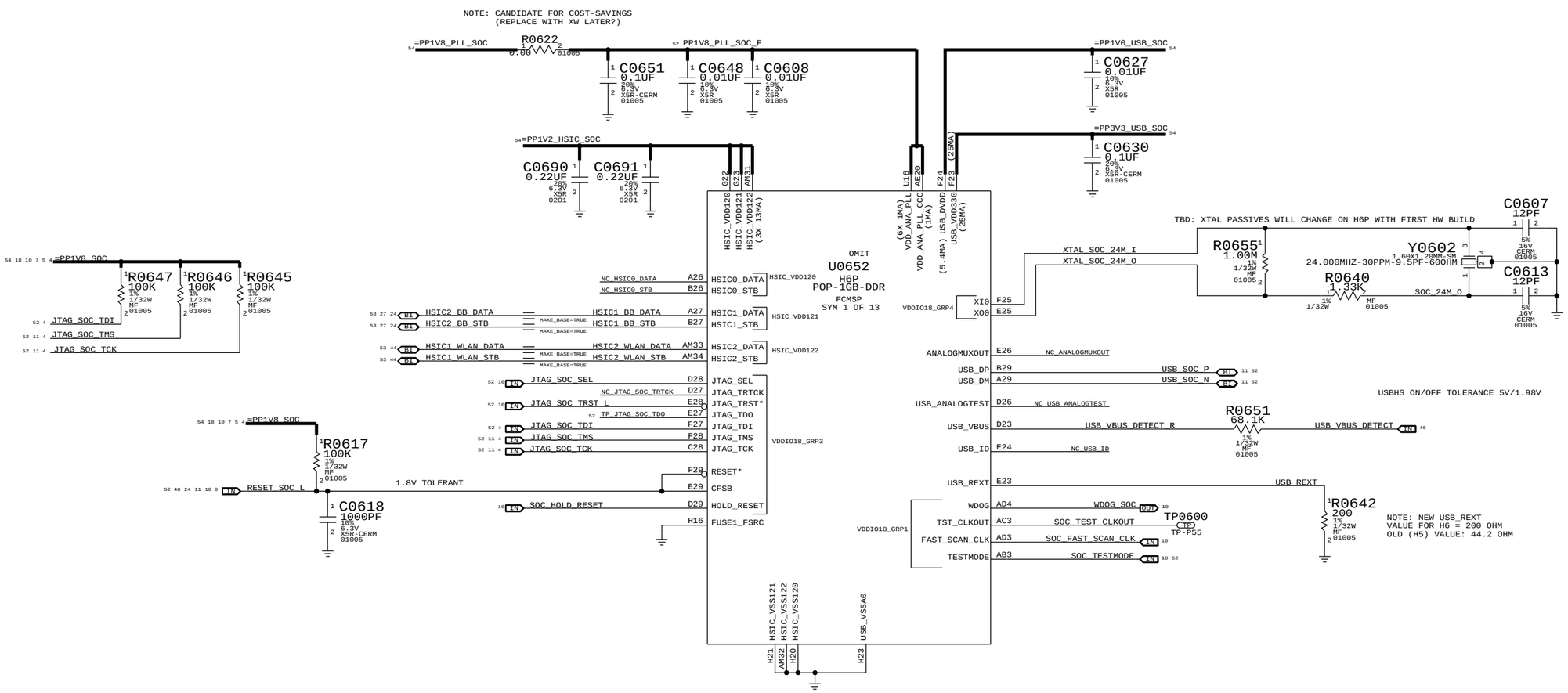
H6P: JTAG, USB, PLL, HSIC, XTAL



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Apple Inc.	DRAWING NUMBER: 051-0886 SIZE: D
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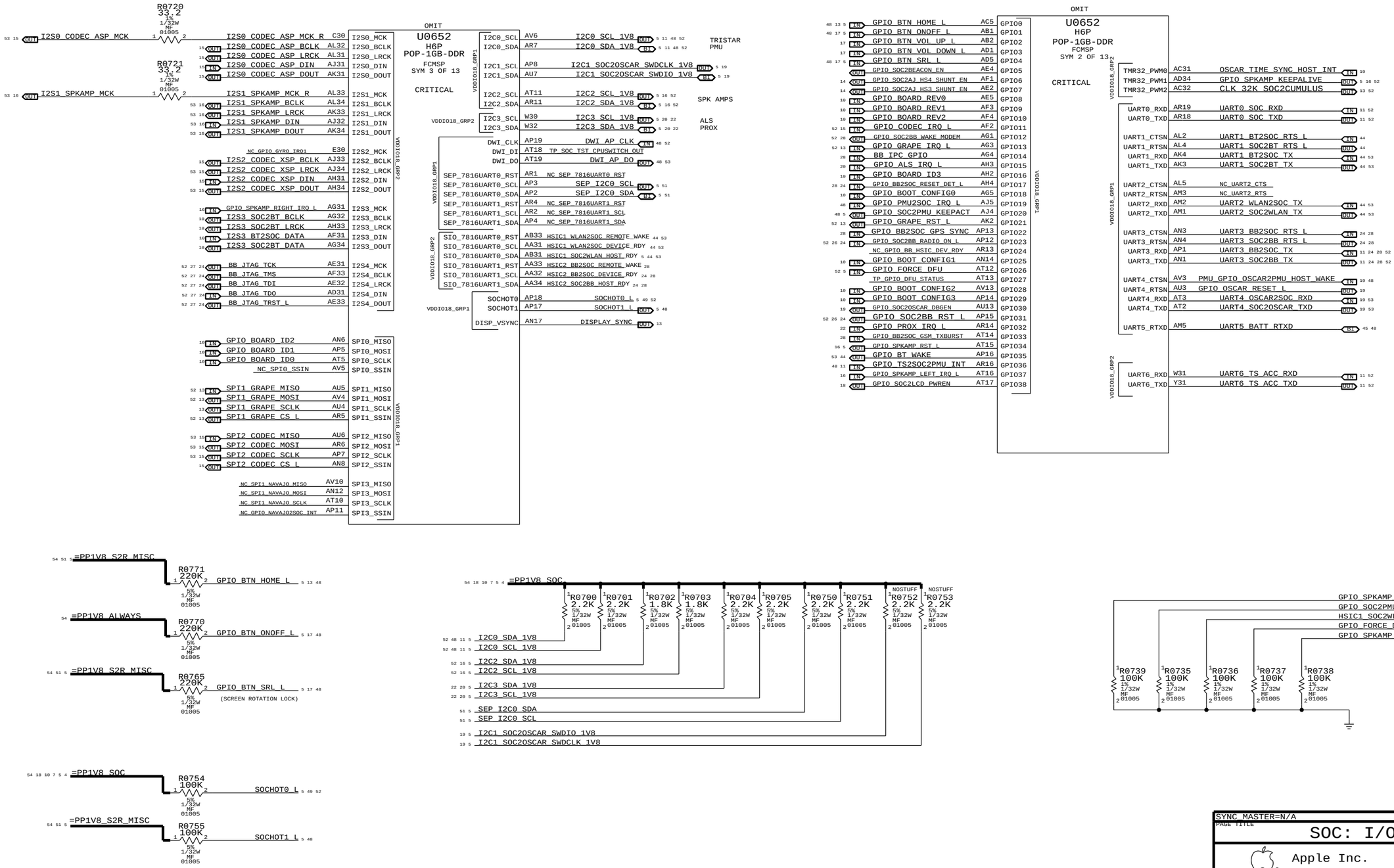
SOC I/OS



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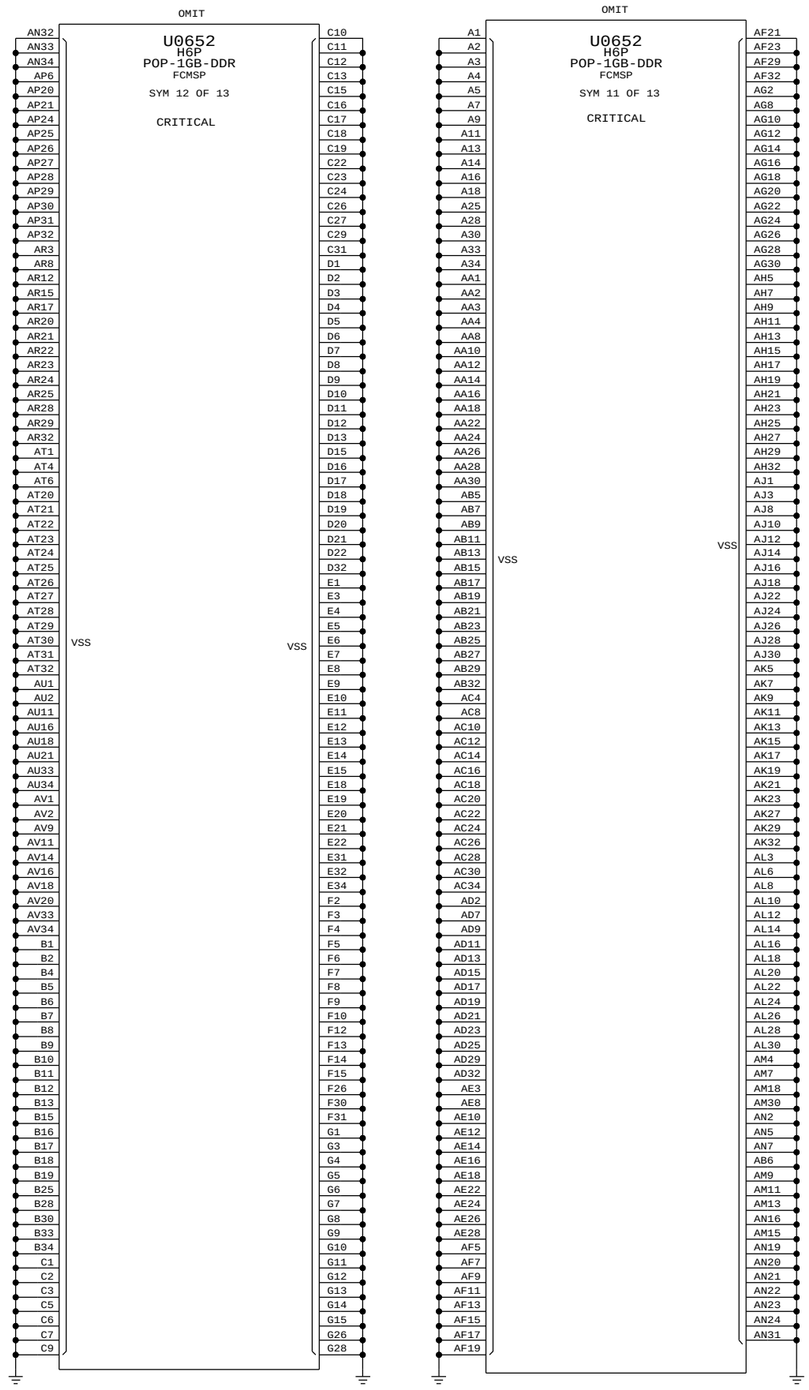

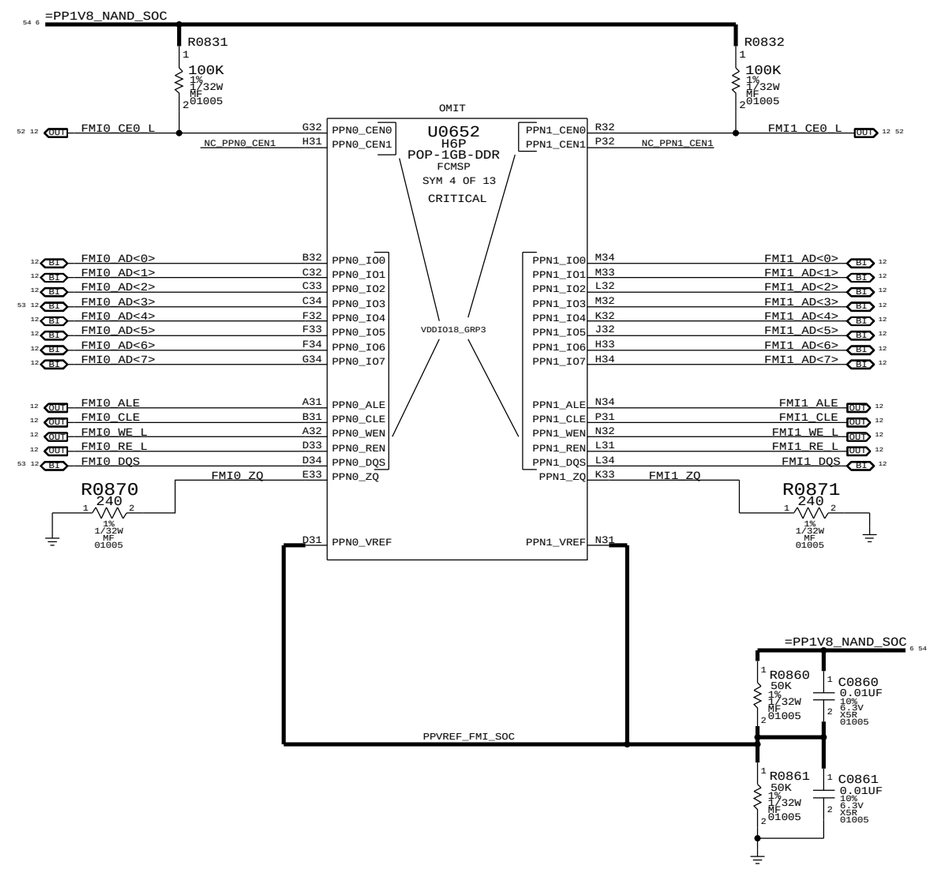

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PAGE TITLE

SOC: NAND

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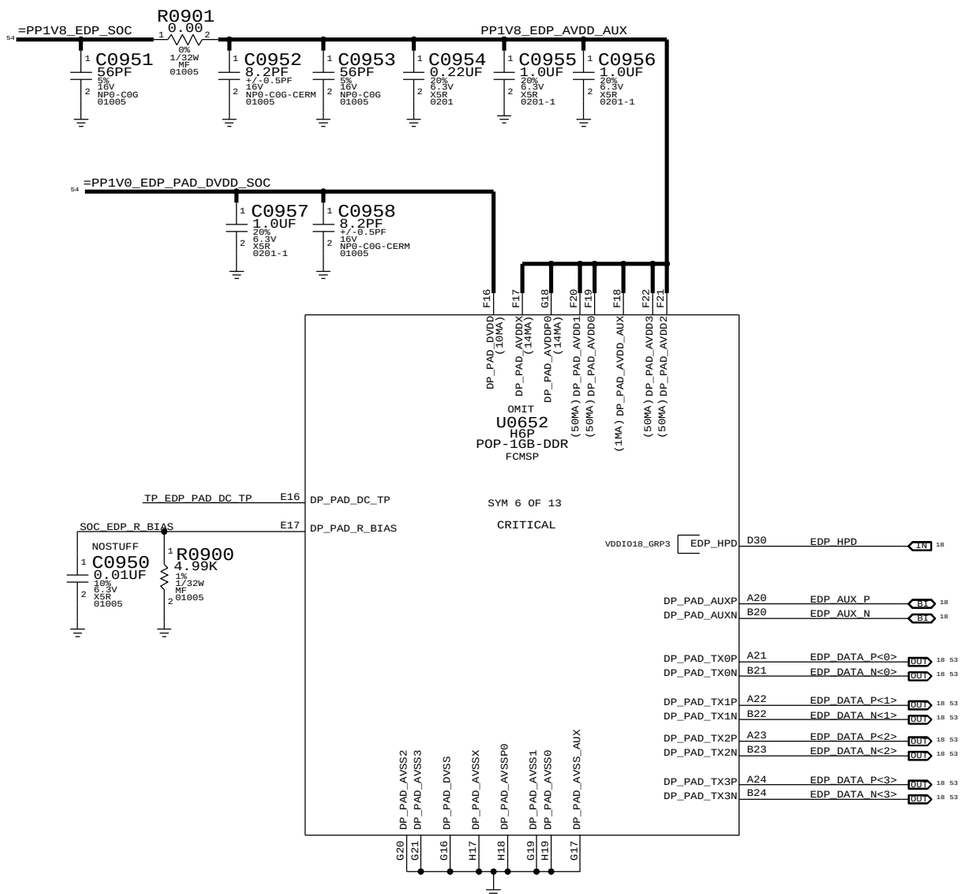

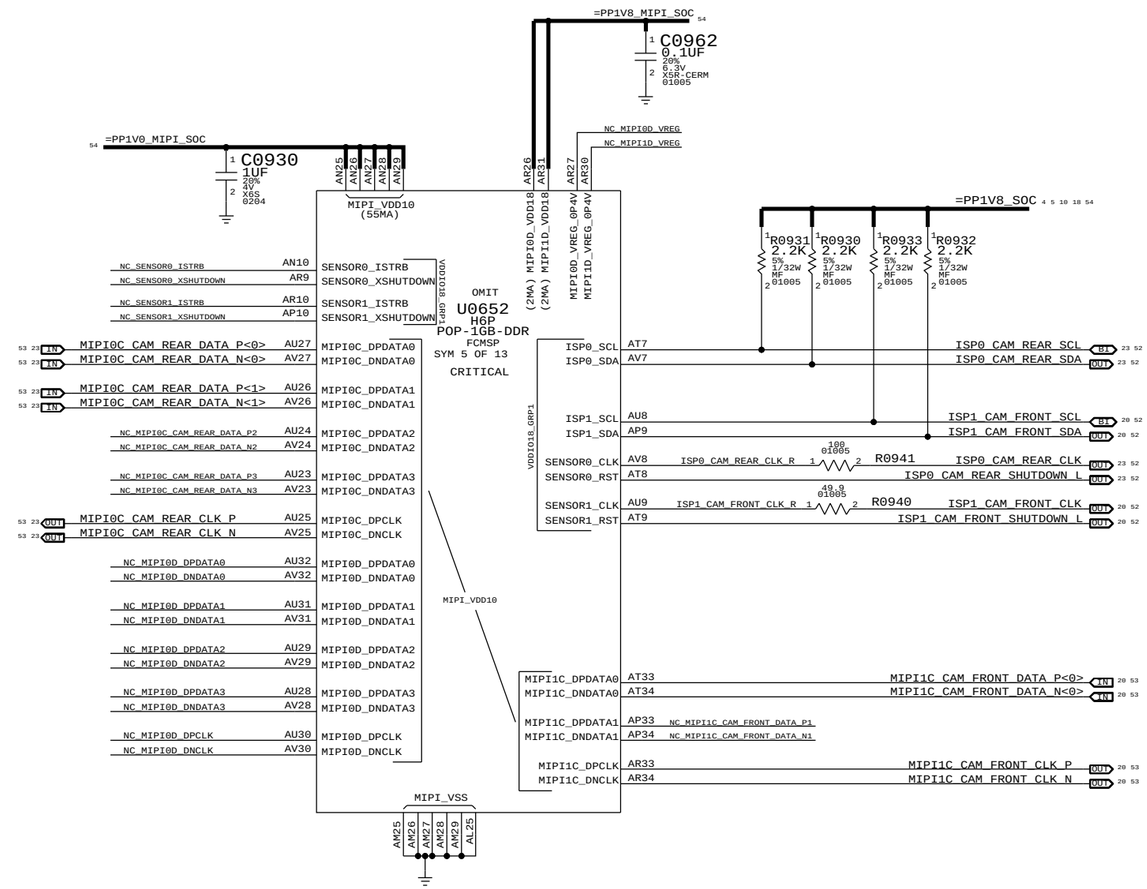

SYNC_MASTER=MLB SYNC_DATE=05/04/2012

PAGE TITLE

SOC: DP,MIPI

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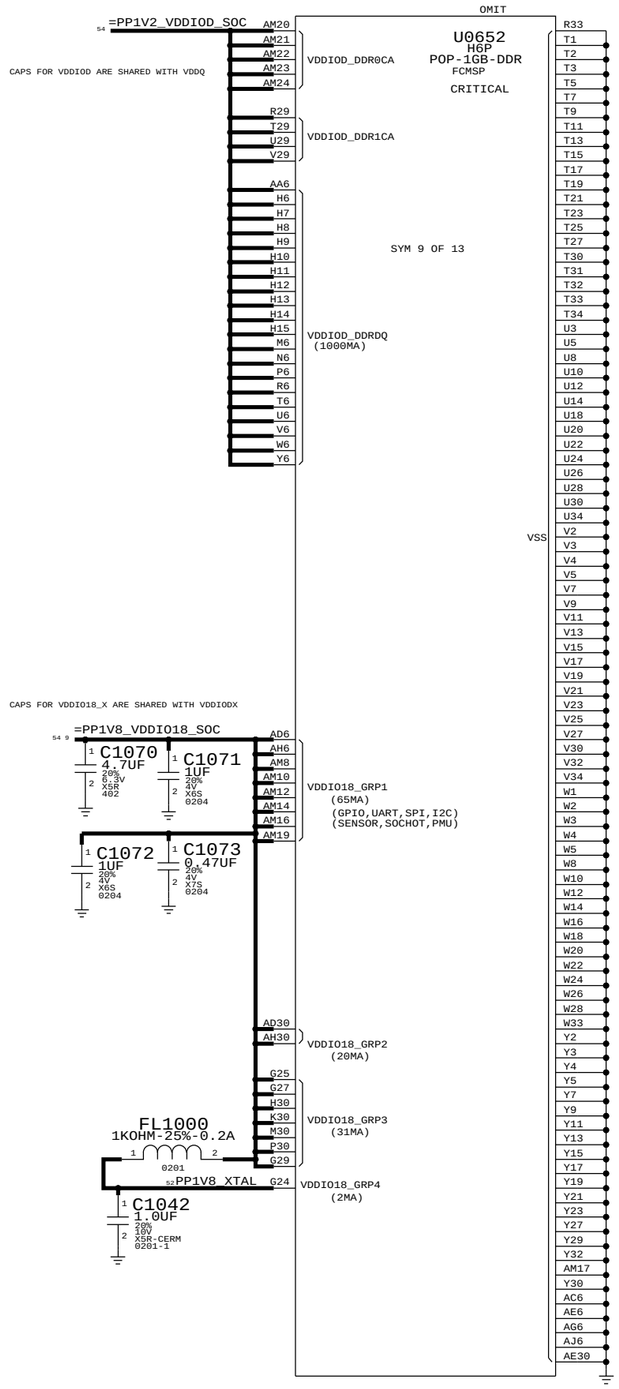

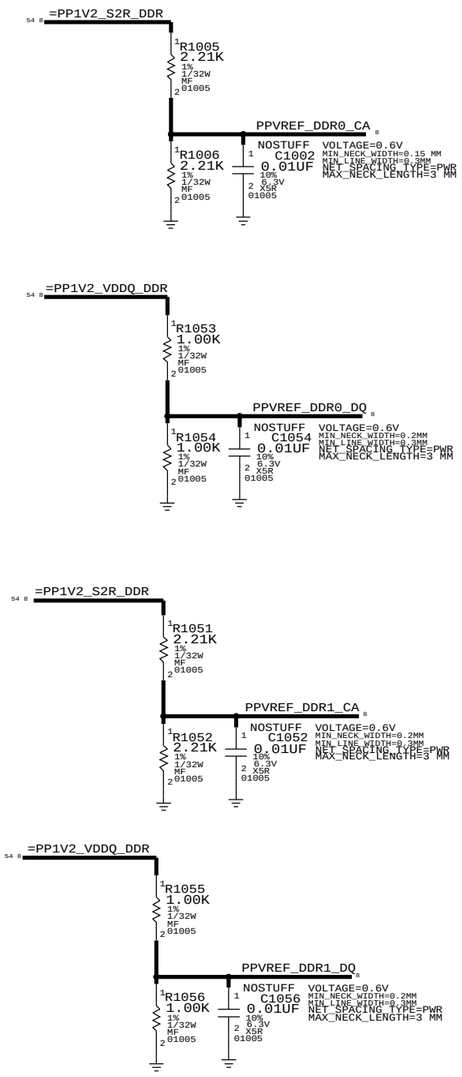

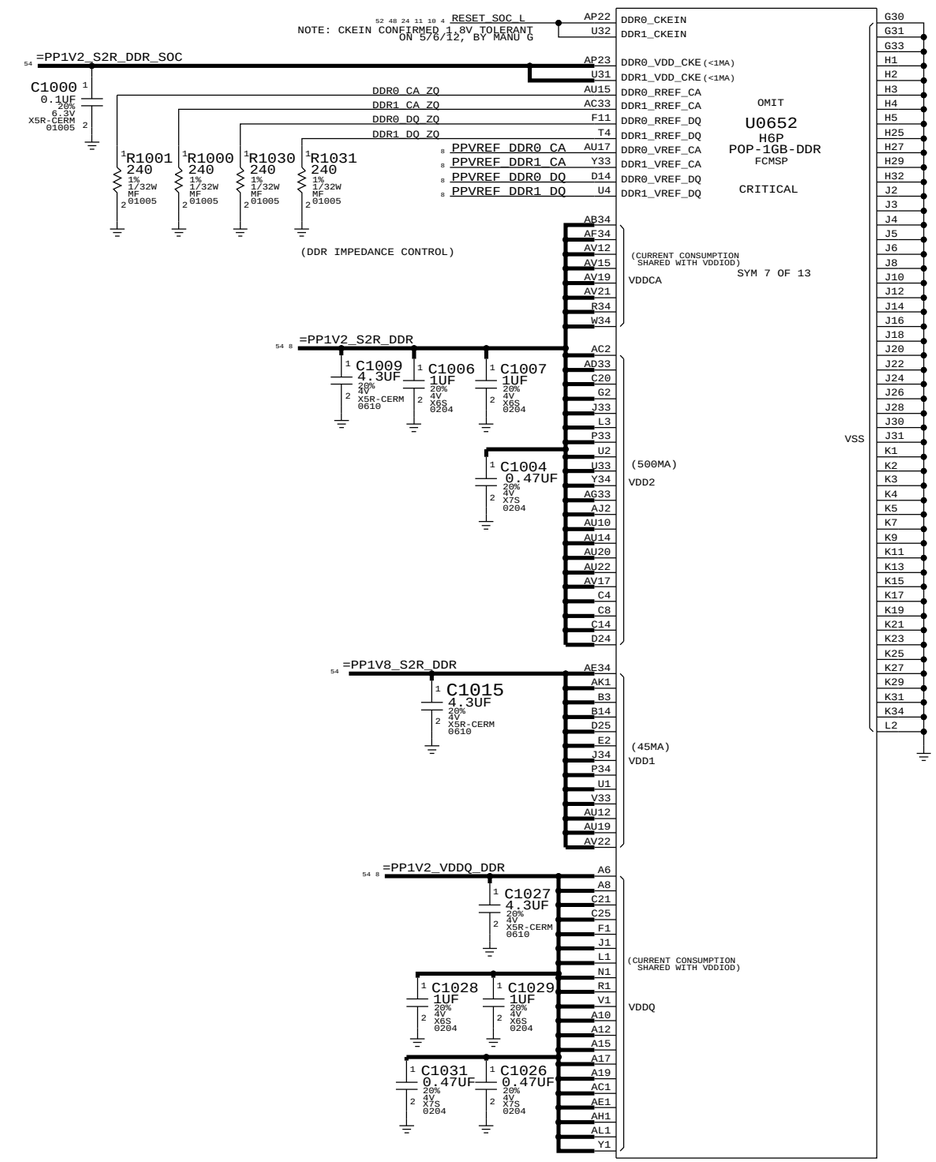

SYNC_MASTER=N/A SYNC_DATE=04/18/2011

PAGE TITLE
SOC: SRAM, IO PWRS

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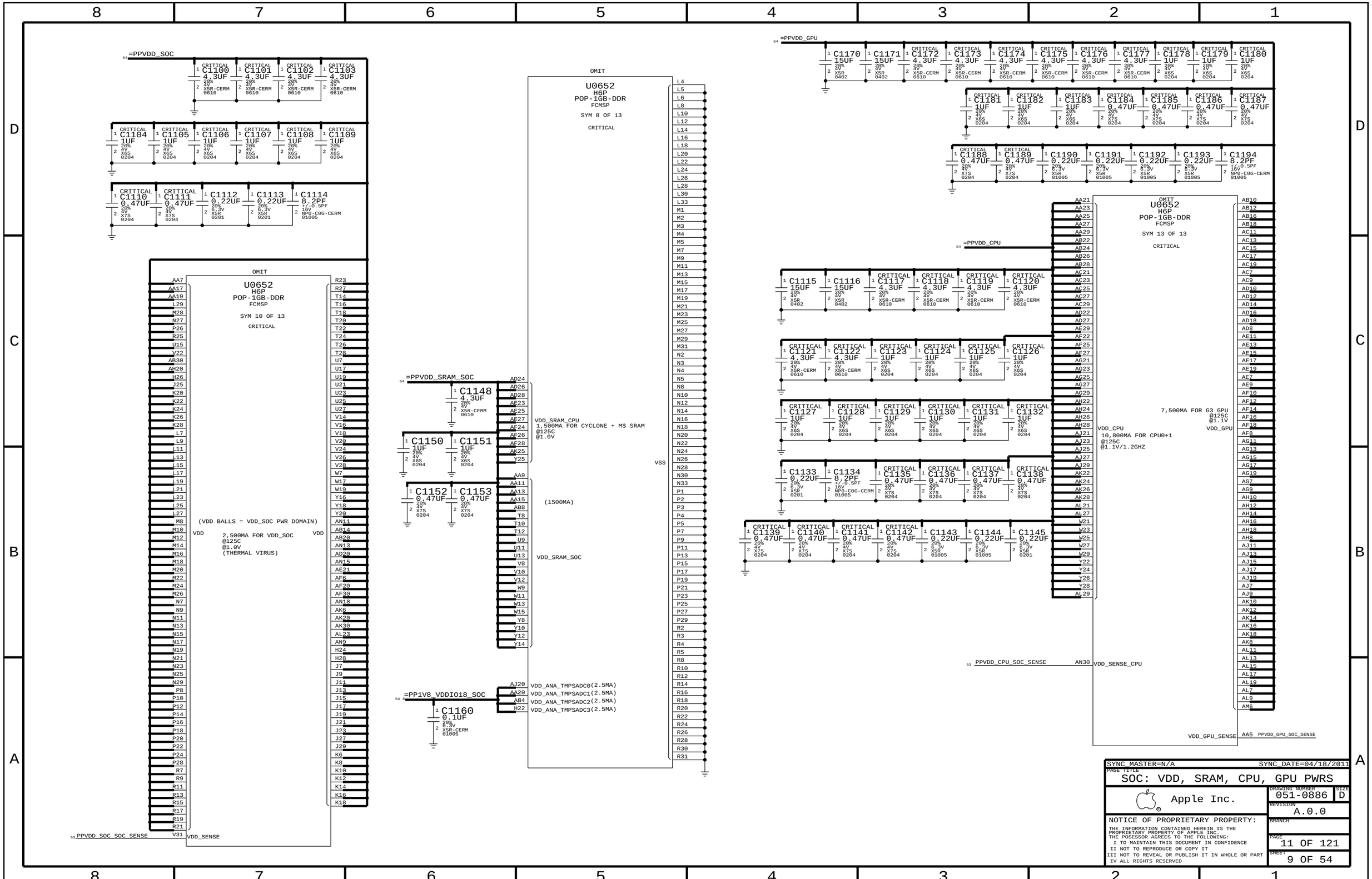

SYNC_MASTER=N/A SYNC_DATE=04/18/2011

PAGE TITLE
SOC: VDD, SRAM, CPU, GPU PWRS

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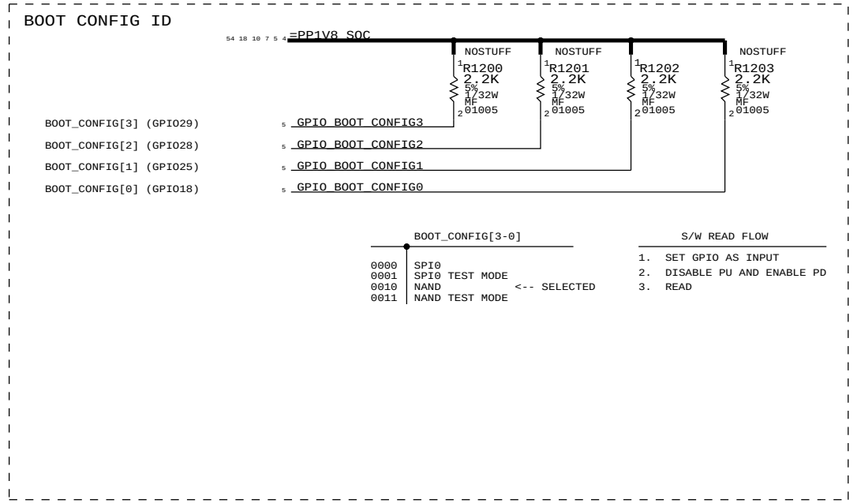

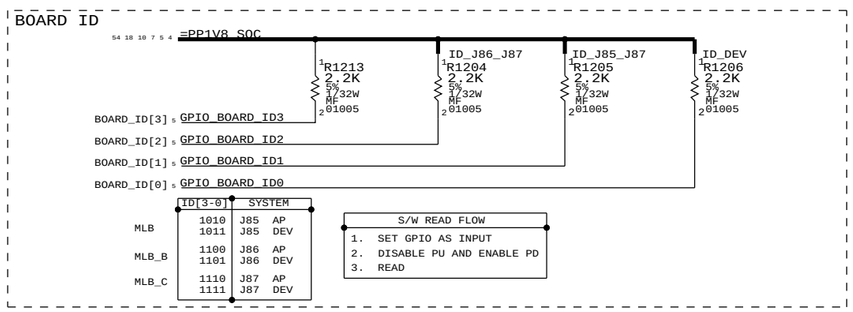

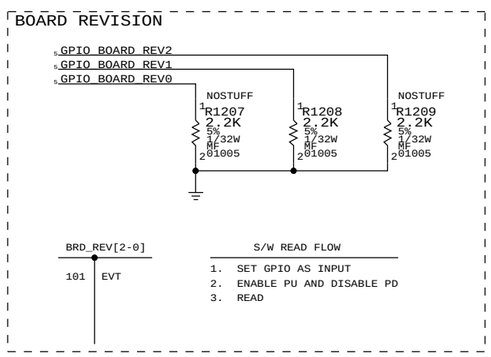

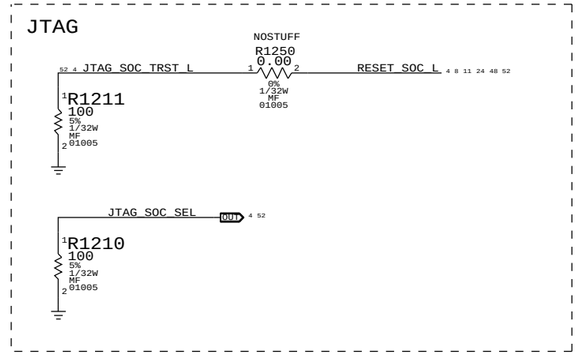

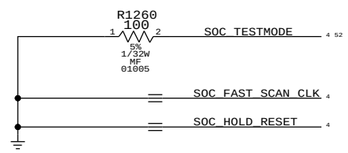

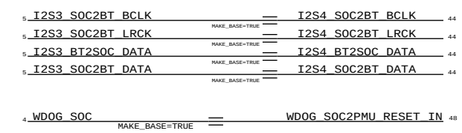

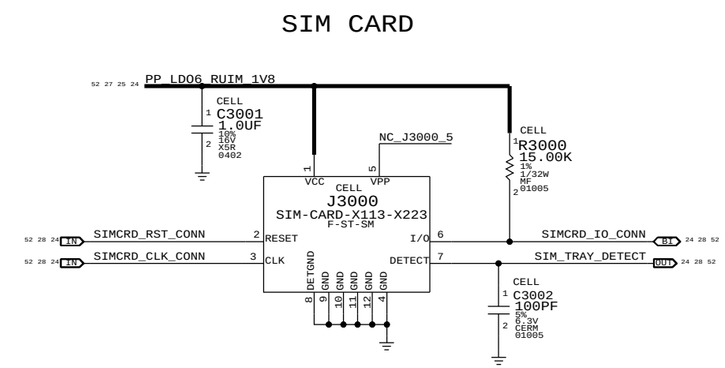

CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

SYNC MASTER=N/A SYNC DATE=04/11/2011

PAGE TITLE
SOC: MISC & ALIASES

Apple Inc.

DRAWING NUMBER 051-0886 SIZE D

REVISION A.0.0

BRANCH

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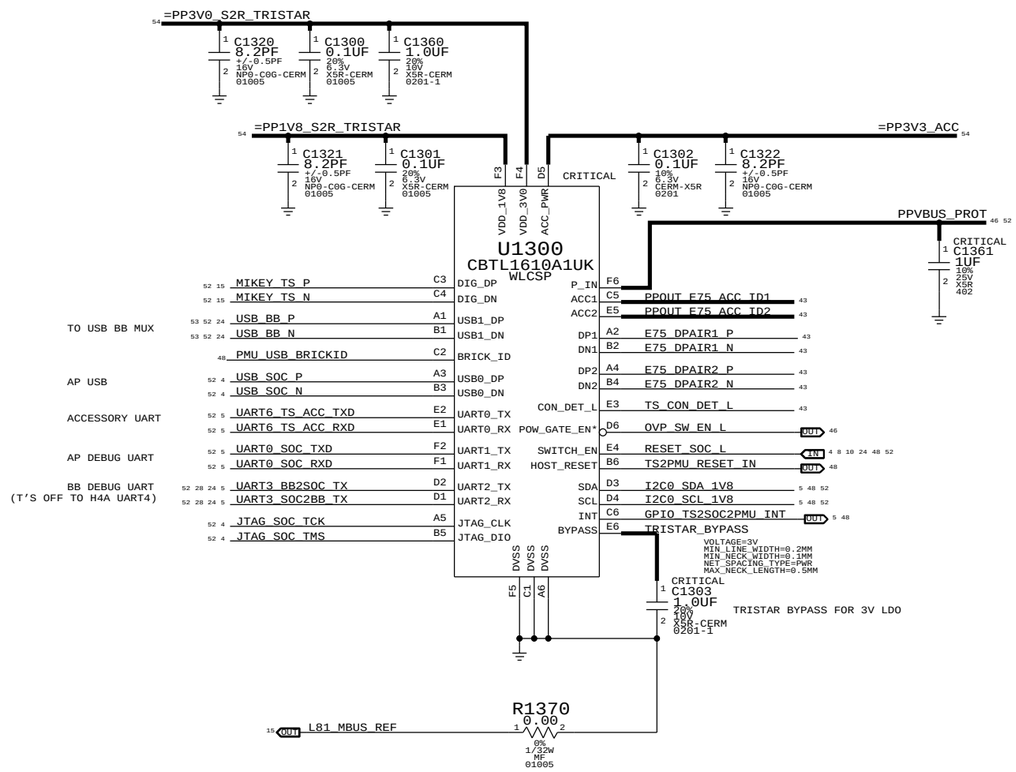
343S0658 = TRISTAR 2, A1
998-5855 = TRISTAR 2, TC
343S0639 = TRISTAR 2, A0
343S0614 = TRISTAR 1

TRISTAR



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Apple Inc.	DRAWING NUMBER 051-0886 SIZE D
	REVISION A.0.0
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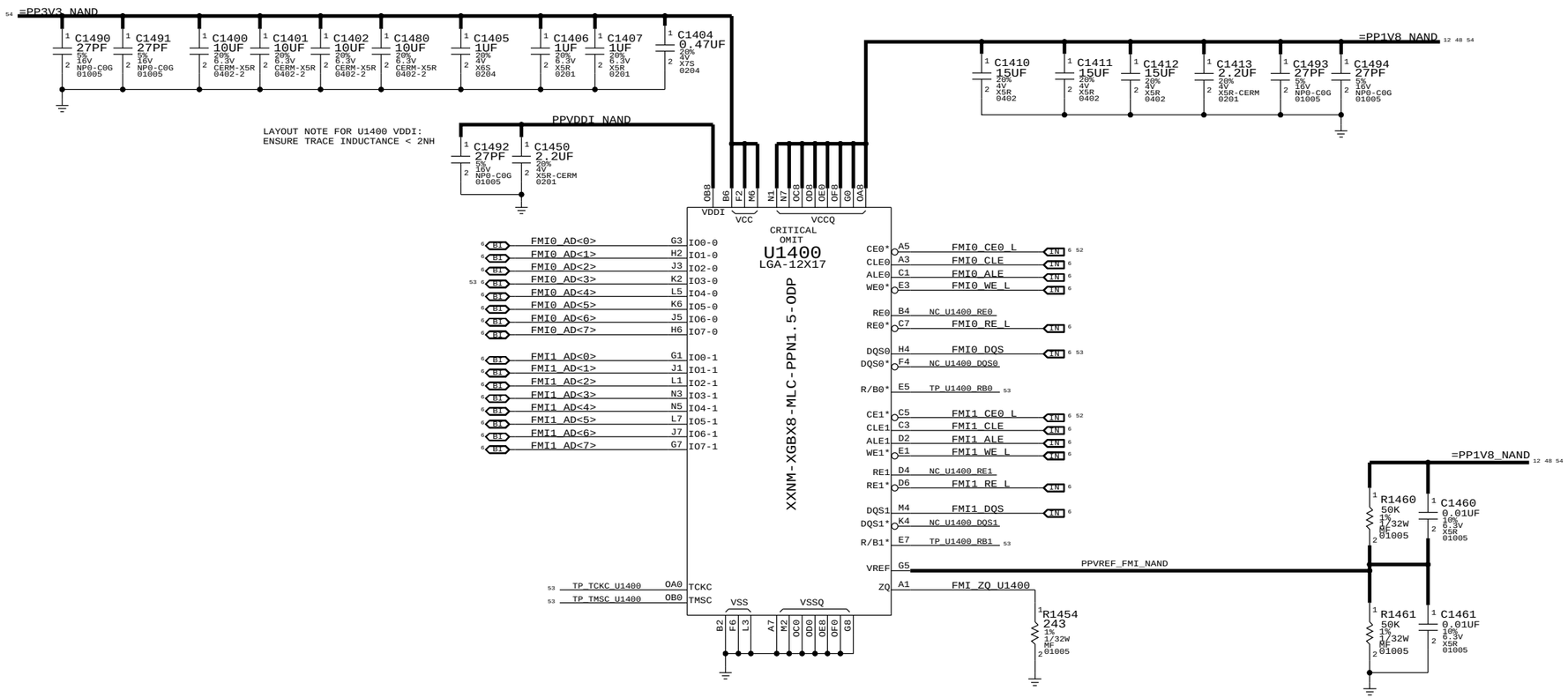
	PAGE 13 OF 121
	SHEET 11 OF 54



SYNC MASTER=MLB SYNC DATE=05/04/2012

PAGE TITLE

NAND STORAGE

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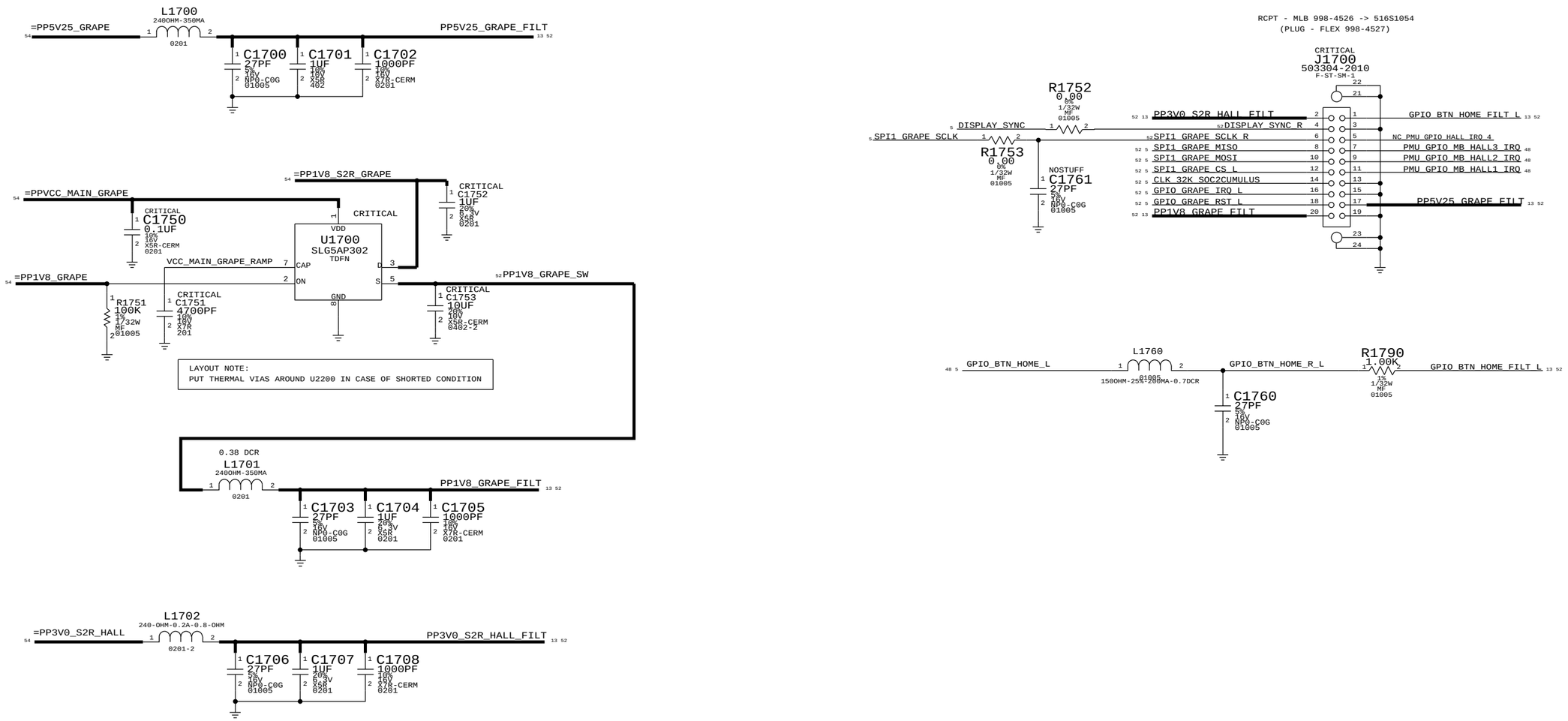
TOUCH SUBSYSTEM



SYNC_MASTER=N/A SYNC_DATE=06/21/2010

PAGE TITLE
TOUCH: SUPPORT CKT & CONN

Apple Inc.

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REVISION A.0.0

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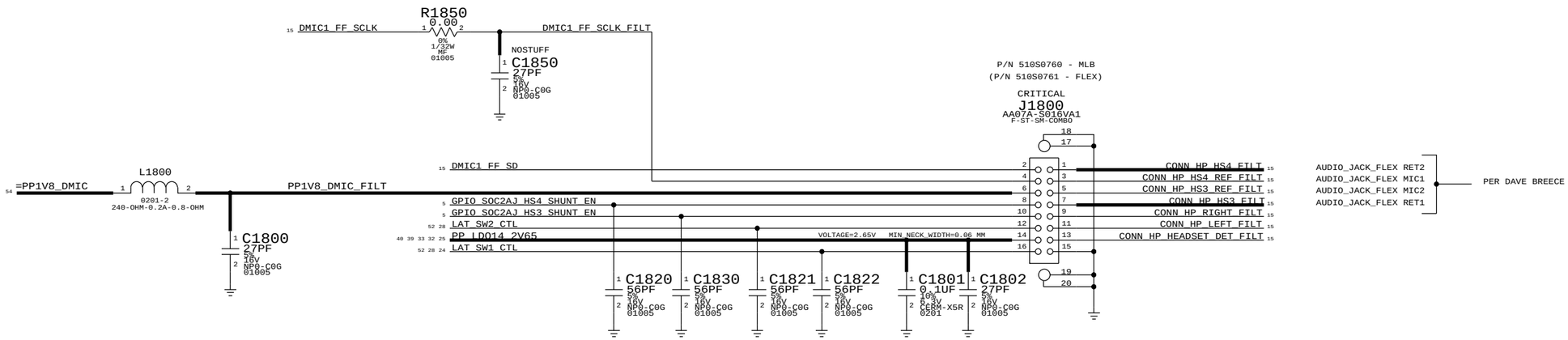

SYNC_MASTER=N/A SYNC_DATE=03/31/2011

PAGE TITLE
AUDIO: HP FLEX CONN

Apple Inc.

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BRANCH 14 OF 54

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SHEET

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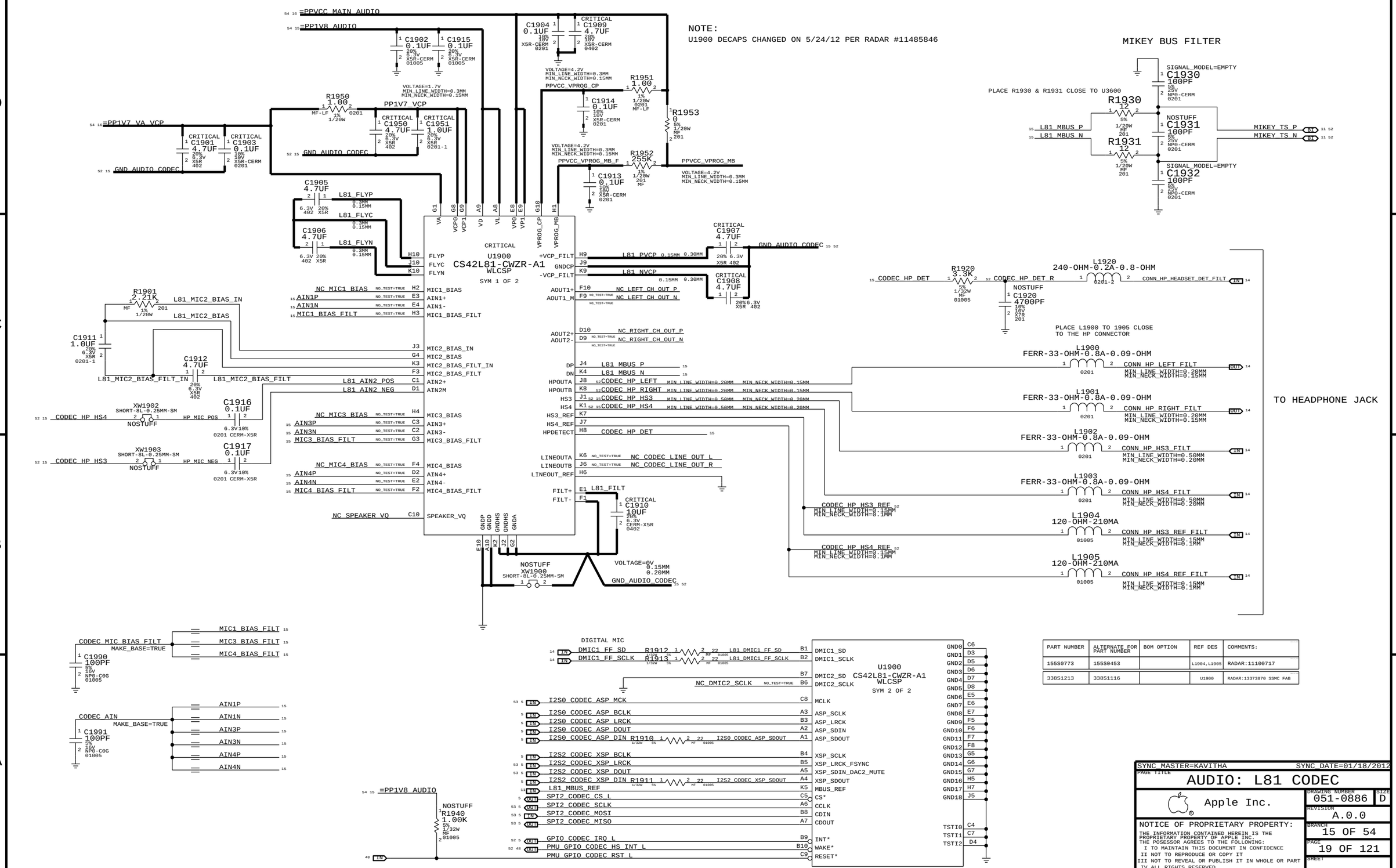

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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338S1213	338S1116		U1900	RADAR:13373870 SSMC FAB

SYNC_MASTER=KAVITHA SYNC_DATE=01/18/2012

PAGE TITLE

AUDIO: L81 CODEC

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SHEET

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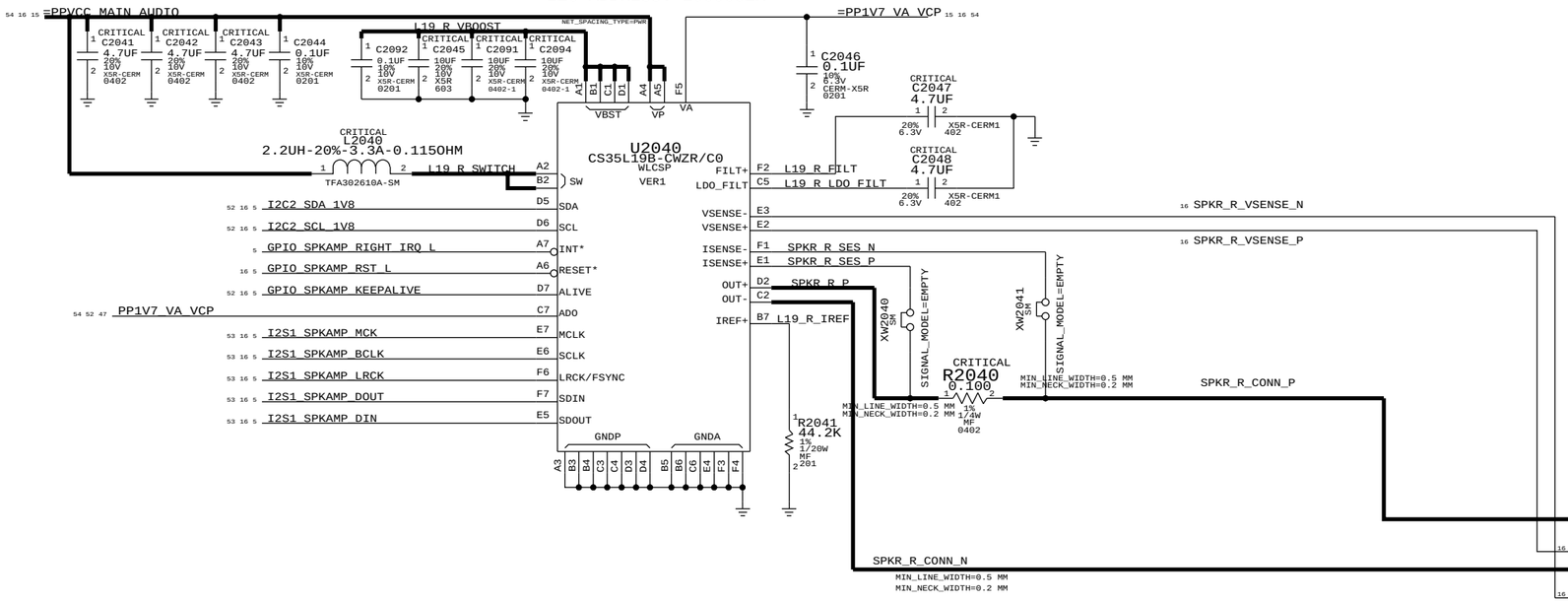
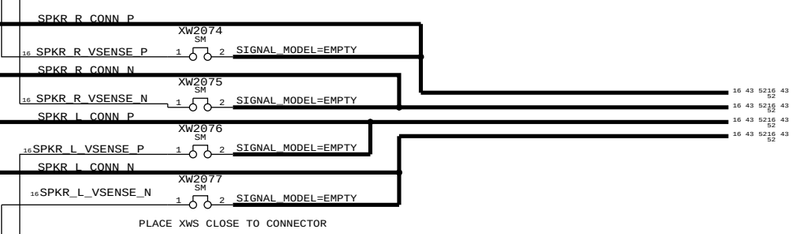
RIGHT SPEAKER AMP

I2C ADDRESS: 1000001X

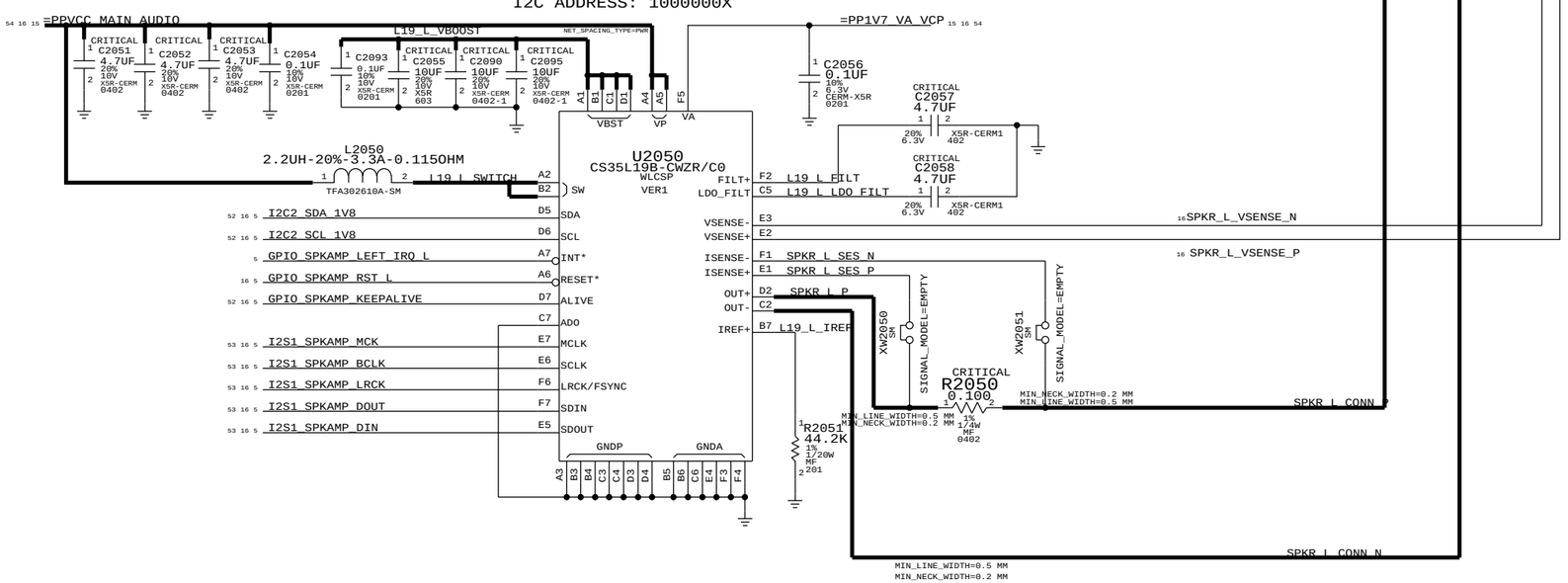


SPEAKER CONNECTOR



LEFT SPEAKER AMP

I2C ADDRESS: 1000000X



UPDATED: DEC 13

1. ALL THE EMI/DESSENSE FILTER COMPONENTS HAVE BEEN REMOVED BASED ON PERFORMANCE ON J65

2. THE CURRENT VERSION OF L19 IS B0 AND WILL CHANGE TO C0 BY MARCH 2013. C0 FIXES PROCESS ISSUES.

SYNC MASTER=KAVITHA SYNC DATE=01/18/2012

PAGE TITLE: AUDIO: CS35L19A AMPS

Apple Inc.

DRAWING NUMBER: 051-0886 SIZE: D

REVISION: A.0.0

BRANCH:

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SHEET: 16 OF 54

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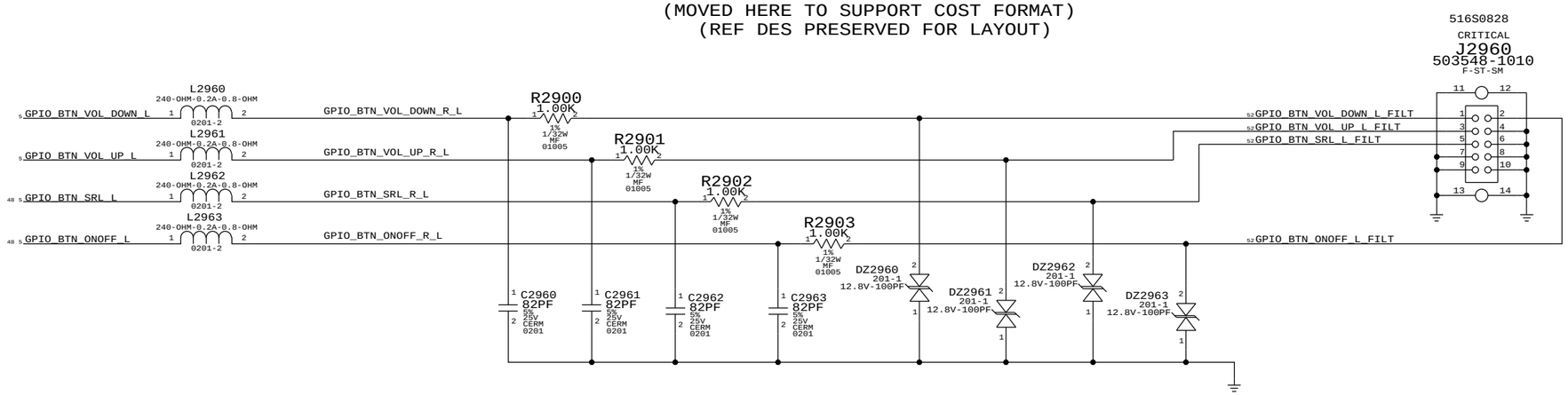
BUTTON CONNECTOR

(MOVED HERE TO SUPPORT COST FORMAT)
(REF DES PRESERVED FOR LAYOUT)



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
BUTTON: CONN

Apple Inc.

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REVISION A.0.0

BRANCH

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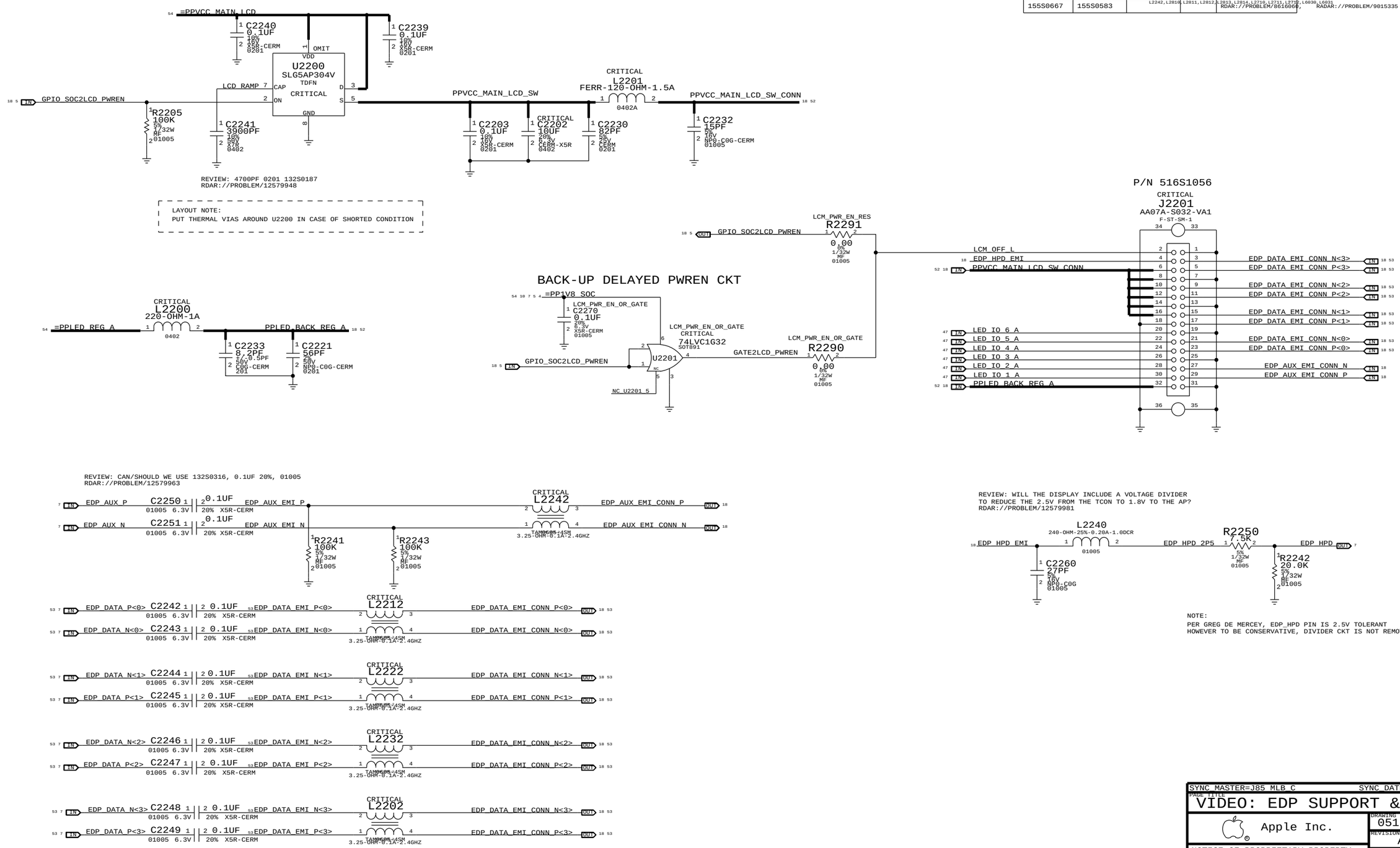
EDP CONNECTOR SUPPORT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0667	155S0583		L2242,L2810,L2811,L2812,L2813,L2814,L2710,L2711,L2712,L6030,L6031	RDAR://PROBLEM/8616060, RDAR://PROBLEM/9015335



SYNC MASTER=J85_MLB_C SYNC DATE=12/05/2012

PAGE TITLE
VIDEO: EDP SUPPORT & CONN

Apple Inc.

DRAWING NUMBER 051-0886 SIZE D

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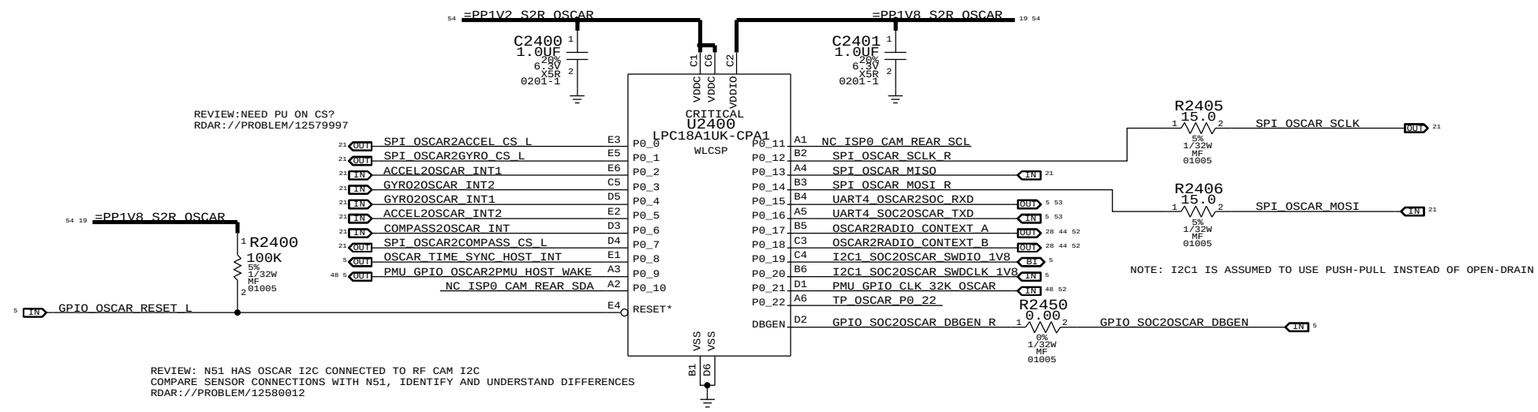
OSCAR

APN 337S4416

OSCAR VDDIO = 1.8V HIBERNATE (NEED TO WAKE HOST)
OSCAR CORE = 1.2V HIBERNATE (NEED TO RUN IN S2R)



NOTE: I2C1 IS ASSUMED TO USE PUSH-PULL INSTEAD OF OPEN-DRAIN

REVIEW: N51 HAS OSCAR I2C CONNECTED TO RF CAM I2C
COMPARE SENSOR CONNECTIONS WITH N51, IDENTIFY AND UNDERSTAND DIFFERENCES
RDAR://PROBLEM/12580012

SYNC_MASTER=J72_MLB_C SYNC_DATE=11/26/2012

PAGE TITLE
SENSOR: OSCAR

Apple Inc.

DRAWING NUMBER 051-0886 SIZE D
REVISION A.0.0
BRANCH
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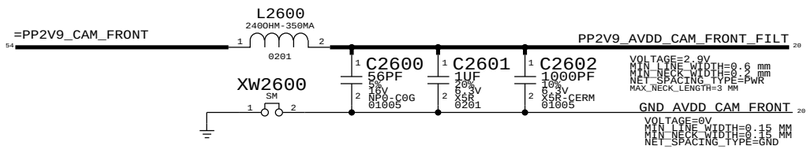
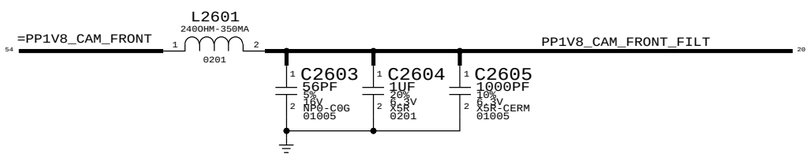
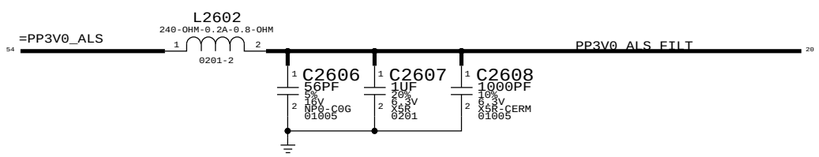
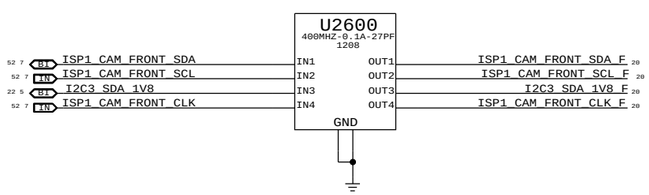
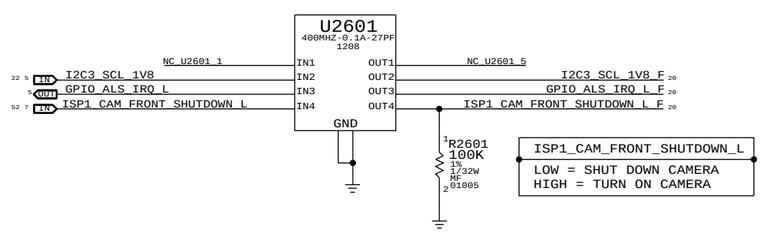
VGA FRONT CAMERA CONNECTOR

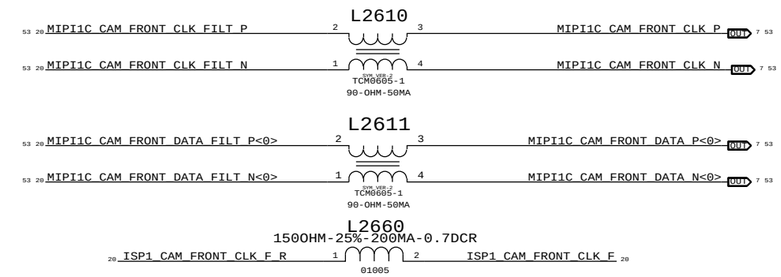


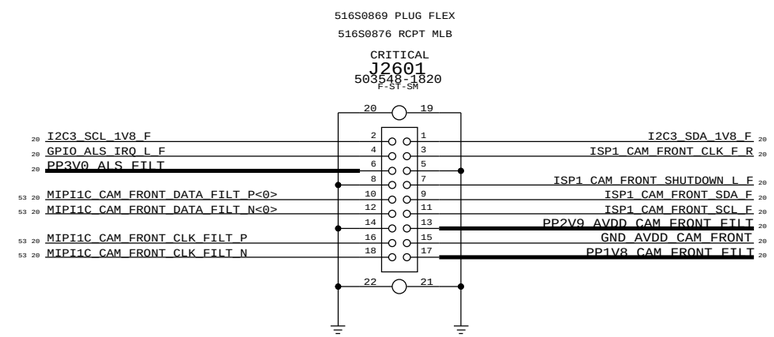












SYNC_MASTER=J85_MLB_C SYNC_DATE=12/03/2012

PAGE TITLE
CAMERA: FF-ALS CONN & FILTERS

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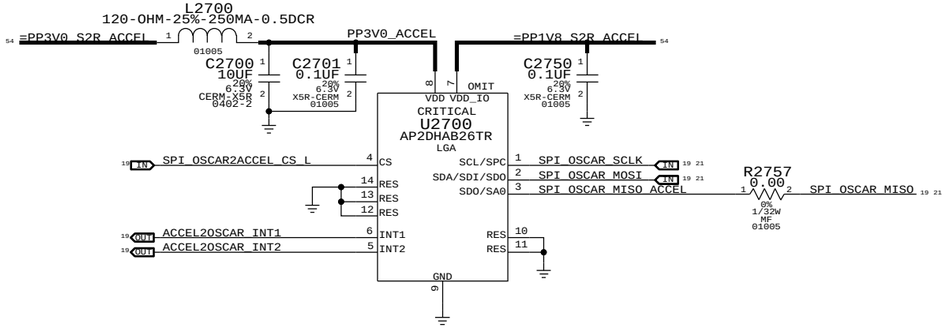
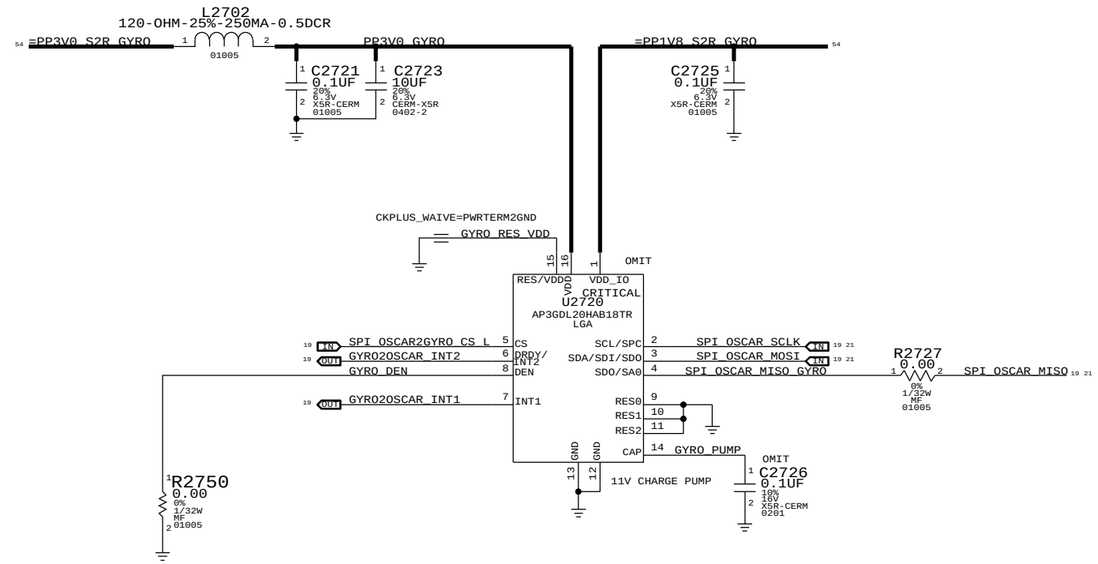
ACCELEROMETER

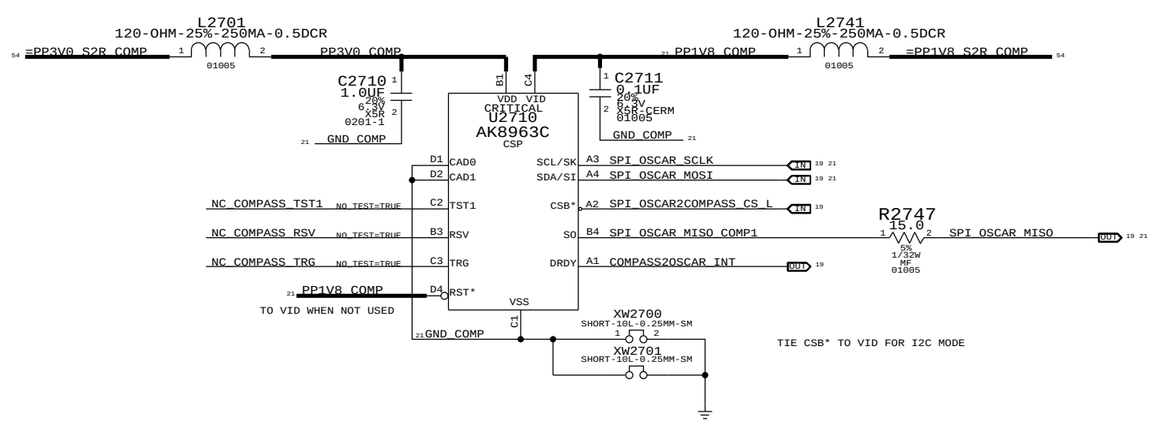


GYRO



COMPASS

APN 338S1014



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
SENSOR: ACCEL, COMPASS, GYRO

Apple Inc.

DRAWING NUMBER 051-0886 SIZE D

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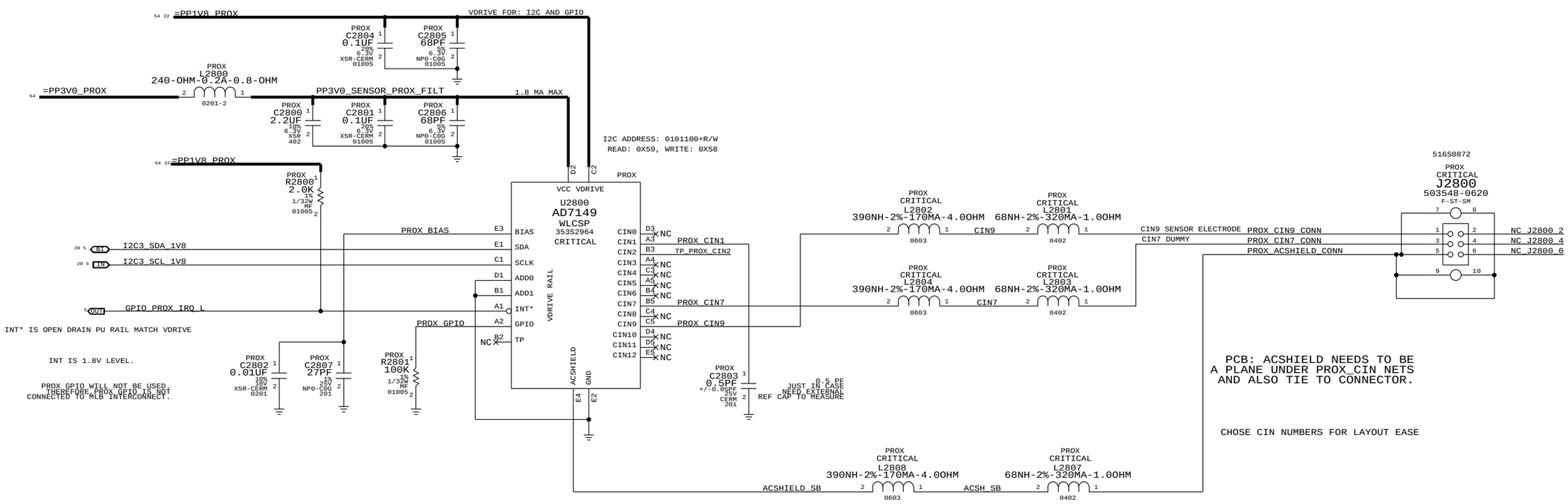
PROX SENSOR



SYNC MASTER=J85 MLB C SYNC DATE=12/05/12

PAGE TITLE: SENSOR: PROX

Apple Inc.

DRAWING NUMBER: 051-0886 SIZE: D

REVISION: A.0.0

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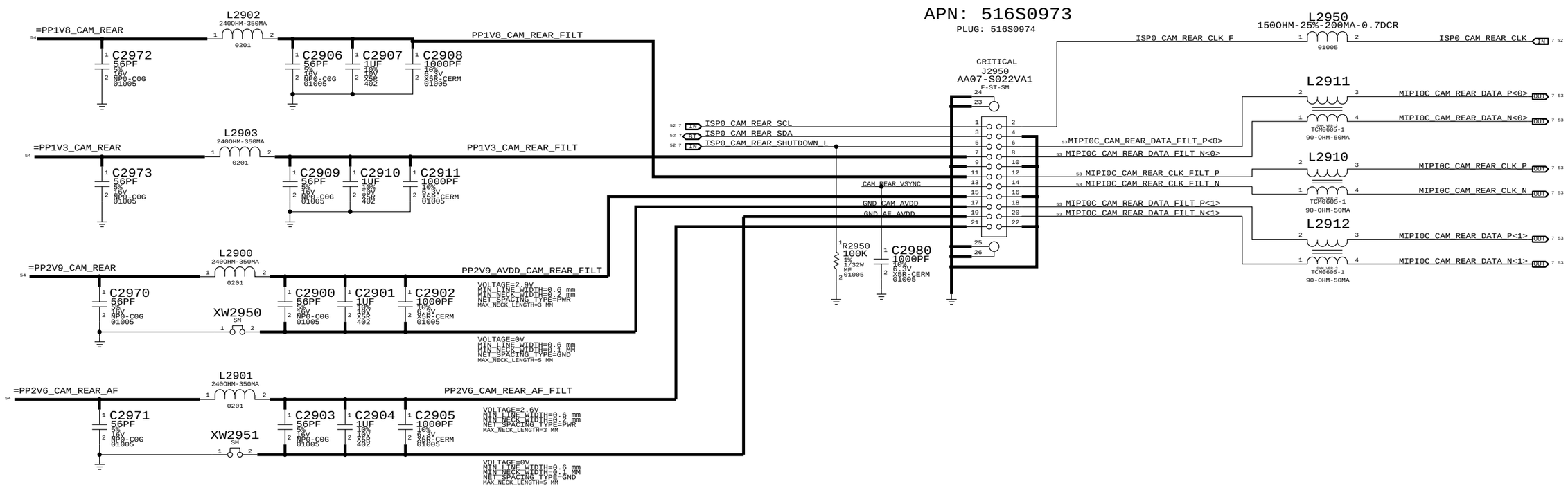
REAR CAMERA CONNECTOR



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
CAMERA: REAR CONN & FILTERS

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DRAWING NUMBER 051-0886 SIZE D

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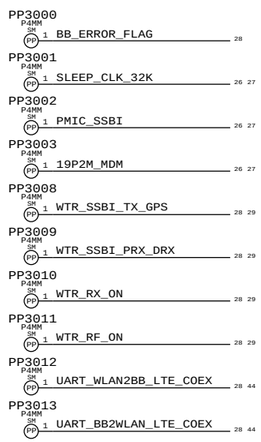
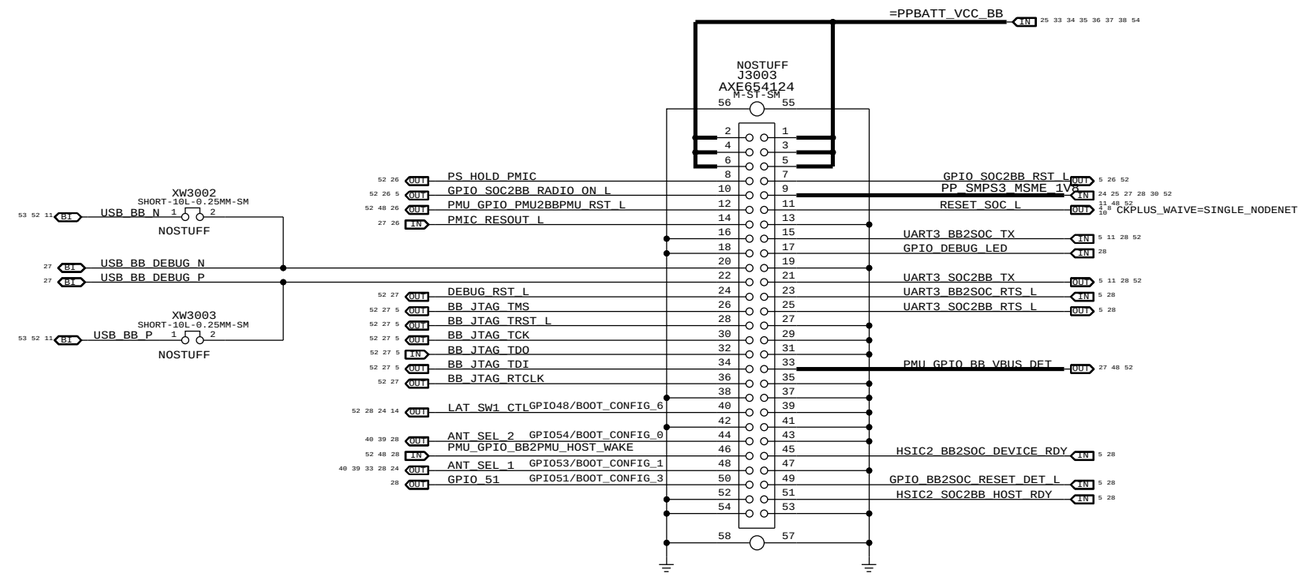
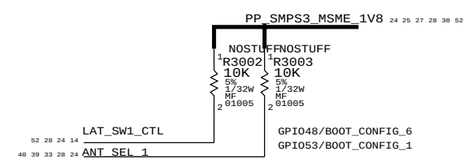
AP INTERFACE & DEBUG CONNECTORS

PROBE POINTS

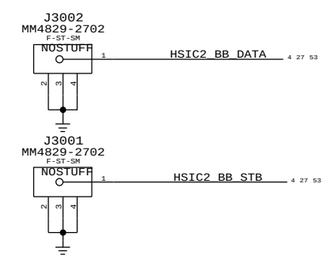


DEBUG CONNECTOR





BOOT OPTIONS	BOOT_CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION							
			6	5	4	3	2	1	0
		47	48	49	50	51	52	53	54	55
BOOT_DEFAULT_OPTION	0X00	X	0	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0X01	X	1	0	0	0	0	0	1	X
BOOT_HSIC_OPTION	0X02	X	1	0	0	0	0	1	0	X
BOOT_USB_OPTION	0X03	X	1	0	0	0	0	1	1	X
ENABLE SAHARA PROTOCOL	0X08	X	1	0	0	1	0	X	X	X



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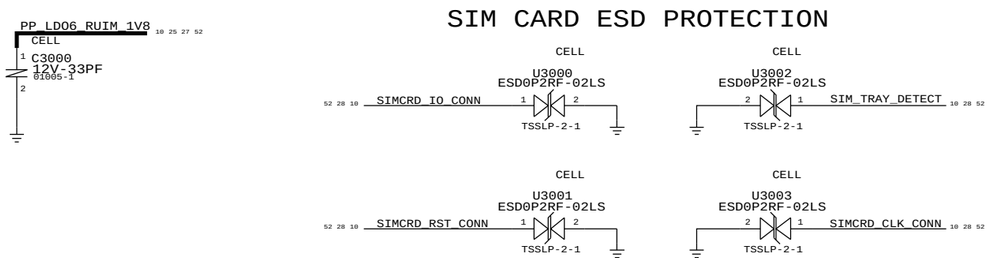

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PAGE TITLE
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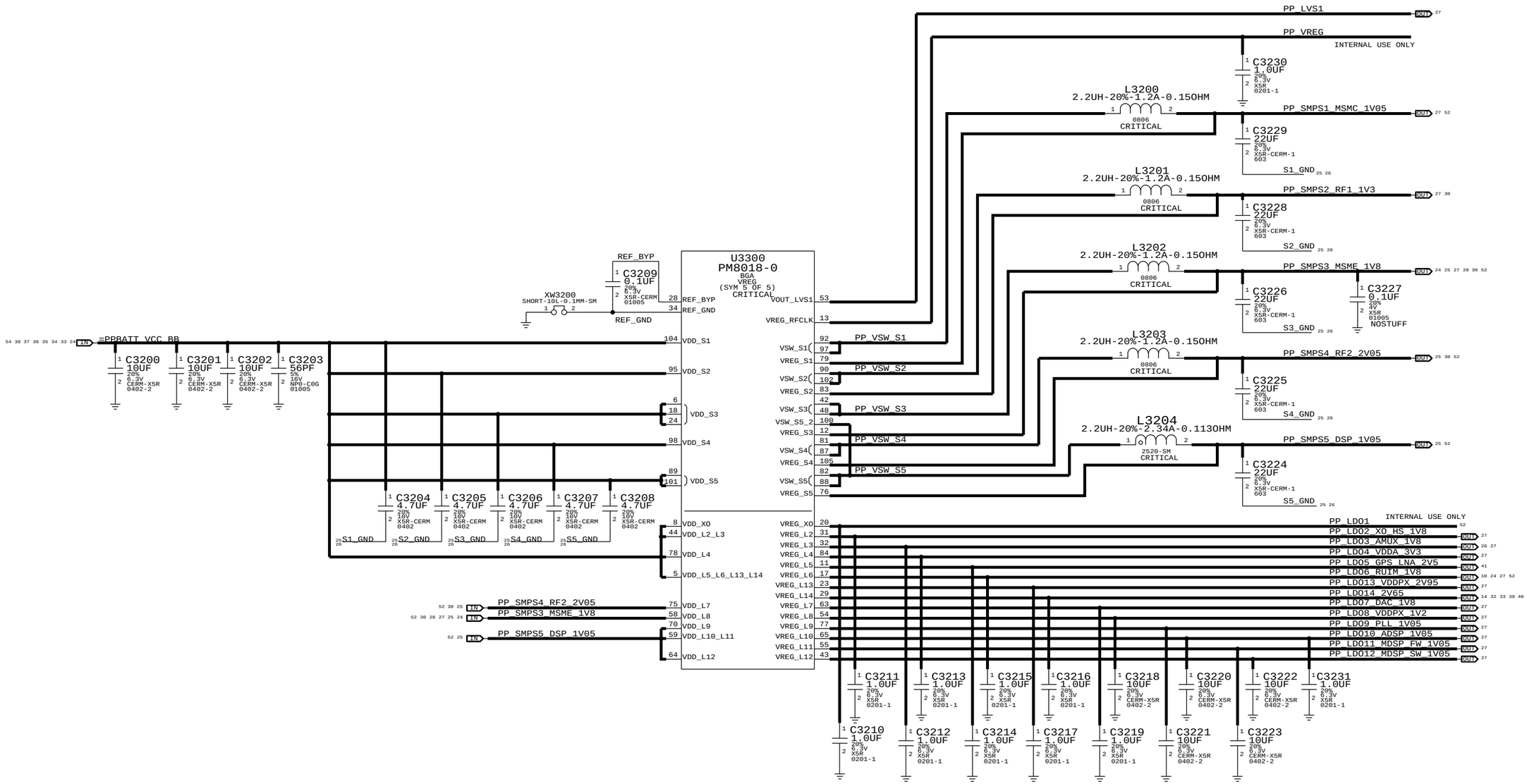
PMU (1 OF 2)



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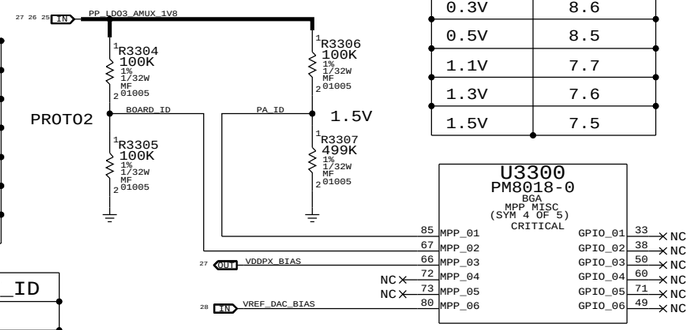
PMU (2 OF 2)

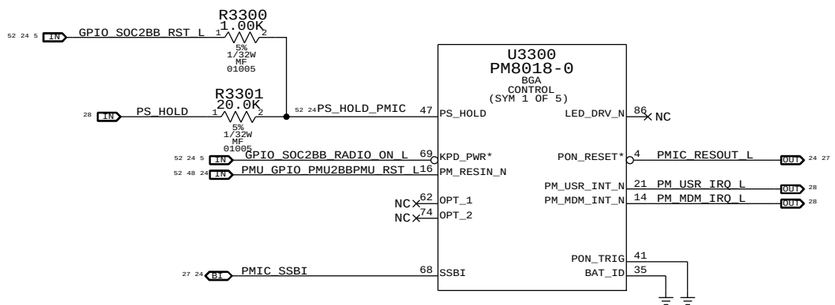
BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT

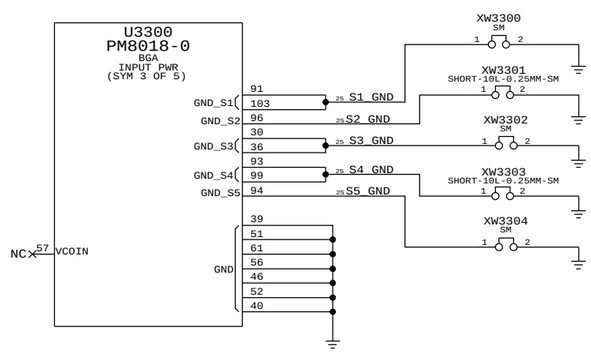
BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX

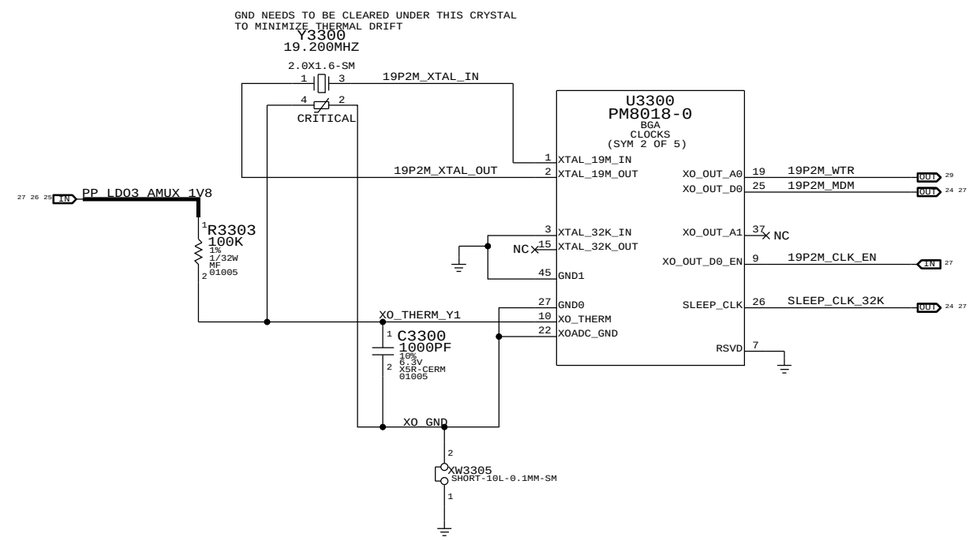
PA_ID	MAV VER
0.1V	8.7
0.3V	8.6
0.5V	8.5
1.1V	7.7
1.3V	7.6
1.5V	7.5



AP SECTION NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.







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BASEBAND (1 OF 2)

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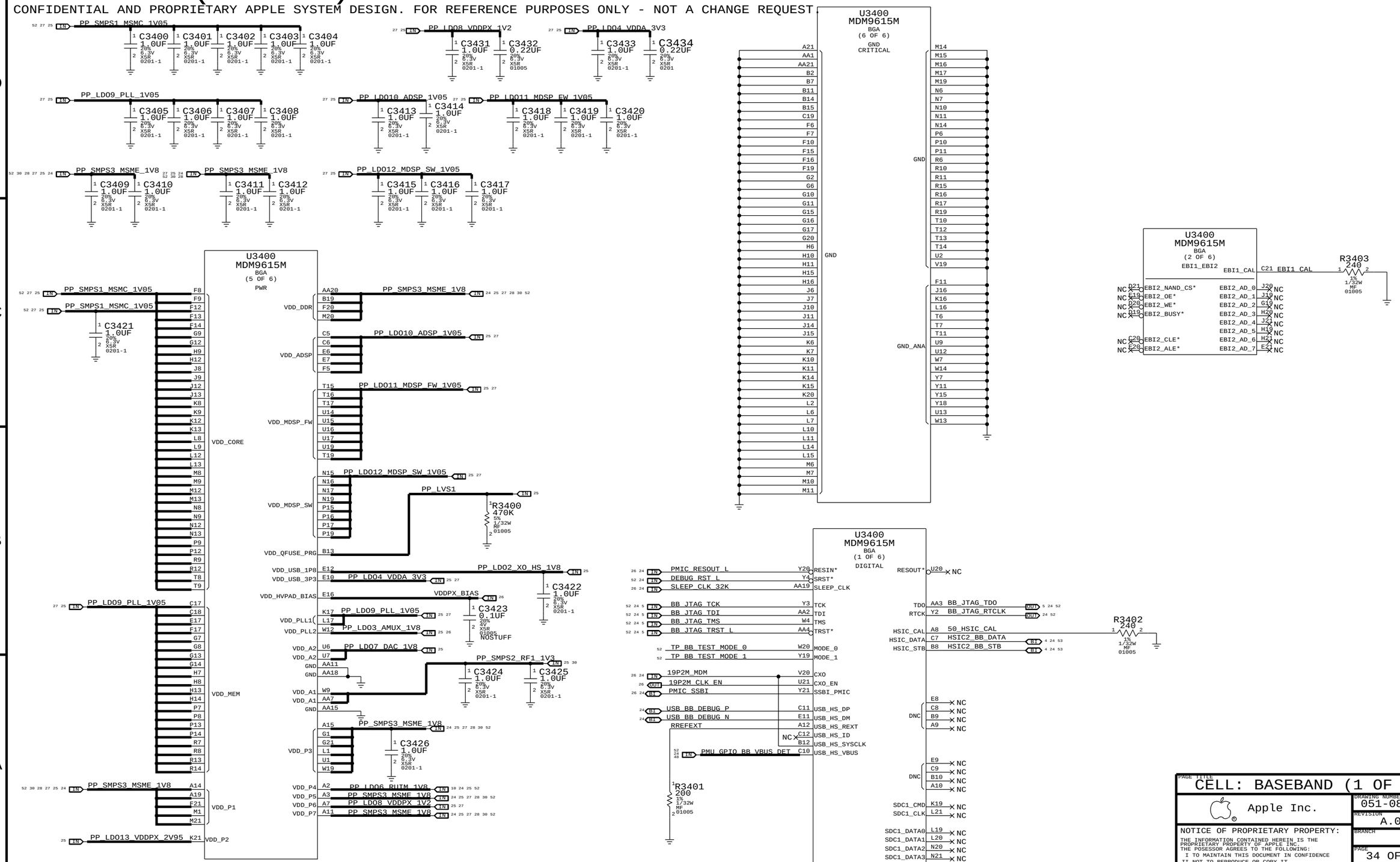

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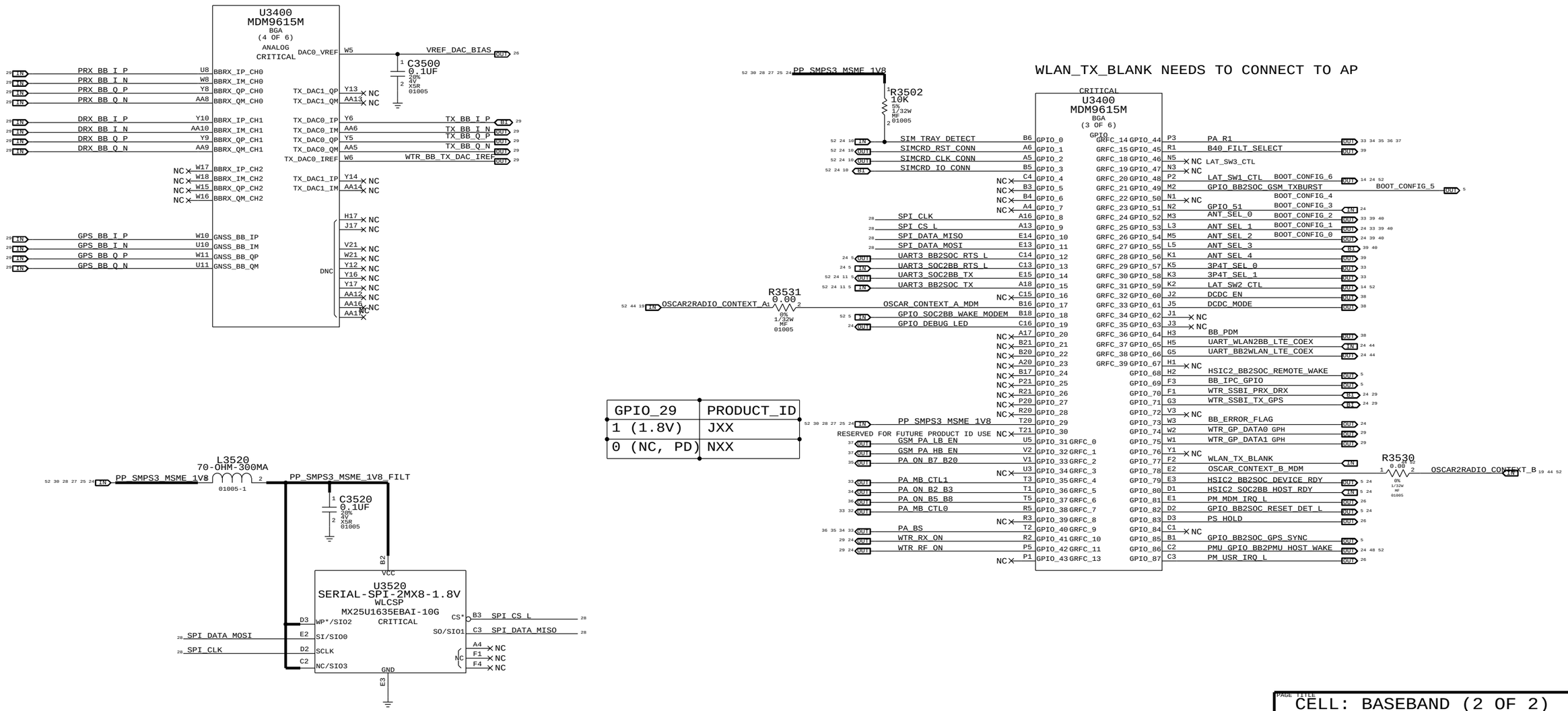
BASEBAND (2 OF 2)



GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX

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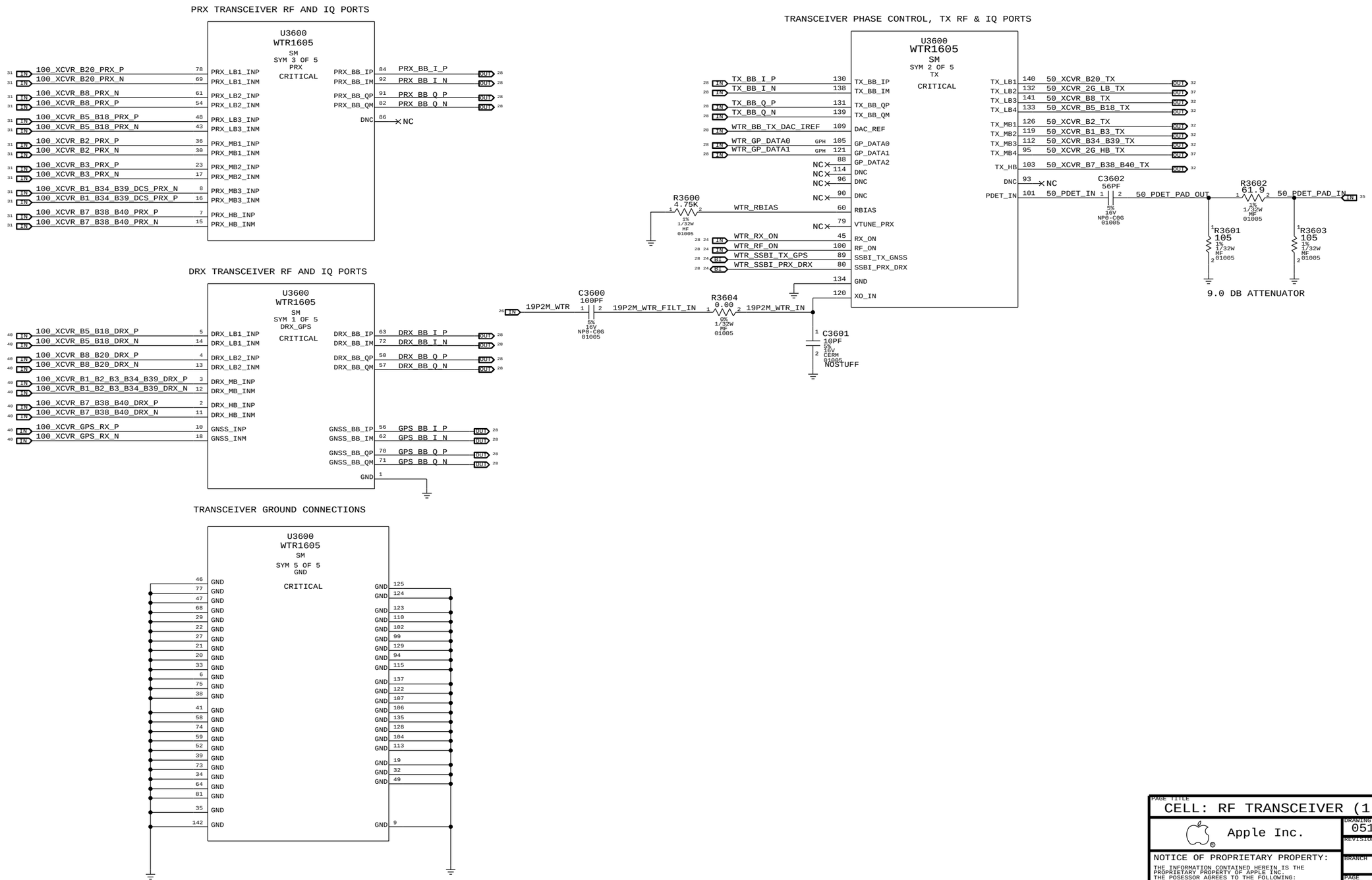
RF TRANSCEIVER (1 OF 2)



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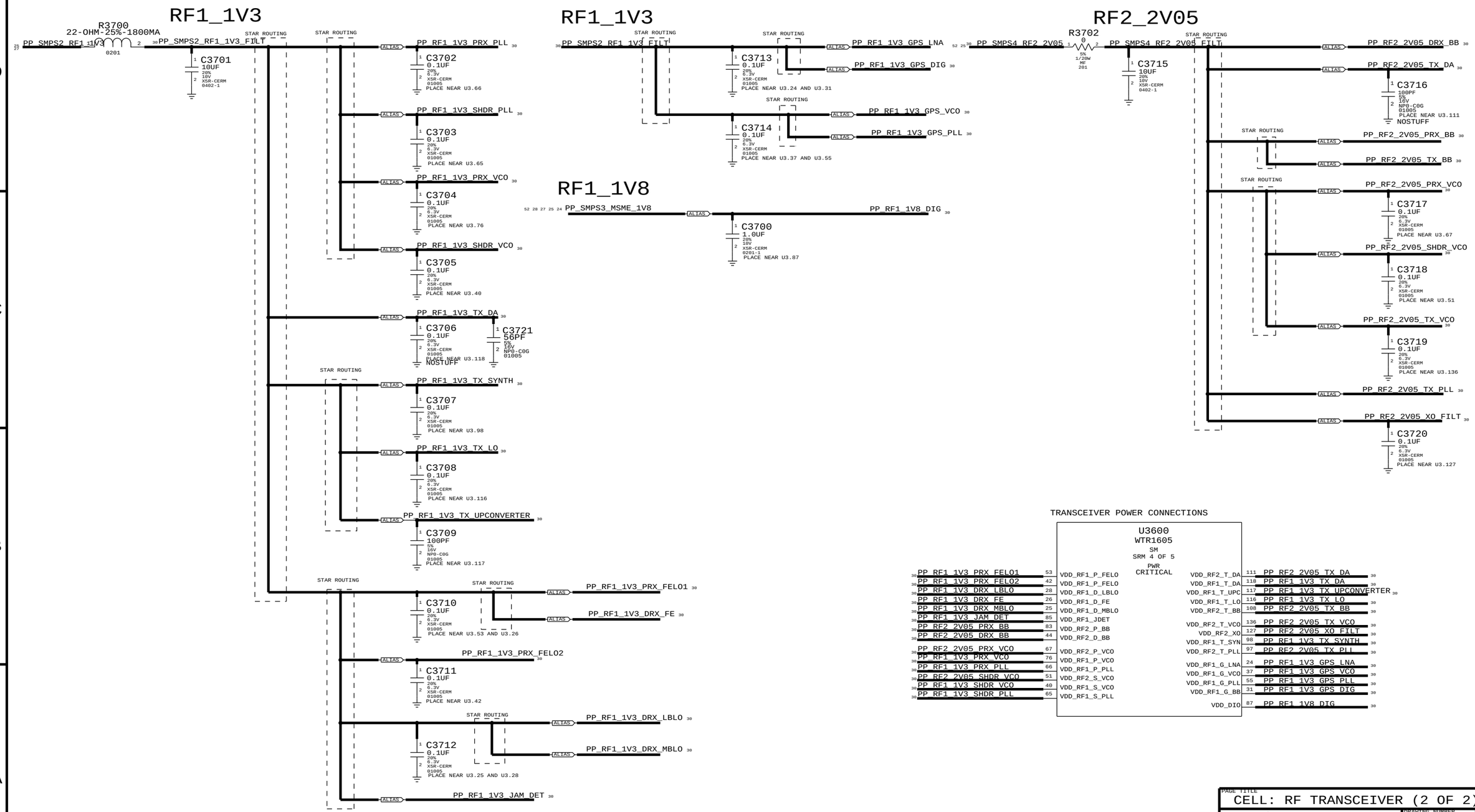

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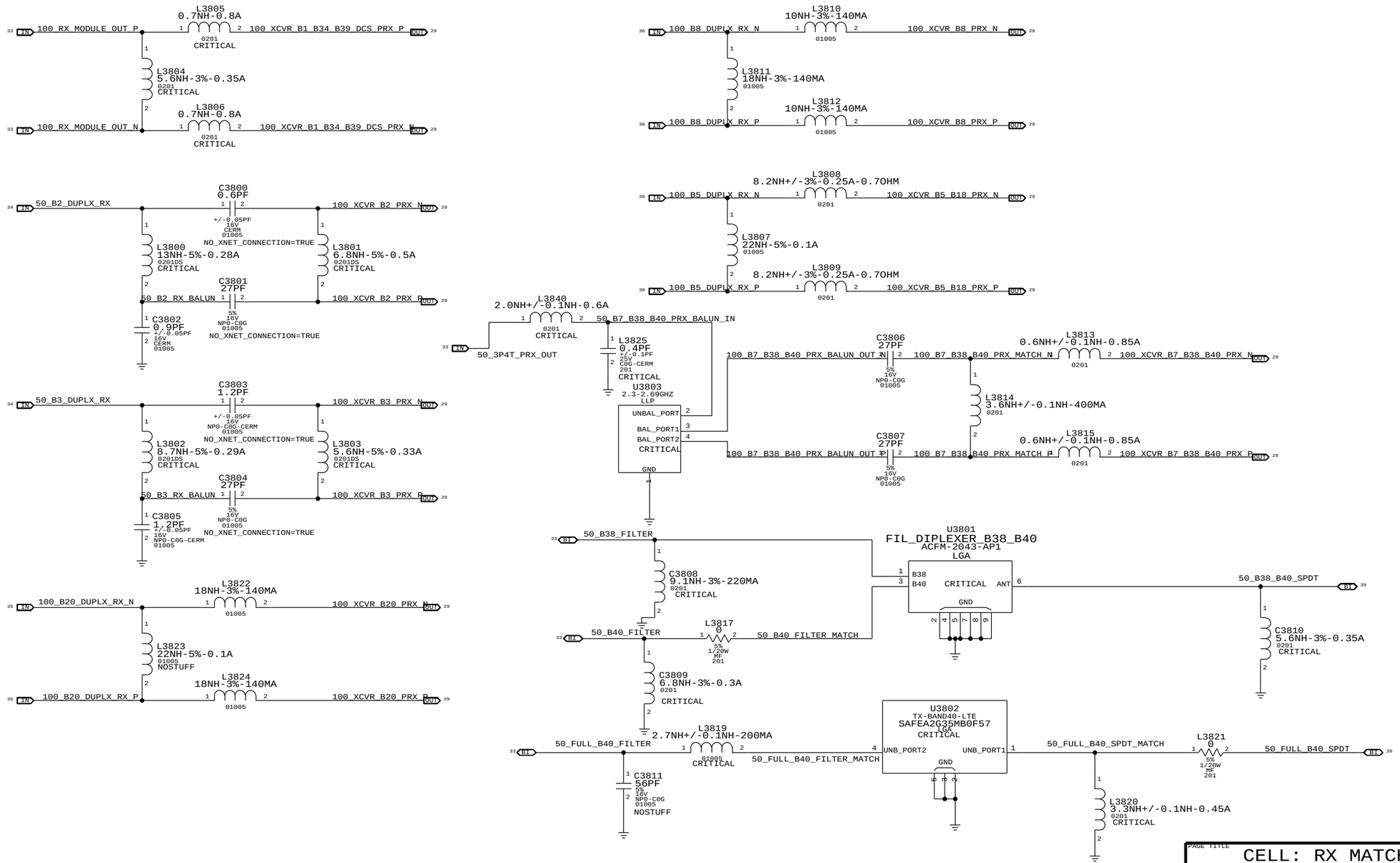
RX MATCHING



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CELL: RX MATCHING	
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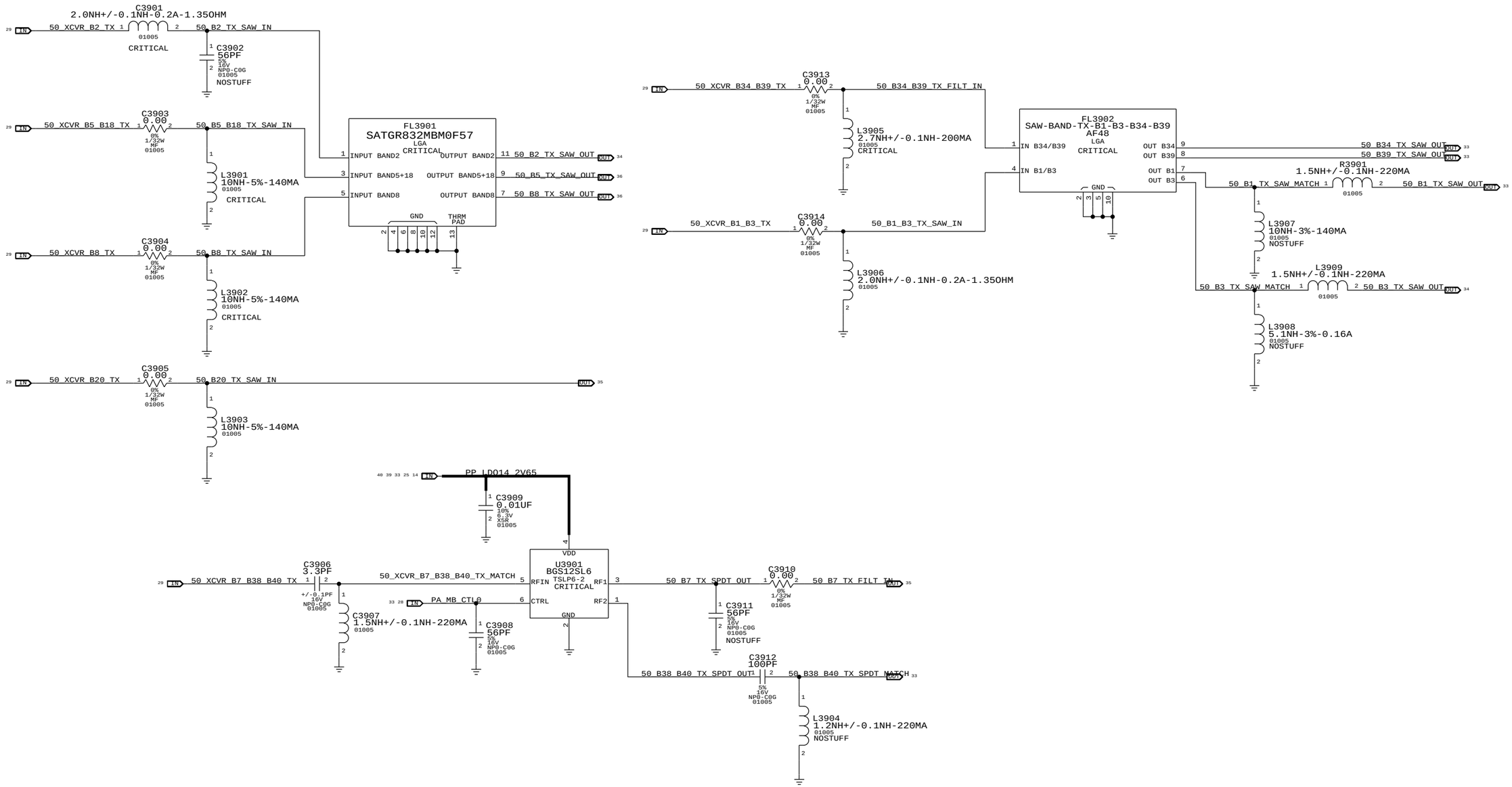
TX INTERSTAGE FILTERS



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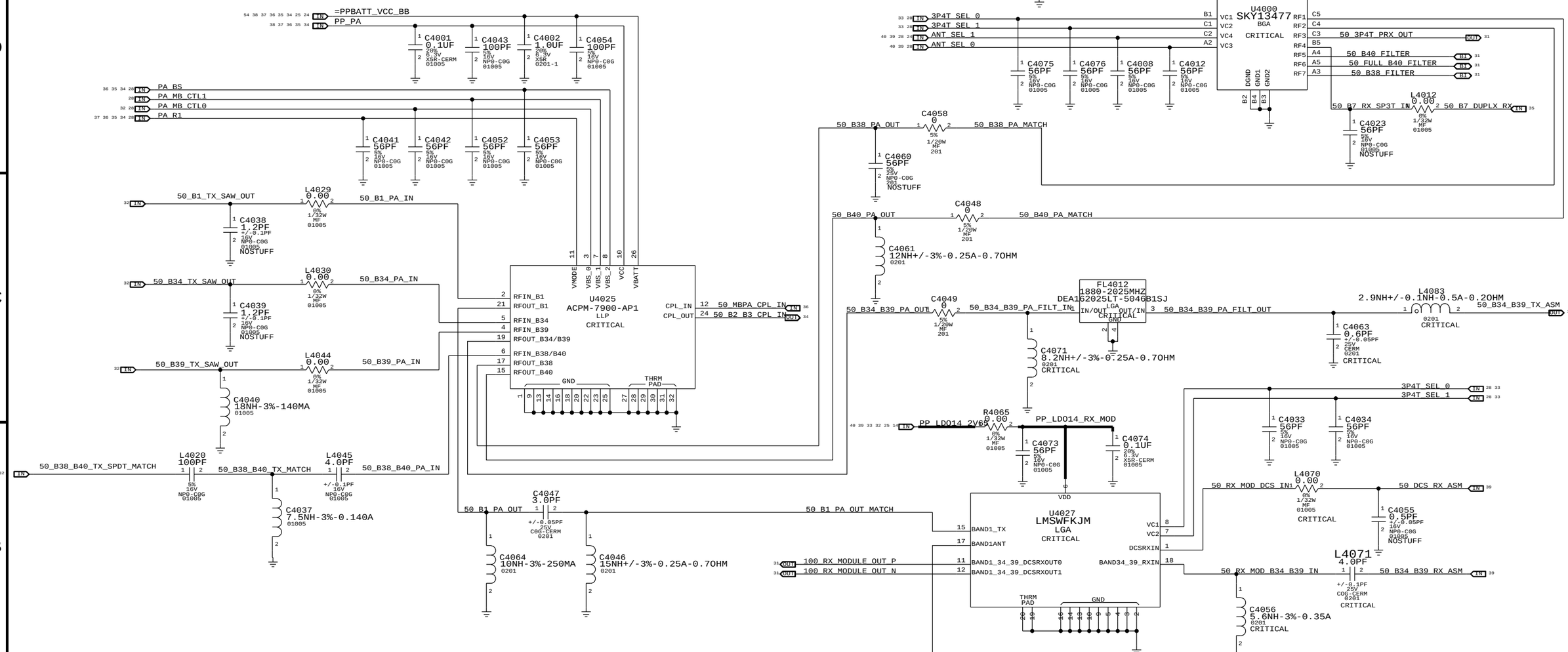
BAND 1/34/39/38/40 TX



BAND	PA POWER MODE	PA_BS	PA_CTL1	PA_CTL0	PA_R1
OFF	X	X	0	0	0
B1	HPM	X	1	0	0
B1	LPM	X	1	0	1
B34	HPM	1	0	1	0
B34	LPM	1	0	1	1
B39	HPM	0	0	1	0
B39	LPM	0	0	1	1
B38	HPM	1	1	1	0
B38	LPM	1	1	1	1
B40	HPM	0	1	1	0
B40	LPM	0	1	1	1

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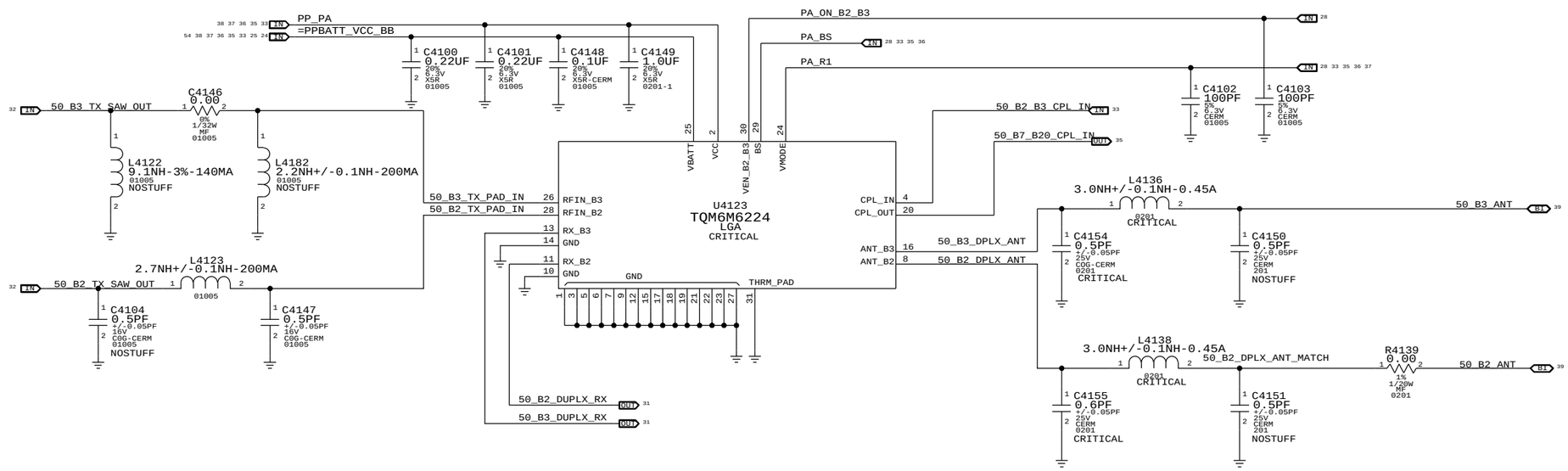
BAND 2/3 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B2_B3	PA_R1
OFF	X	X	0	X
B3	HPM	0	1	0
B3	LPM	0	1	1
B2	HPM	1	1	0
B2	LPM	1	1	1

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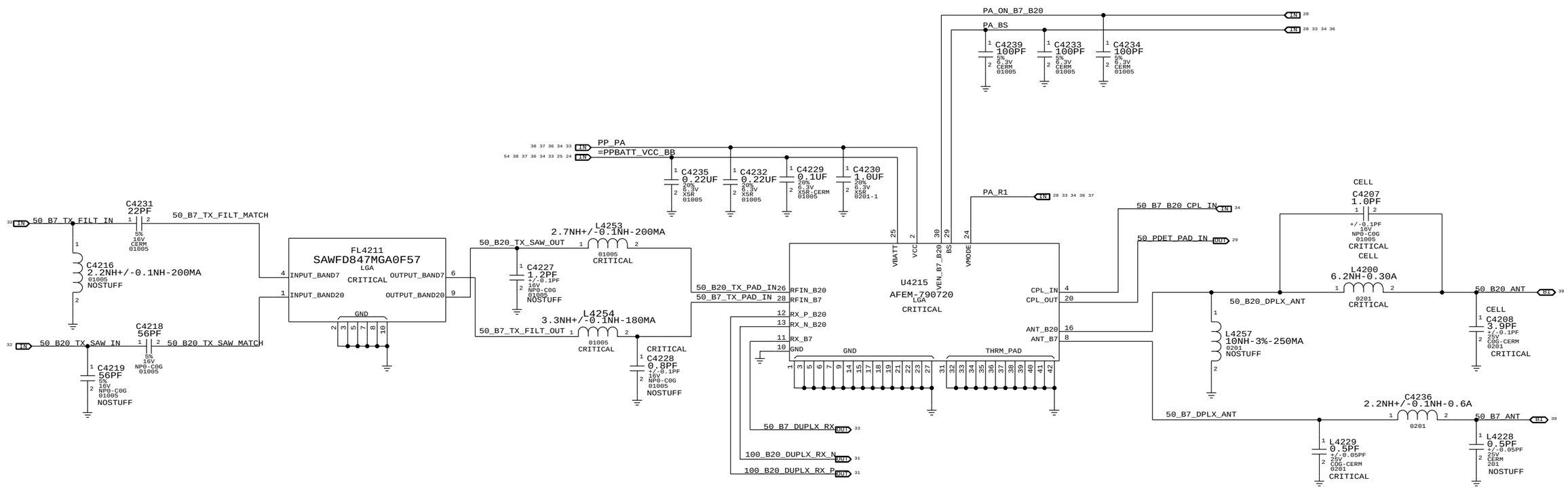
BAND 20/7 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B20_B7	PA_R1
OFF	X	X	0	X
B20	HPM	0	1	0
B20	LPM	0	1	1
B7	HPM	1	1	0
B7	LPM	1	1	1

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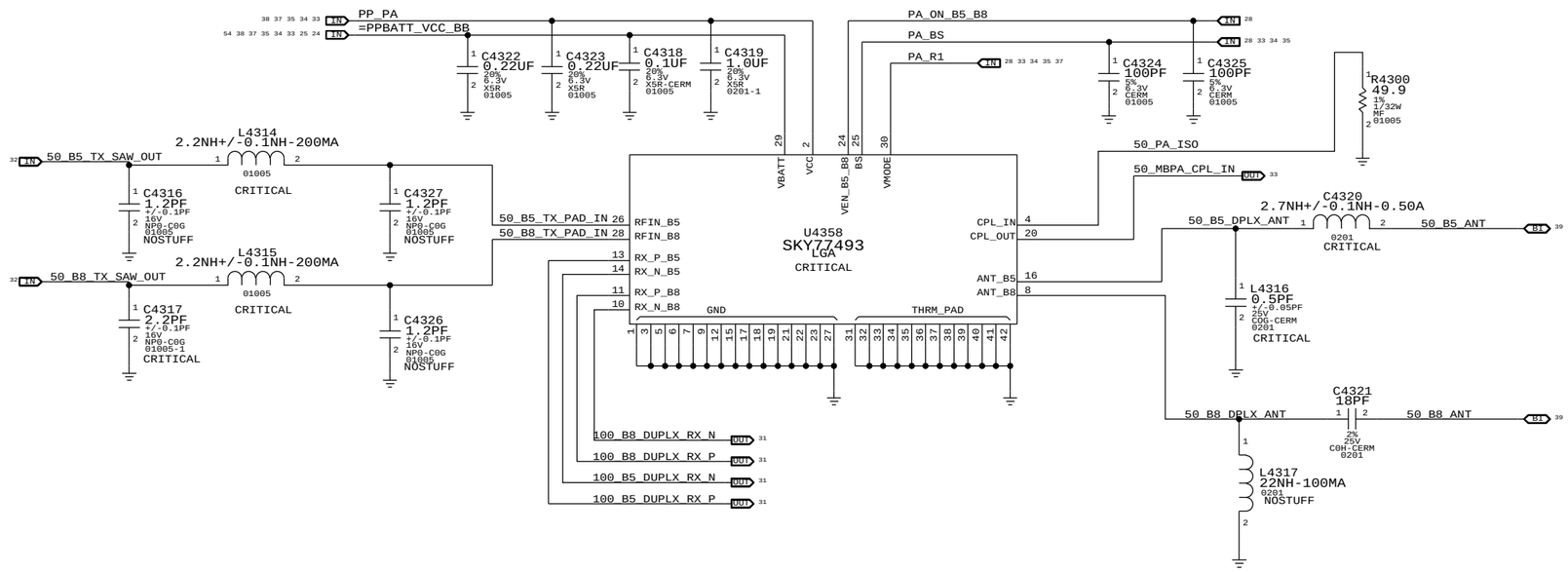
BAND 5/8 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B5_B8	PA_R1
OFF	X	X	0	X
B5	HPM	0	1	0
B5	LPM	0	1	1
B8	HPM	1	1	0
B8	LPM	1	1	1

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2G PA

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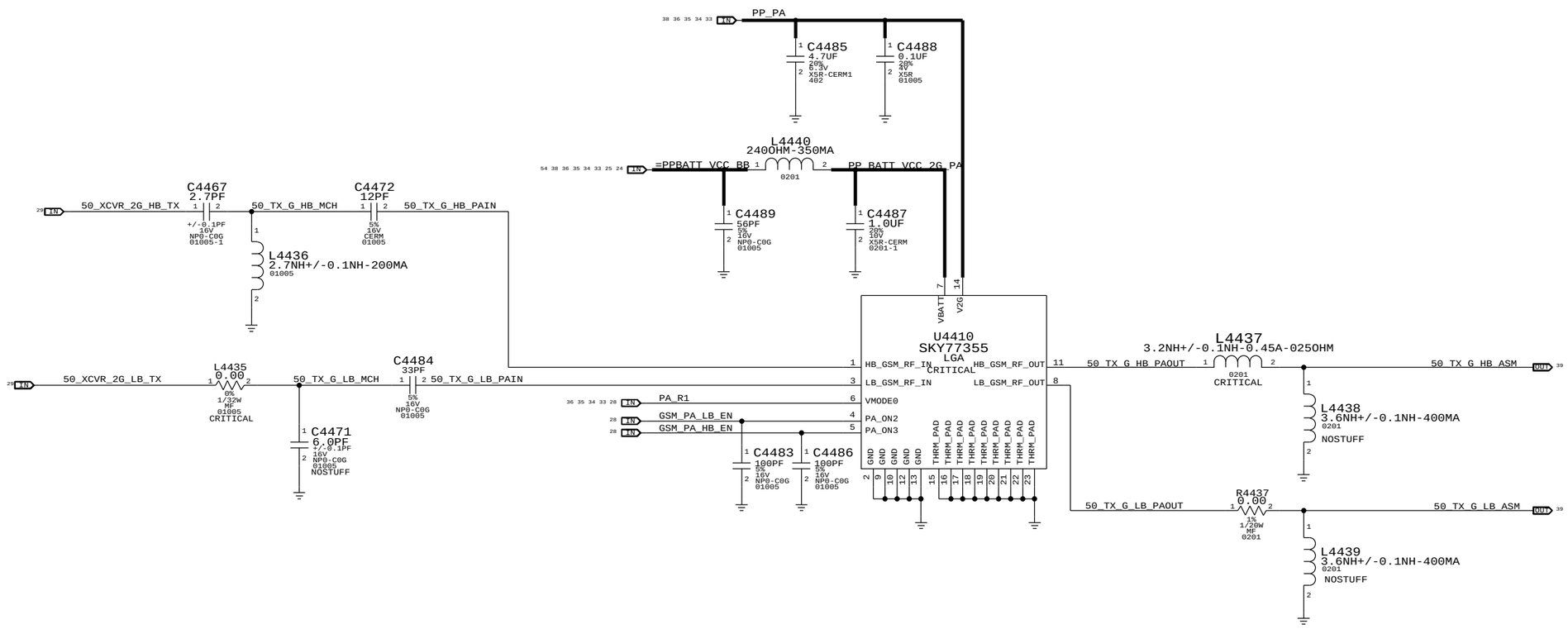
2G PA GAIN MODES

BAND	MODE	GAIN MODE	PA_R1	PCL RANGE
LOW BAND	GSM	ULTRA LOW	HIGH	16 TO 19
LOW BAND	GSM	LOW	HIGH	14 TO 15
LOW BAND	GSM	MEDIUM	LOW	7 TO 13
LOW BAND	GSM	HIGH	LOW	5 TO 6
HIGH BAND	GSM	ULTRA LOW	HIGH	10 TO 15
HIGH BAND	GSM	LOW	HIGH	7 TO 9
HIGH BAND	GSM	HIGH	LOW	0 TO 6
LOW BAND	EDGE	LOW	HIGH	15 TO 19
LOW BAND	EDGE	MEDIUM	LOW	10 TO 14
LOW BAND	EDGE	HIGH	LOW	8 TO 9
HIGH BAND	EDGE	LOW	HIGH	9 TO 15
HIGH BAND	EDGE	HIGH	LOW	2 TO 8



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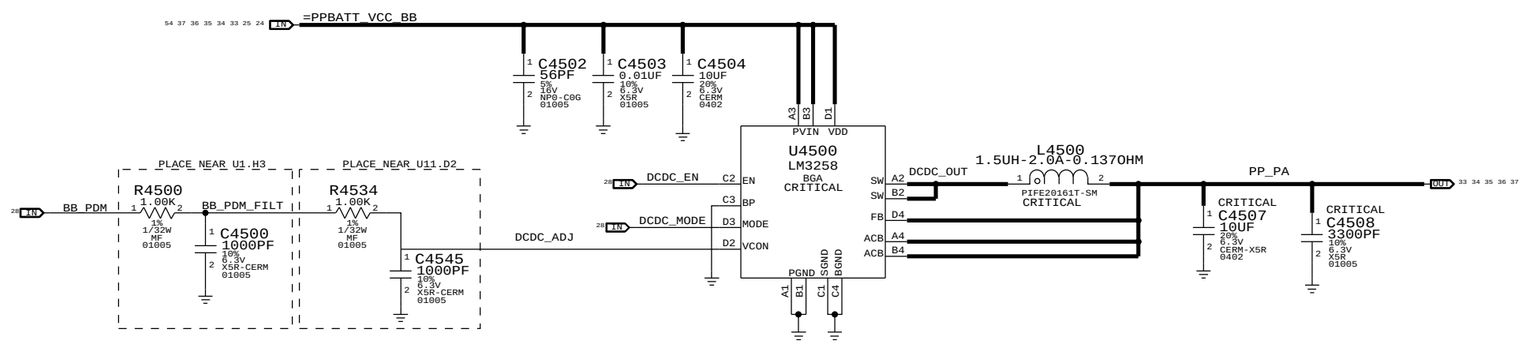
PA DC/DC CONVERTER



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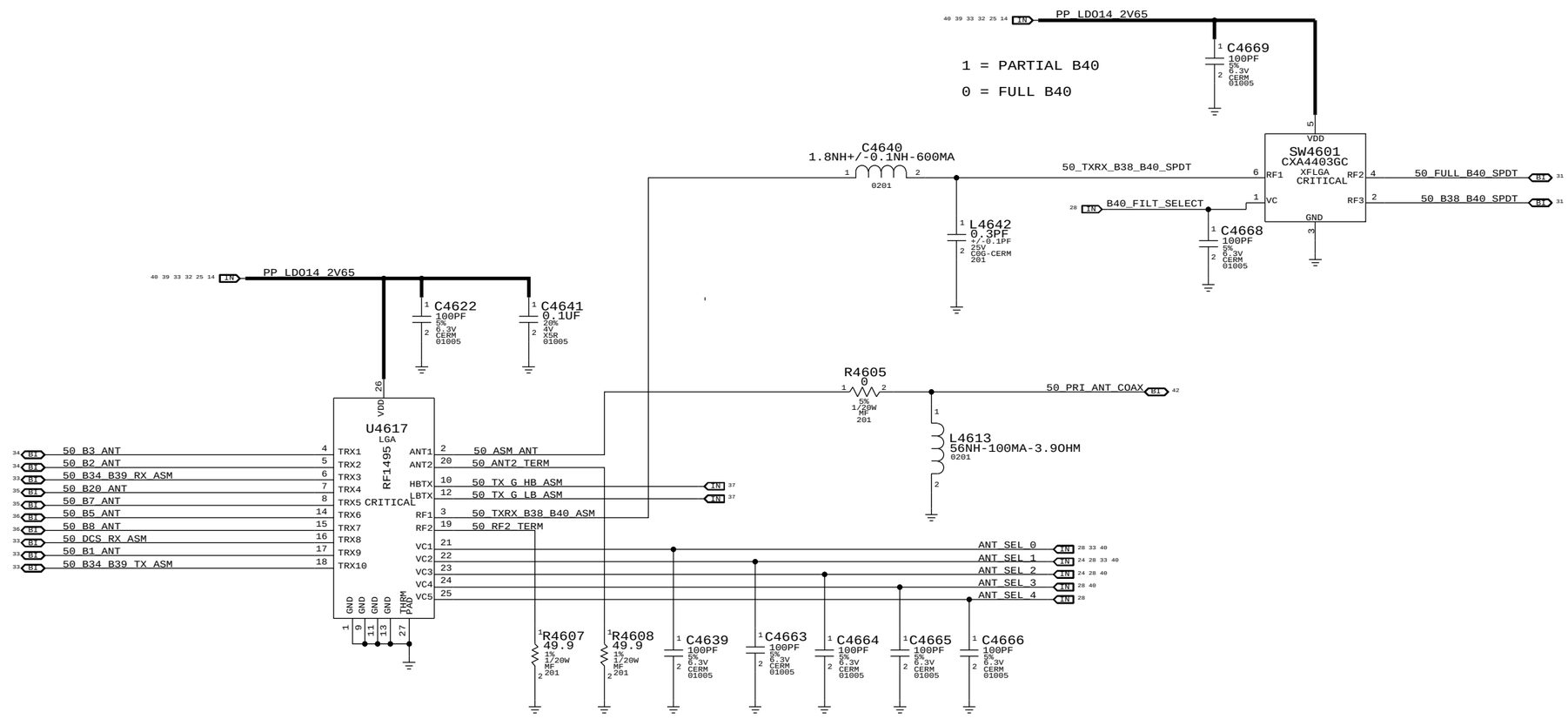
PRIMARY ASM



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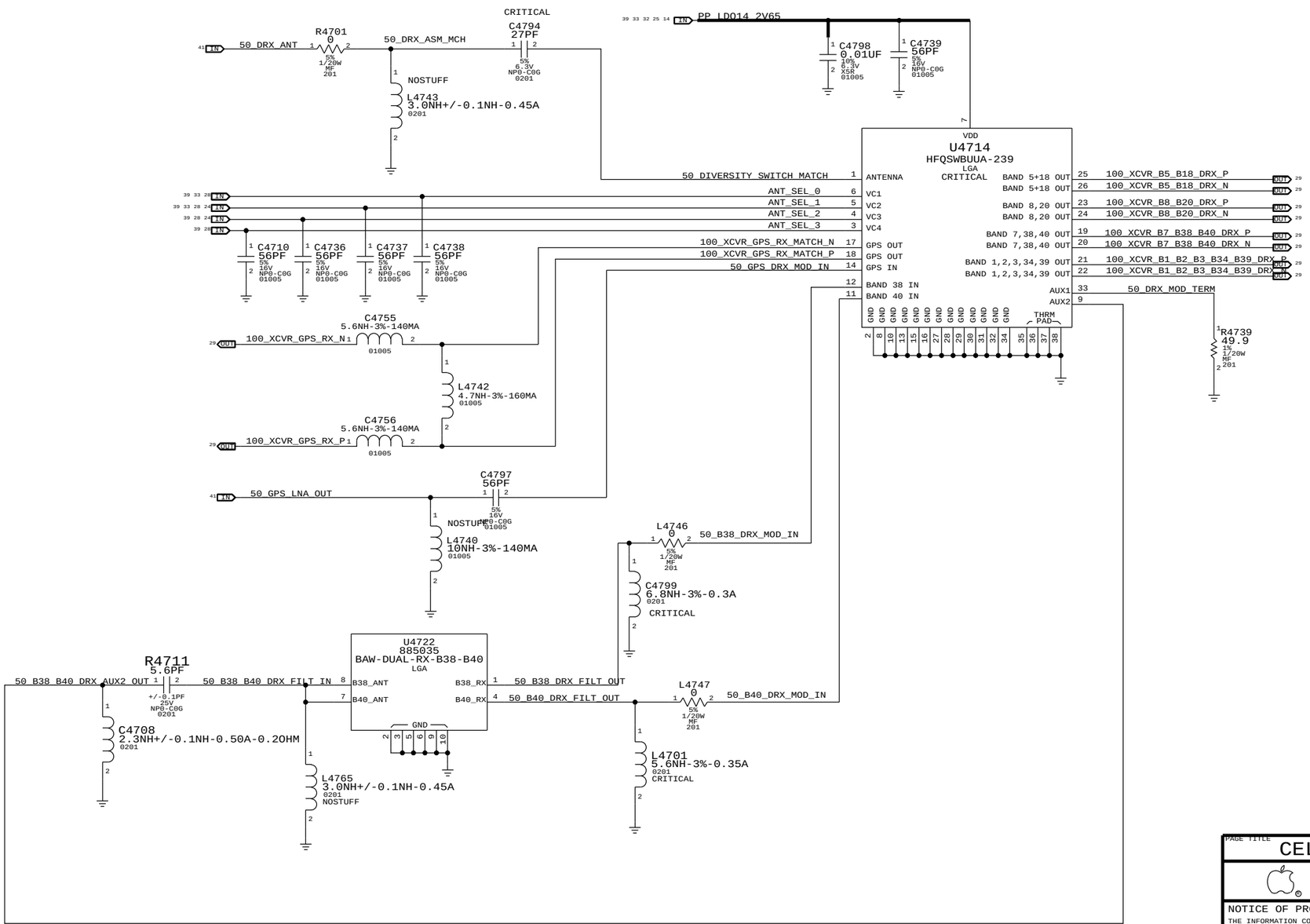
RX DIVERSITY



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PAGE TITLE
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GPS

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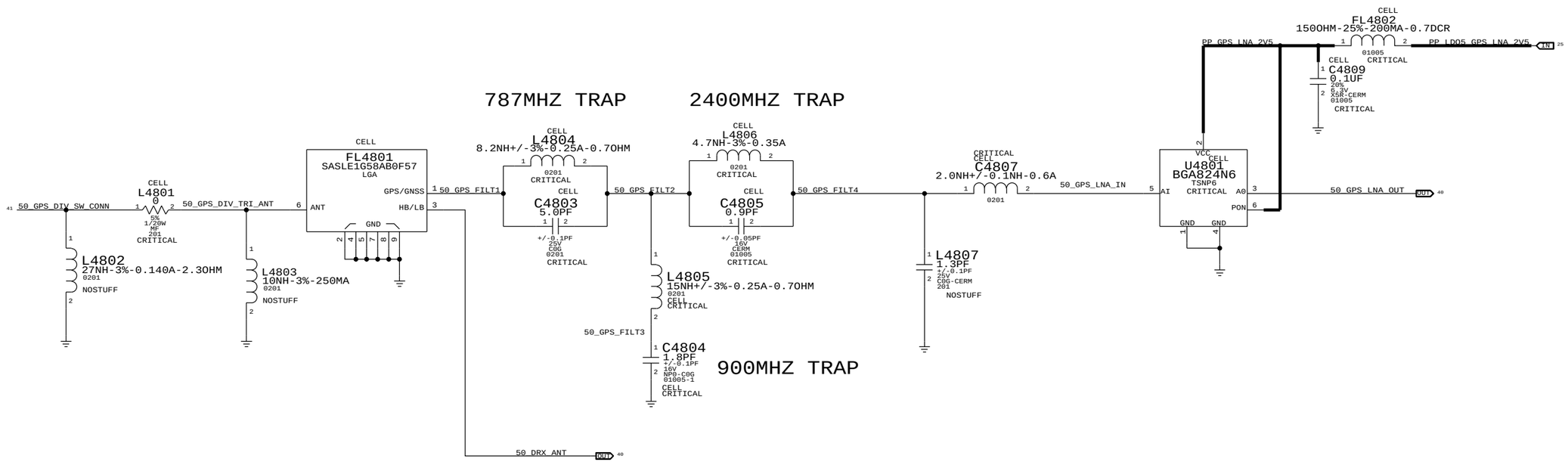

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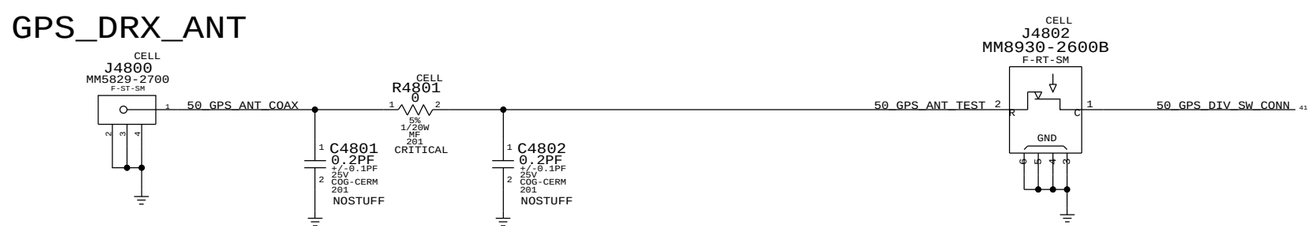

TOP MOUNT

TOP MOUNT

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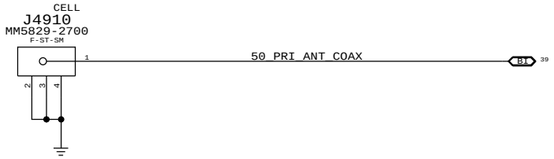
ANTENNA FEEDS

PRI_ANT COAX



SYNC_MASTER=RADIO_MLB_87 SYNC_DATE=10/29/2013

PAGE TITLE
CELL: ANTENNA FEEDS

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DRAWING NUMBER 051-0886 SIZE D

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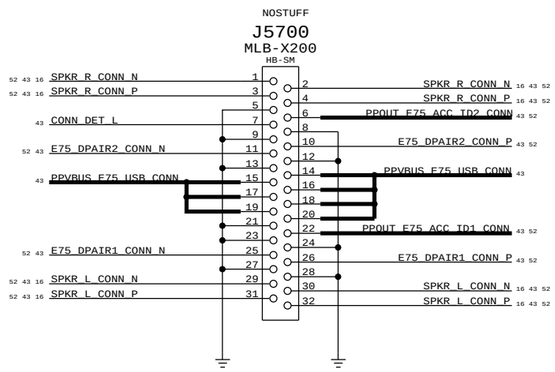
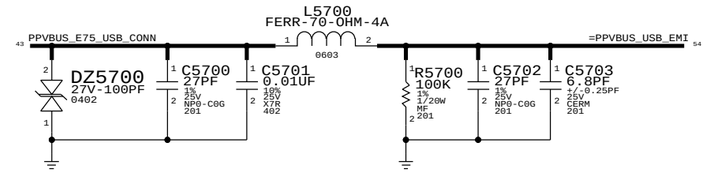
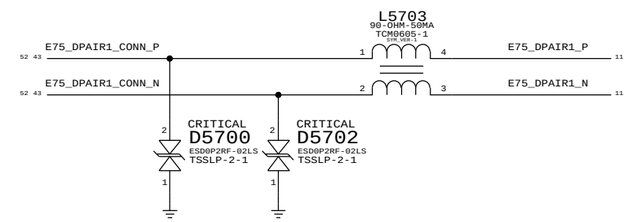
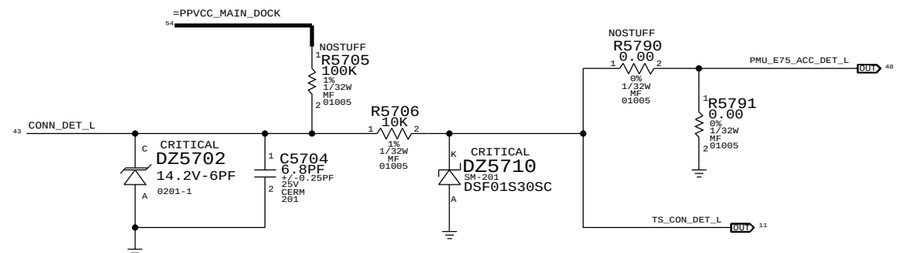
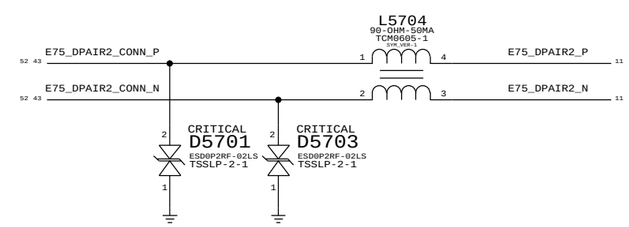


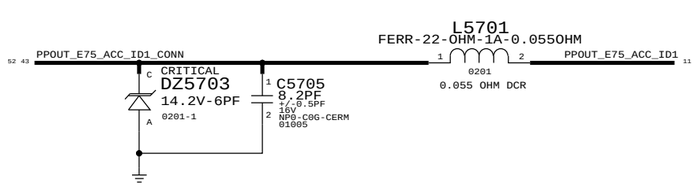
NOTE: SPKR_L_CONN_N AND SPKR_L_CONN_P WERE SWAPPED ON 5/22/12 PER RADAR #11526818

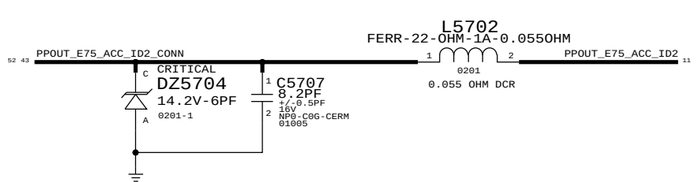












SYNC_MASTER=N/A SYNC_DATE=04/18/2011

PAGE TITLE
IO: FILTERS & HOTBAR CONN

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WIFI/BT: MODULE

MODULE ISOLATION

XW5890 SHORT-10L-0.25MM-SM: PMU_GPIO_WLAN_REG_ON (52 48 IN) → PMU_GPIO_WLAN_REG_ON_R (44)
XW5891 SHORT-10L-0.25MM-SM: PMU_GPIO_BT_REG_ON (52 48 IN) → PMU_GPIO_BT_REG_ON_R (44)
XW5892 SHORT-10L-0.25MM-SM: PMU_GPIO_CLK_32K_WLAN (52 48 IN) → PMU_GPIO_CLK_32K_WLAN_R (44)
XW5893 SHORT-10L-0.25MM-SM: UART_WLAN2BB_LTE_COEX (28 24 OUT) → UART_WLAN2BB_LTE_COEX_R (44)
XW5894 SHORT-10L-0.25MM-SM: UART_BB2WLAN_LTE_COEX (28 24 IN) → UART_BB2WLAN_LTE_COEX_R (44)
XW5895 SHORT-10L-0.25MM-SM: UART2_WLAN2SOC_TX (53 5 OUT) → UART2_WLAN2SOC_TX_R (44)
XW5896 SHORT-10L-0.25MM-SM: UART2_SOC2WLAN_TX (53 5 IN) → UART2_SOC2WLAN_TX_R (44)
XW5897 SHORT-10L-0.25MM-SM: HSIC1_SOC2WLAN_HOST_RDY (53 5 IN) → HSIC1_SOC2WLAN_HOST_RDY_R (44)

=PPVCC_MAIN_WLAN (54)
C5880 10UF 20% 6.3V CERM-X5R 0402-2
C5881 10UF 20% 6.3V CERM-X5R 0402-2
C5882 10UF 20% 6.3V CERM-X5R 0402-2

=PP3V3_S2R_WIFI_PA (54)
C5800 4.7UF 20% 6.3V X5R-CERM1 402
C5801 4.7UF 20% 6.3V X5R-CERM1 402

=PP1V8_S2R_VDDIO_WLAN_BT (44 54)
NOSTUFF R5805 10K 5% 1/32W MF 01005
R5800 10K 5% 1/32W MF 01005
JTAG_WLAN_SEL (52)

CRITICAL U5800 WIFI-BT-DOPPELBOCK LGA

Pin	Signal	Net
16	VBAT	
17	VBAT	
70	RF_VCC_FEM	
71	RF_VCC_FEM	
33	CLK_32K	PMU_GPIO_CLK_32K_WLAN_R (44)
4	WL_REG_ON	PMU_GPIO_WLAN_REG_ON_R (44)
3	BT_REG_ON	PMU_GPIO_BT_REG_ON_R (44)
23	JTAG_SEL	
13	HSIC_DATA	HSIC1_WLAN_DATA (53 4 BI)
14	HSIC_STROBE	HSIC1_WLAN_STB (53 4 BI)
7	SDIO_CLK	NC
6	SDIO_CMD	NC
8	SDIO_DATA0	NC
9	SDIO_DATA1	NC
10	SDIO_DATA2	NC
11	SDIO_DATA3	NC
77	RF_SW_CTRL11	NC
47	I2SWS	NC
36	I2SDO	NC
48	I2SDI	NC
49	I2SCLK	NC
67	RF_A_0	
79	RF_A_1	
62	RF_G_0	
74	RF_G_1	
51	UART_WLAN2BB_LTE_COEX_R	BT_GPIO5/LTE_COEX_UART_TX
50	UART_BB2WLAN_LTE_COEX_R	BT_GPIO4/LTE_COEX_UART_RX
55	PMU_GPIO_BT_HOST_WAKE	BT_GPIO1/HOSTWAKE (OUT 48 52)
56	GPIO_BT_WAKE	BT_GPIO0/BTWAKE (IN 5 53)
37	UART1_SOC2BT_TX	BT_UART_RXD (IN 5 53)
38	UART1_BT2SOC_TX	BT_UART_TXD (OUT 5 53)
36	UART1_BT2SOC_RTS_L	BT_UART_RTS* (OUT 5)
39	UART1_SOC2BT_RTS_L	BT_UART_CTS* (IN 5)
41	I2S4_SOC2BT_BCLK	BT_PCM_CLK (IN 10)
42	I2S4_SOC2BT_LRCK	BT_PCM_SYNC (IN 10)
43	I2S4_BT2SOC_DATA	BT_PCM_OUT (OUT 10)
44	I2S4_SOC2BT_DATA	BT_PCM_IN (IN 10)
22	PMU_GPIO_WLAN_HOST_WAKE	GPIO0/WL_HOST_WAKE (OUT 48 53)
20	HSIC1_SOC2WLAN_HOST_RDY_R	GPIO1/HOST_READY (44)
27	TP_JTAG_WLAN_TCK	GPIO2/WL_TCK (52)
28	JTAG_WLAN_TMS_TX_BLANK	GPIO3/WL_TMS
26	JTAG_WLAN_TDI_OSCAR_A	GPIO4/WL_TDI
24	JTAG_WLAN_TDO_OSCAR_B	GPIO5/WL_TDO
25	TP_JTAG_WLAN_TRST_L	GPIO12/WL_TRST* (52)
19	NC	GPIO9/AGG_CHANNEL
1	HSIC1_WLAN2SOC_DEVICE_RDY	GPIO10/HSIC_DEVICE_READY (OUT 5 53)
2	HSIC1_WLAN2SOC_REMOTE_WAKE	GPIO11/HSIC_RESUME (OUT 5 53)
52	UART2_WLAN2SOC_TX_R	GPIO15/WLAN_UART_TX (44)
53	UART2_SOC2WLAN_TX_R	GPIO14/WLAN_UART_RX (44)
30	NC	GPIO6
29	WLAN_GPIO7	GPIO7
31	NC	GPIO8
35	=PP1V8_S2R_VDDIO_WLAN_BT (44 54)	VIO
57	NC	DUMMY

GND_SIGNAL: 5, 12, 15, 18, 21, 32, 34, 40, 45, 54, 58, 59, 60, 61, 63, 64, 65, 66, 68, 69, 72, 73, 75, 76, 78, 80, 81, 82, 83, 84, 85, 86, 87, 88

R5804 0.00 0% 1/32W MF 01005: WLAN_TX_BLANK (IN 28 52)
R5801 0.00 0% 1/32W MF 01005: OSCAR2RADIO_CONTEXT_A (IN 19 28 52)
R5802 0.00 0% 1/32W MF 01005: OSCAR2RADIO_CONTEXT_B (IN 19 28 52)
=PP1V8_S2R_VDDIO_WLAN_BT (44 54)
R5803 10K 5% 1/32W MF 01005

CRITICAL U5810 2.4-5.0GHZ SM: LOW(2.4GHZ) (3), HIGH(5.0GHZ) (1), ANT(COMMON) (5), GND (6 4 2)
RF_G_0_DIPLEXER → CRITICAL R5830 0.00 1% 1/20W MF 0201 → RF_G_0_BAW_ANT

CRITICAL U5811 BAW-2436MHZ 885061 LGA: OUT (4), IN (1), GND (5 3 2)
RF_G_0_BAW_MOD → CRITICAL C5811 2.0NH+/-0.1NH-0.6A 0201 → RF_G_0_MATCH_MOD
CRITICAL C5810 0.5PF +/-0.05PF 25V CERM 201

CRITICAL L5811 10NH-3%-250MA 0201
CRITICAL L5810 8.2NH+/-3%-0.25A-0.7OHM 0201

CRITICAL J5810 MM4829-2702 F-ST-SM
RF_0_ANT → CRITICAL R5810 0.00 1% 1/20W MF 0201 → RF_0_ANT_MATCH_T
NOSTUFF C5817 0.2PF +/-0.1PF 25V COG-CERM 201
NOSTUFF C5816 0.2PF +/-0.1PF 25V COG-CERM 201

RF_A_0_DIPLEXER
CRITICAL C5814 1.0NH+/-0.1NH-0.75A 0201
NOSTUFF C5815 0.2PF +/-0.1PF 25V COG-CERM 201
RF_A_0_MATCH
CRITICAL C5813 0.2PF +/-0.05PF 25V COG-CERM 0201

CRITICAL J5820 MM4829-2702 F-ST-SM
RF_1_ANT → CRITICAL R5820 0.00 1% 1/20W MF 0201 → RF_1_ANT_MATCH_T
NOSTUFF C5827 0.2PF +/-0.1PF 25V COG-CERM 201
NOSTUFF C5826 0.2PF +/-0.1PF 25V COG-CERM 201

CRITICAL U5820 DPX205850DT-9038A1SJ SM: COM (5), HI (1), LO (3), GND (6 4 2)

RF_G_1_DIPLEXER
CRITICAL C5821 1.1NH+/-0.1NH 0201
NOSTUFF C5822 0.2PF +/-0.1PF 25V COG-CERM 201
RF_G_1_MATCH_MOD
CRITICAL C5820 0.5PF +/-0.05PF 25V CERM 201

RF_A_1_DIPLEXER
CRITICAL C5824 1.0NH+/-0.1NH-0.75A 0201
NOSTUFF C5825 0.2PF +/-0.1PF 25V COG-CERM 201
RF_A_1_MATCH
CRITICAL C5823 0.2PF +/-0.05PF 25V COG-CERM 0201

SYNC_MASTER=WIFI_DEV SYNC_DATE=05/20/2013

PAGE TITLE: WIFI/BT: MODULE

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DRAWING NUMBER: 051-0886 SIZE: D
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BRANCH:
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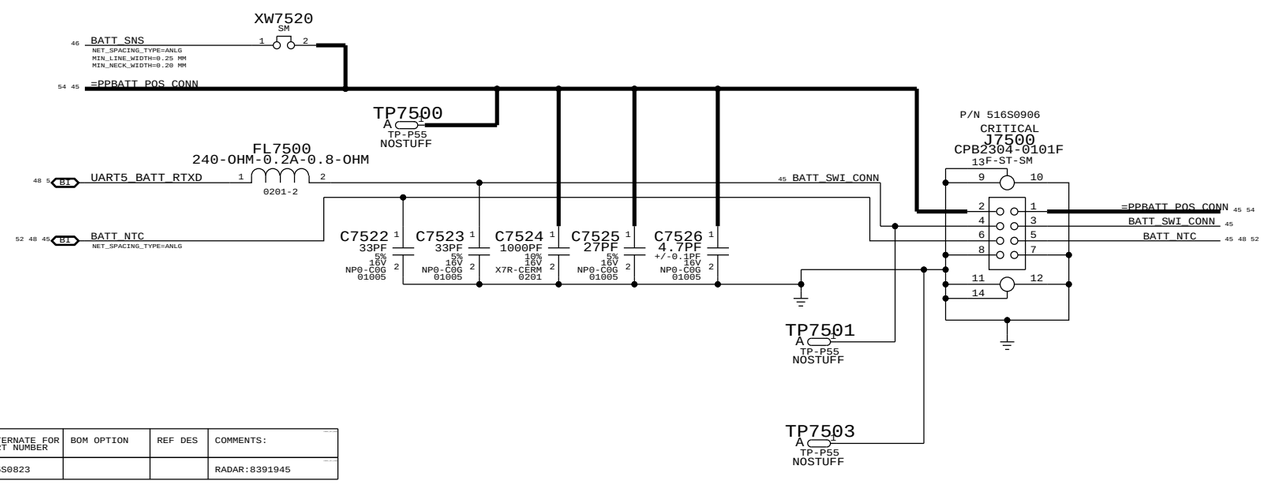

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0823			RADAR:8391945

FL7500,L1702,L1800,L1920,L2602,L2700,L2701,L2702,L2800,L2960,L2961,L2962,L2963,L38014_RF

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
POWER: BATTERY CONNECTOR

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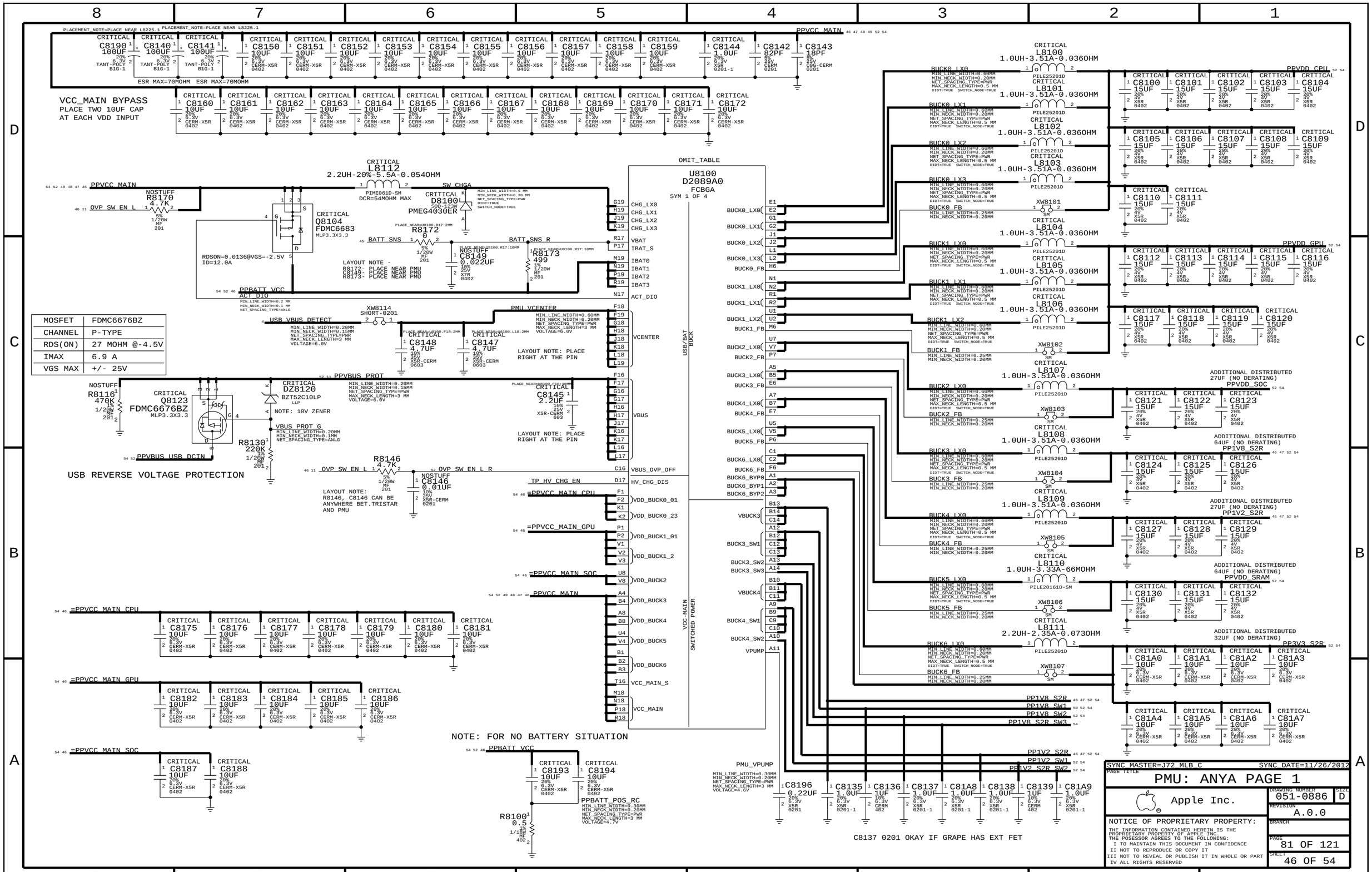
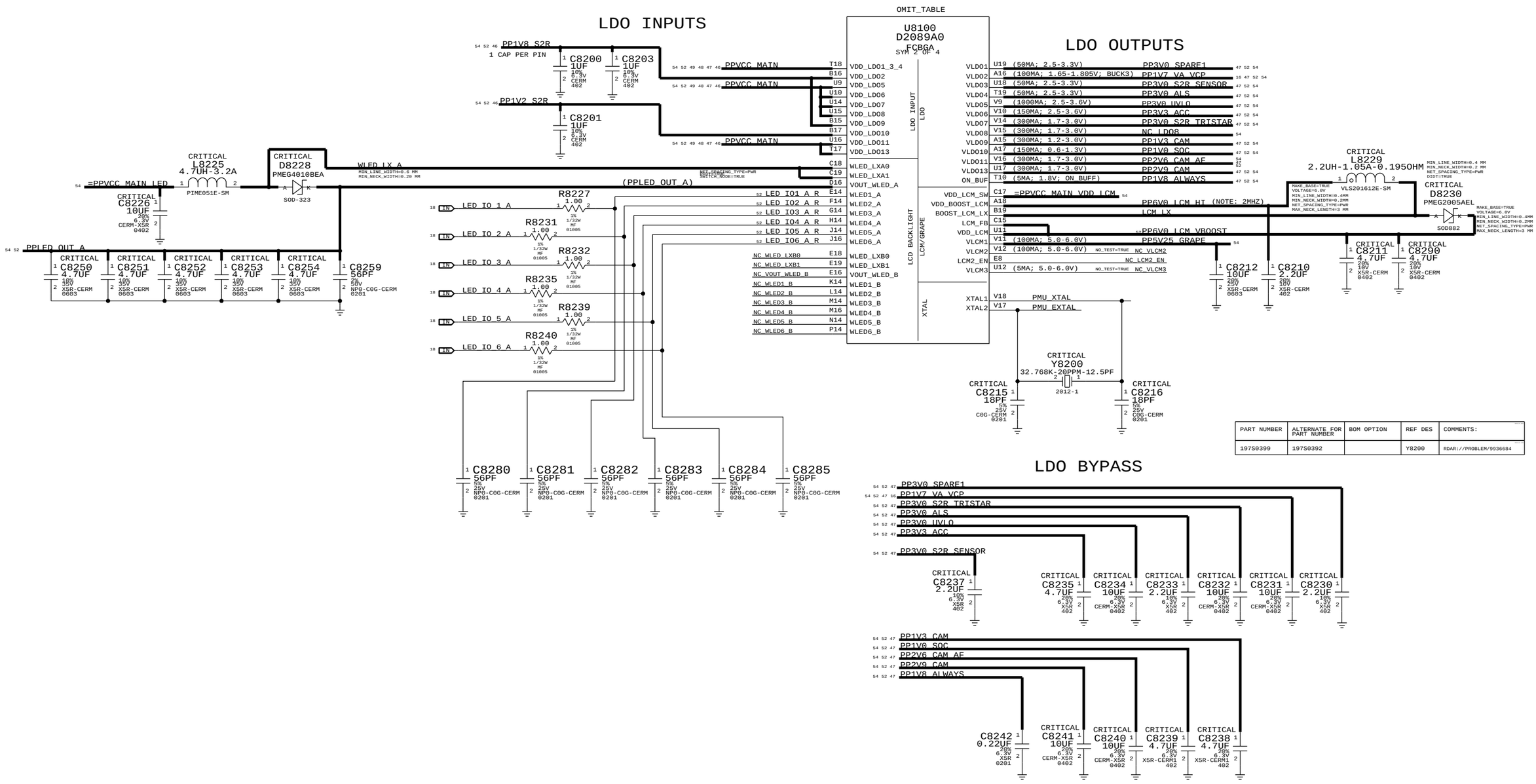


MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392		Y8200	RDAR://PROBLEM/9936684

SYNC MASTER=J85 MLB C SYNC DATE=12/03/2012

PAGE TITLE
PMU: ANYA PAGE 2

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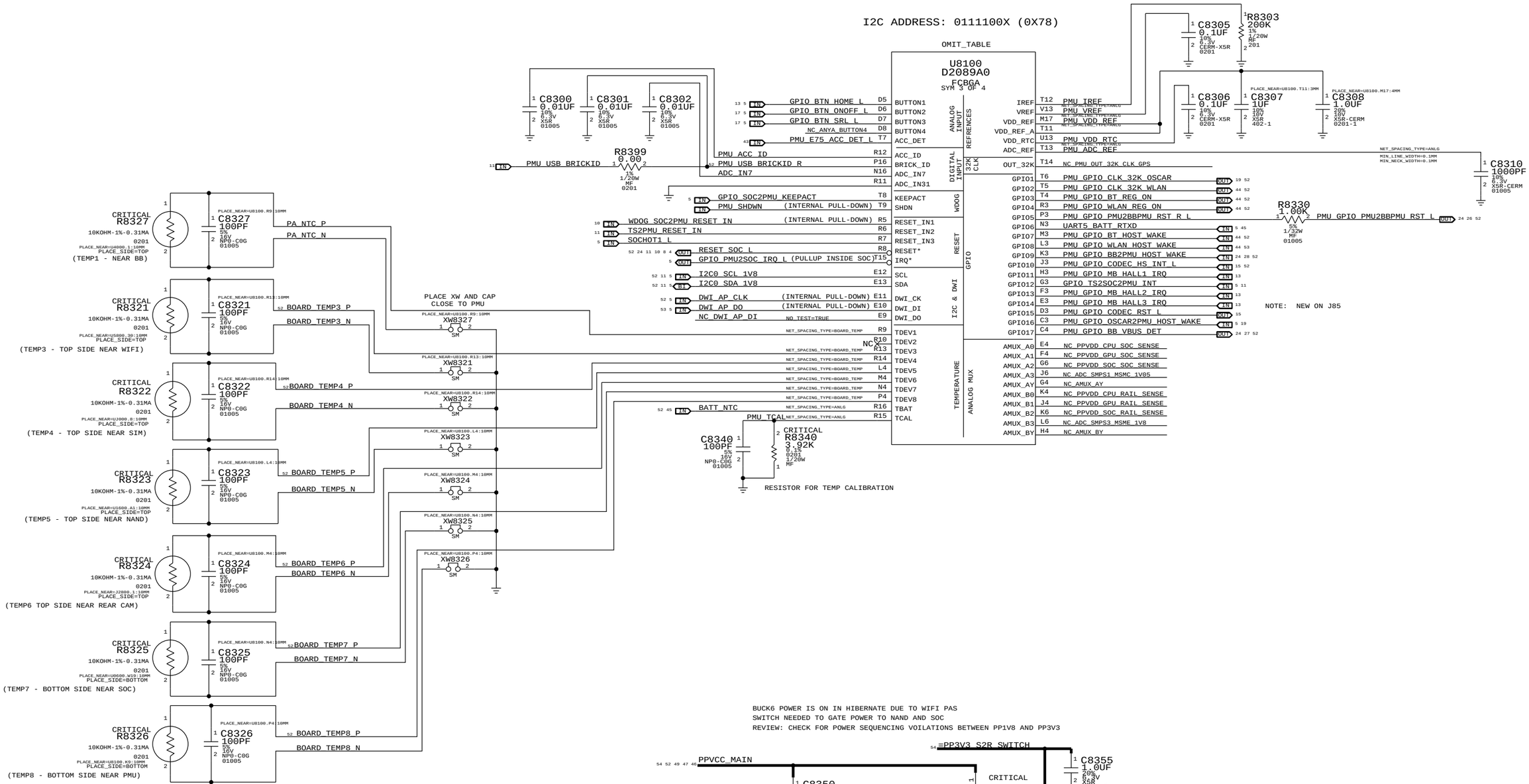
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0739	138S0706		C8308	

REVIEW: VERIFY NC ON TDEV2 IS OK

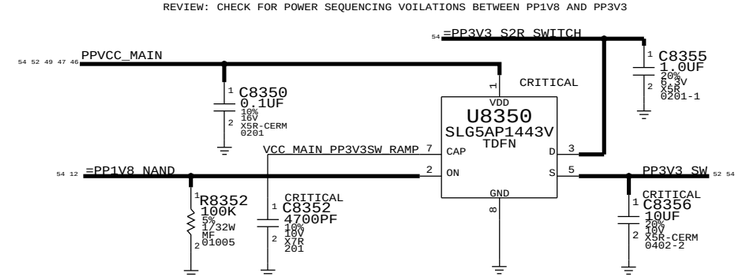
I2C ADDRESS: 0111100X (0X78)

OMIT_TABLE

U8100
D2089A0
FCBGA
SYM 3 OF 4



BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS
SWITCH NEEDED TO GATE POWER TO NAND AND SOC
REVIEW: CHECK FOR POWER SEQUENCING VOILATIONS BETWEEN PP1V8 AND PP3V3



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	R8321,R8322	R8323,R8324,R8325,R8326	RDAR://PROBLEM/8380367
118S0764	118S0717		R8340	RDAR://PROBLEM/8380367

SYNC_MASTER=J72_MLB_C SYNC_DATE=11/26/2012

PAGE TITLE
PMU: ANYA PAGE 3

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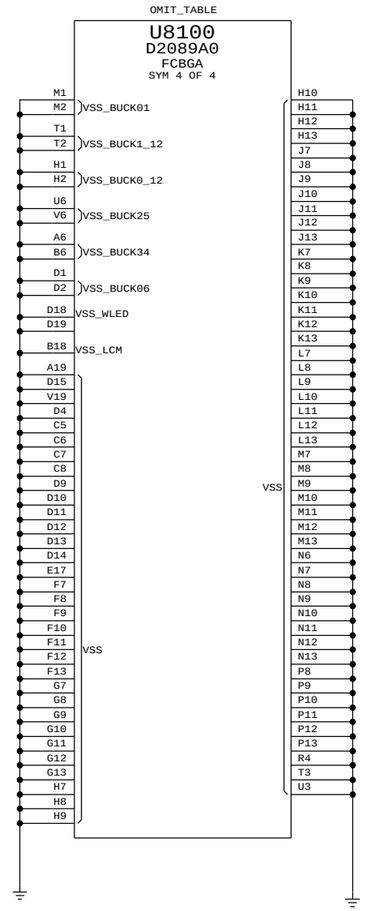
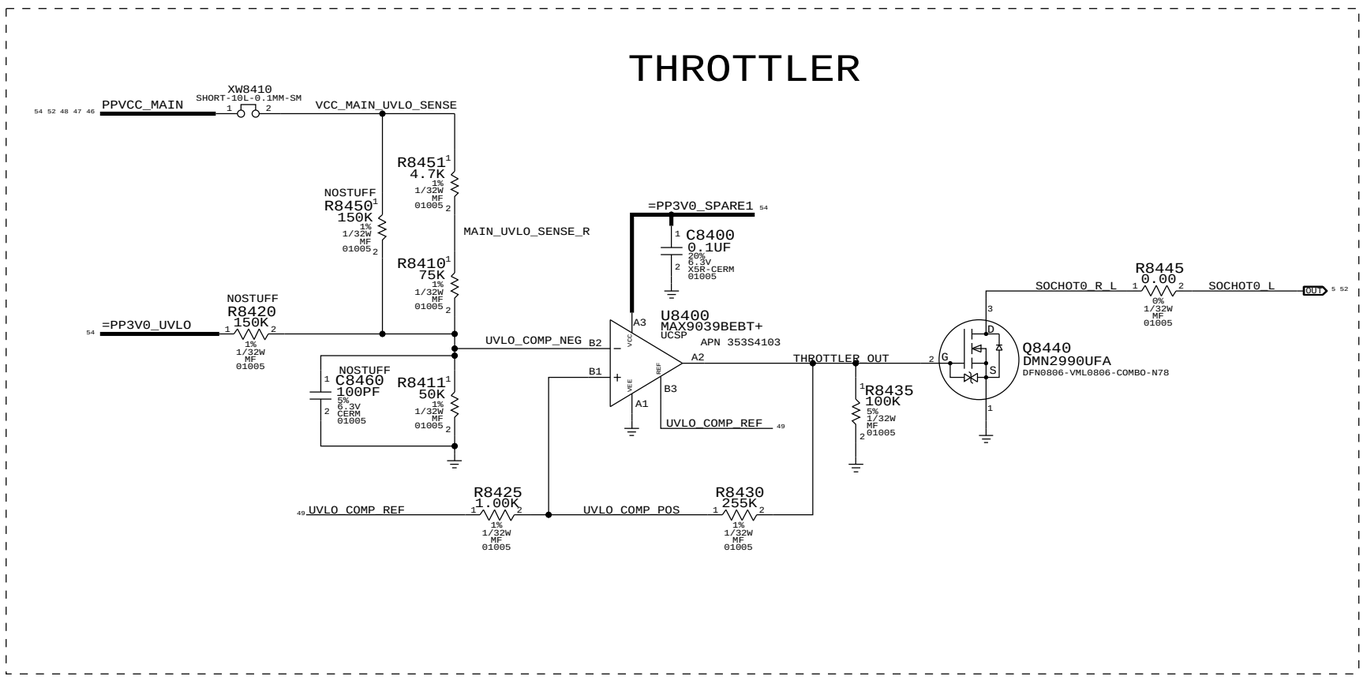


ADD A VIA PER PIN FOR ALL VSS_* AND VSSA_* PINS



SYNC_MASTER=J72_MLB_C SYNC_DATE=11/26/2012

PAGE TITLE
PMU: ANYA PAGE 4

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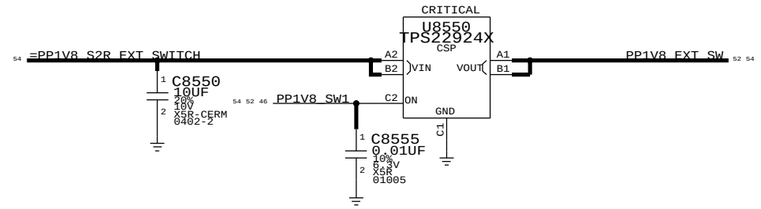
SWITCH TO GATE POWER TO SOC AND NAND. NEEDED FOR J72 ROUTING.



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SYNC_MASTER=J85_MLB_C SYNC_DATE=11/26/2012

PAGE TITLE
POWER: PP1V8_SW

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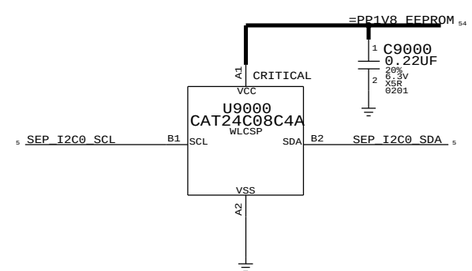
DEBUG

SEP EEPROM

UNPROGRAMMED P/N: 335S0894



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SYNC MASTER=J72_MLB_C SYNC DATE=11/26/2012

PAGE TITLE
SEP: EEPROM & SOC DEBUG

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TP9300	GPIO_CODEC_IRQ_L	5 15
TP9304	PMU_GPIO_CODEC_HS_INT_L	15 48
TP9303	BATT_NTC	45 48
TP9305	PPLED_OUT_A	47 54
TP9396	PP3V0_UVLO	47 54
TP9397	PP3V0_SPARE1	47 54
TP9398	SOCHOT0_L	5 49
TP9312	BOARD_TEMP3_P	48
TP9313	BOARD_TEMP4_P	48
TP9314	BOARD_TEMP5_P	48
TP9315	BOARD_TEMP6_P	48
TP9316	BOARD_TEMP7_P	48
TP9317	BOARD_TEMP8_P	48
TP9318	CLK_32K_SOC2CUMULUS	5 13
TP9320	CODEC_HP_DET_R	15
TP9321	CODEC_HP_HS3	15
TP9322	CODEC_HP_HS3_REF	15
TP9323	CODEC_HP_HS4	15
TP9324	CODEC_HP_HS4_REF	15
TP9325	CODEC_HP_LEFT	15
TP9326	CODEC_HP_RIGHT	15
TP9328	DISPLAY_SYNC_R	13
TP9329	DWI_AP_CLK	5 48
TP9330	E75_DPAIR1_CONN_N	43
TP9331	E75_DPAIR1_CONN_P	43
TP9332	E75_DPAIR2_CONN_N	43
TP9333	E75_DPAIR2_CONN_P	43
TP9334	FMI0_CE0_L	6 12
TP9335	FMI1_CE0_L	6 12
TP9336	GND	
TP9337	GND_AUDIO_CODEC	15
TP9338	GPIO_BTN_HOME_FILT_L	13
TP9339	GPIO_BTN_ONOFF_L_FILT	17
TP9340	GPIO_BTN_SRL_L_FILT	17
TP9341	GPIO_BTN_VOL_DOWN_L_FILT	17
TP9342	GPIO_BTN_VOL_UP_L_FILT	17
TP9343	GPIO_FORCE_DFU	5
TP9344	GPIO_GRAPE_IRQ_L	5 13
TP9345	GPIO_GRAPE_RST_L	5 13
TP9346	GPIO_SOC2BB_WAKE_MODEM	5 28
TP9347	GPIO_SPKAMP_KEEPALIVE	5 16
TP9348	I2C0_SCL_1V8	5 11 48
TP9349	I2C0_SDA_1V8	5 11 48
TP9350	I2C2_SCL_1V8	5 16
TP9351	I2C2_SDA_1V8	5 16
TP9352	ISP0_CAM_REAR_CLK	7 23
TP9353	ISP0_CAM_REAR_SCL	7 23
TP9354	ISP0_CAM_REAR_SDA	7 23
TP9355	ISP0_CAM_REAR_SHUTDOWN_L	7 23
TP9356	ISP1_CAM_FRONT_CLK	7 20
TP9357	ISP1_CAM_FRONT_SCL	7 20
TP9358	ISP1_CAM_FRONT_SDA	7 20
TP9359	ISP1_CAM_FRONT_SHUTDOWN_L	7 20
TP9360	JTAG_SOC_SEL	4 10
TP9361	JTAG_SOC_TCK	4 11
TP9362	JTAG_SOC_TDI	4
TP9363	JTAG_SOC_TMS	4 11
TP9364	JTAG_SOC_TRST_L	4 10
TP9365	JTAG_WLAN_SEL	44
TP9366	OSCAR2RADIO_CONTEXT_A	19 28 44
TP9367	OSCAR2RADIO_CONTEXT_B	19 28 44
TP9368	WLAN_TX_BLANK	28 44
TP9369	LAT_SW1_CTL	14 24 28
TP9370	LAT_SW2_CTL	14 28
TP9371		
TP9372	LED_IO1_A_R	47
TP9373	LED_IO2_A_R	47
TP9374	LED_IO3_A_R	47
TP9375	LED_IO4_A_R	47
TP9376	LED_IO5_A_R	47
TP9377	LED_IO6_A_R	47
TP9378	MIKEY_TS_N	11 15
TP9379	MIKEY_TS_P	11 15

TP9380	OVP_SW_EN_L_R	46
TP9382	PMU_GPIO_BT_HOST_WAKE	44 48
TP9383	PMU_GPIO_BT_REG_ON	44 48
TP9384	PMU_GPIO_CLK_32K_OSCAR	19 48
TP9385	PMU_GPIO_CLK_32K_WLAN	44 48
TP9387	PMU_USB_BRICKID_R	48
TP9388	PP1V0_SOC	47 54
TP9389	PP1V2_S2R	46 47 54
TP9390	PP1V2_S2R_SW2	46 54
TP9391	PP1V2_SW1	46 54
TP9393	PP1V7_VA_VCP	16 47 54
TP9395	PP1V8_ALWAYS	47 54
TP93A0	PP1V8_EXT_SW	50 54
TP93A1	PP1V8_GRAPE_FILT	13
TP93A2	PP1V8_GRAPE_SW	13
TP93A3	PP1V8_PLL_SOC_F	4
TP93A4	PP1V8_S2R	46 47 54
TP93A6	PP1V8_S2R_SW3_COMP	54
TP93A7	PP1V8_SW1	46 50 54
TP93A8	PP1V8_SW2	46 54
TP93A9	PP1V8_XTAL	8
TP93B0	PP2V6_CAM_AF	47 54
TP93B8	PP3V0_S2R_HALL_FILT	13
TP93C0	PP3V0_S2R_SENSOR	47 54
TP93C1	PP3V0_S2R_TRISTAR	47 54
TP93C3	PP3V3_ACC	47 54
TP93C4	PP3V3_S2R	46 54
TP93C5	PP3V3_SW	48 54
TP93C6	PP5V25_GRAPE_FILT	13
TP93C8	PP6V0_LCM_VBOOST	47
TP93C9	PPBATT_VCC	46 54
TP93D0	PPLED_BACK_REG_A	18
TP93D1	PPOUT_E75_ACC_ID1_CONN	43
TP93D2	PPOUT_E75_ACC_ID2_CONN	43
TP93D3	PPVBUS_PROT	11 46
TP93D4	PPVBUS_USB_DCIN	46 54
TP93D5	PPVCC_MAIN	46 47 48 49 54
TP93D6	PPVCC_MAIN_LCD_SW_CONN	18
TP93D7	PPVDD_CPU	46 54
TP93D8	PPVDD_GPU	46 54
TP93D9	PPVDD_SOC	46 54
TP93E0	PPVDD_SRAM	46 54

TP93G4	PP_SMPS4_RF2_2V05	25 30
TP93G9	SOC_TESTMODE	4 10
TP93H1	SPI1_GRAPE_CS_L	5 13
TP93H2	SPI1_GRAPE_MISO	5 13
TP93H3	SPI1_GRAPE_MOSI	5 13
TP93H4	SPI1_GRAPE_SCLK_R	13
TP93H5	SPKR_L_CONN_N	16 43
TP93H6	SPKR_L_CONN_P	16 43
TP93H7	SPKR_R_CONN_N	16 43
TP93H8	SPKR_R_CONN_P	16 43
TP93I1	TP_JTAG_SOC_TDO	4
TP93I2	TP_JTAG_WLAN_TCK	44
TP93I3	TP_JTAG_WLAN_TRST_L	44
TP93I4	UART0_SOC_RXD	5 11
TP93I5	UART0_SOC_TXD	5 11
TP93I6	UART3_BB2SOC_TX	5 11 24 28
TP93I7	UART3_SOC2BB_TX	5 11 24 28
TP93I8	UART6_TS_ACC_RXD	5 11
TP93I9	UART6_TS_ACC_TXD	5 11
TP93J0	USB_SOC_N	4 11
TP93J1	USB_SOC_P	4 11
TP93J9	PP3V0_ALS	47 54
TP93JA	PP2V9_CAM	47 54
TP93JB	PP1V3_CAM	47 54
TP93JC	PMU_GPIO_WLAN_REG_ON	44 48

RF TEST POINTS

TP93G1	PP_SMPS1_MSMC_1V05	25 27
TP9301	PP_SMPS3_MSME_1V8	24 25 27 28 30
TP93G5	PP_SMPS5_DSP_1V05	25
TP93E1	PP_LDO1	25
TP93H9	TP_BB_TEST_MODE_0	27
TP9316	TP_BB_TEST_MODE_1	27
TP9302	SIMCRD_RST_CONN	10 24 28
TP93B9	SIMCRD_CLK_CONN	10 24 28
TP93E7	SIMCRD_IO_CONN	10 24 28
TP93E8	SIM_TRAY_DETECT	10 24 28
TP93F3	PP_LDO6_RUIM_1V8	10 24 25 27
TP93J2	GPIO_SOC2BB_RADIO_ON_L	5 24 26
TP93J3	GPIO_SOC2BB_RST_L	5 24 26
TP93J4	PMU_GPIO_PMU2BBPMU_RST_L	24 26 48
TP9381	PMU_GPIO_BB2PMU_HOST_WAKE	24 28 48
TP93J5	PS_HOLD_PMIC	24 26
TP9327	DEBUG_RST_L	24 27
TP9306	BB_JTAG_RTCLK	24 27
TP9307	BB_JTAG_TCK	5 24 27
TP9308	BB_JTAG_TDI	5 24 27
TP9309	BB_JTAG_TDO	5 24 27
TP9310	BB_JTAG_TMS	5 24 27
TP9311	BB_JTAG_TRST_L	5 24 27
TP93J6	USB_BB_N	11 24 53
TP93J7	USB_BB_P	11 24 53
TP93G6	RESET_SOC_L	4 8 10 11 24 48
TP93J8	PMU_GPIO_BB_VBUS_DET	24 27 48

STANDOFFS: P/N 860-1657

STD9300
STDOFF-3.3X1.8R1.28H-SM

STD9301
STDOFF-3.3X1.8R1.28H-SM

STANDOFF: P/N 860-1683

STD9302
STDOFF-3.3X2.2R1.35H-SM-1

PLATED THROUGH HOLES
DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

SL9300
TH-NSP
SL-1.1X0.4-1.4X0.7

SL9303
TH-NSP
SL-1.1X0.4-1.4X0.7

SL9304
TH-NSP
SL-1.1X0.4-1.4X0.7

SL9305
TH-NSP
SL-1.1X0.4-1.4X0.7

MH9300
3P25R2P5

860-1688
MH9302
WASHER-BTN-MLB-X221
TH

NEAR BUTTON FLEX CONN

SYNC MASTER=J85 MLB C SYNC DATE=12/03/12

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EE CHARACTERIZATION TP

NAND

PP9401	1	FMI0_DQS	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652.D34:2MM	6 12 53
PP9402	1	FMI0_AD<3>	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652.C34:2MM	6 12
PP9403	1	FMI0_DQS	PLACE_NEAR=U0652.D34:2MM	6 12 53
PP9410	1	TP_TCKC_U1400		12
PP9411	1	TP_TMSC_U1400		12
PP9412	1	TP_U1400_RB0		12
PP9413	1	TP_U1400_RB1		12

DWI

PP9405	1	DWI_AP_DO	PLACE_SIDE=BOTTOM PLACE_NEAR=U8100:2MM	5 48

AUDIO

PP9406	1	I2S0_CODEC_ASP_MCK	PLACE_NEAR=U1900:2MM	5 15
PP9416	1	I2S2_CODEC_XSP_LRCK	PLACE_NEAR=U1900:2MM	5 15
PP9417	1	I2S2_CODEC_XSP_DOUT	PLACE_NEAR=U1900:2MM	5 15
PP9419	1	I2S1_SPKAMP_MCK	PLACE_NEAR=U2040:2MM	5 16
PP9420	1	I2S1_SPKAMP_BCLK	PLACE_NEAR=U2040:2MM	5 16
PP9421	1	I2S1_SPKAMP_LRCK	PLACE_NEAR=U2040:2MM	5 16
PP9422	1	I2S1_SPKAMP_DOUT	PLACE_NEAR=U2040:2MM	5 16
PP9423	1	I2S1_SPKAMP_DIN	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	5 16
PP9424	1	SPI2_CODEC_SCLK	PLACE_NEAR=U1900:2MM	5 15
PP9425	1	SPI2_CODEC_MOSI	PLACE_NEAR=U1900:2MM	5 15
PP9426	1	SPI2_CODEC_MISO	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	5 15

GRAPE

OSCAR

PP9428	1	UART4_SOC2OSCAR_TXD	PLACE_SIDE=BOTTOM PLACE_NEAR=U2400:2MM	5 19
PP9429	1	UART4_OSCAR2SOC_RXD	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	5 19

UART5

FOR FRANK (SEG)

PP9450	1	PPVDD_SOC_SOC_SENSE	PLACE_NEAR=U0652.V31:1MM	9
PP9451	1	PPVDD_CPU_SOC_SENSE	PLACE_NEAR=U0652.AN30:1MM	9

WIFI

PP9480	HSIC1_WLAN2SOC_DEVICE_RDY		5 44
PP9481	HSIC1_WLAN2SOC_REMOTE_WAKE		5 44
PP9482	PMU_GPIO_WLAN_HOST_WAKE		44 48
PP9483	HSIC1_SOC2WLAN_HOST_RDY		5 44
	GPIO_BT_WAKE	FUNC_TEST=TRUE	5 44

FOR HSIC CHARACTERIZATION

PP9460	1	HSIC1_WLAN_DATA	PLACE_NEAR=U0652.AM33:3MM	4 44 53
PP9462	1	HSIC1_WLAN_DATA	PLACE_NEAR=U5800.13:3MM	4 44 53
PP9463	1	HSIC1_WLAN_STB	PLACE_NEAR=U5800.14:3MM	4 44
PP9468	1	UART1_BT2SOC_TX	PLACE_NEAR=U0652:3MM	5 44
PP9469	1	UART1_SOC2BT_TX	PLACE_NEAR=U5800:3MM	5 44
PP9471	1	UART2_WLAN2SOC_TX	PLACE_NEAR=U0652:3MM	5 44
PP9472	1	UART2_SOC2WLAN_TX	PLACE_NEAR=U5800:3MM	5 44

BASEBAND

	USB_BB_P	FUNC_TEST=TRUE	11 24 52
	USB_BB_N	FUNC_TEST=TRUE	11 24 52

FOR HSIC CHARACTERIZATION

PP9465	1	HSIC2_BB_STB	PLACE_NEAR=U0652.B27:3MM	4 24 27
PP9466	1	HSIC2_BB_DATA	PLACE_NEAR=U3400.C7:3MM	4 24 27

PROX

HIGH SPEED, NO TEST

	MIPI0C_CAM_REAR_CLK_P	NO_TEST=TRUE	7 23 53
	MIPI0C_CAM_REAR_CLK_N	NO_TEST=TRUE	7 23 53
	MIPI0C_CAM_REAR_DATA_P<0..3>	NO_TEST=TRUE	7 23 53
	MIPI0C_CAM_REAR_DATA_N<0..3>	NO_TEST=TRUE	7 23 53
	MIPI0C_CAM_REAR_CLK_FILT_P	NO_TEST=TRUE	23
	MIPI0C_CAM_REAR_CLK_FILT_N	NO_TEST=TRUE	23
	MIPI0C_CAM_REAR_DATA_FILT_P<0..3>	NO_TEST=TRUE	23
	MIPI0C_CAM_REAR_DATA_FILT_N<0..3>	NO_TEST=TRUE	23
	MIPI1C_CAM_FRONT_CLK_P	NO_TEST=TRUE	7 20 53
	MIPI1C_CAM_FRONT_CLK_N	NO_TEST=TRUE	7 20 53
	MIPI1C_CAM_FRONT_DATA_P<0>	NO_TEST=TRUE	7 20 53
	MIPI1C_CAM_FRONT_DATA_N<0>	NO_TEST=TRUE	7 20 53
	MIPI1C_CAM_FRONT_CLK_FILT_P	NO_TEST=TRUE	20
	MIPI1C_CAM_FRONT_CLK_FILT_N	NO_TEST=TRUE	20
	MIPI1C_CAM_FRONT_DATA_FILT_P<0>	NO_TEST=TRUE	20
	MIPI1C_CAM_FRONT_DATA_FILT_N<0>	NO_TEST=TRUE	20
	EDP_DATA_P<0..3>	NO_TEST=TRUE	7 18
	EDP_DATA_N<0..3>	NO_TEST=TRUE	7 18
	EDP_DATA_EMI_P<0..3>	NO_TEST=TRUE	18
	EDP_DATA_EMI_N<0..3>	NO_TEST=TRUE	18
	EDP_DATA_EMI_CONN_P<0..3>	NO_TEST=TRUE	18
	EDP_DATA_EMI_CONN_N<0..3>	NO_TEST=TRUE	18

CAMERA

PP9440	1	MIPI1C_CAM_FRONT_CLK_P	PLACE_NEAR=U0652.AR33:3MM	7 20 53
PP9441	1	MIPI1C_CAM_FRONT_CLK_N	PLACE_NEAR=U0652.AR34:3MM	7 20 53
PP9442	1	MIPI1C_CAM_FRONT_DATA_P<0>	PLACE_NEAR=U0652.AT33:3MM	7 20 53
PP9443	1	MIPI1C_CAM_FRONT_DATA_N<0>	PLACE_NEAR=U0652.AT34:3MM	7 20 53
PP9444	1	MIPI0C_CAM_REAR_CLK_P	PLACE_NEAR=U0652.AU25:3MM	7 23 53
PP9445	1	MIPI0C_CAM_REAR_CLK_N	PLACE_NEAR=U0652.AV25:3MM	7 23 53
PP9446	1	MIPI0C_CAM_REAR_DATA_P<0>	PLACE_NEAR=U0652.AU27:3MM	7 23 53
PP9447	1	MIPI0C_CAM_REAR_DATA_N<0>	PLACE_NEAR=U0652.AV27:3MM	7 23 53

iFixit.Solutions

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POWER CONNECTIONS

BUCK0

52 46 PPVDD_CPU (MAKE_BASE=TRUE) — =PPVDD_CPU 9

BUCK1

52 46 PPVDD_GPU (MAKE_BASE=TRUE) — =PPVDD_GPU 9

BUCK2

52 46 PPVDD_SOC (MAKE_BASE=TRUE) — =PPVDD_SOC 9

BUCK3

52 47 46 PP1V8_S2R (MAKE_BASE=TRUE)
- =PP1V8_S2R_MISC 5 51
- =PP1V8_S2R_VDDIO_WLAN_BT 44
- =PP1V8_S2R_TRISTAR 11
- =PP1V8_S2R_DDR 8
- =PP1V8_S2R_GRAPE 13
- =PP1V8_S2R_EXT_SWITCH 50
- =PP1V8_S2R_REAR_CAMERA
- =PP1V8_S2R_MESA
- =PP1V8_S2R_VDD_CORE_GPS
- =PP1V8_S2R_VDD_IO_GPS

BUCK3_SW

52 50 46 PP1V8_SW1 (MAKE_BASE=TRUE)
- =PP1V8_AUDIO 15
- =PP1V8_DMIC 14
- =PP1V8_CAM_FRONT 20
- =PP1V8_CAM_REAR 23
- =PP1V8_PROX 22

52 50 PP1V8_EXT_SW (MAKE_BASE=TRUE)
- =PP1V8_VDDIO18_SOC 8 9
- =PP1V8_SOC 4 5 7 10 18
- =PP1V8_MIPI_SOC 7
- =PP1V8_EDP_SOC 7
- =PP1V8_NAND_SOC 6
- =PP1V8_NAND 12 48
- =PP1V8_PLL_SOC 4
- =PP1V8_SPKRAMP
- =PP1V8_EEPROM 51
- =PP1V8_BEACON

52 46 PP1V8_SW2 (MAKE_BASE=TRUE) — =PP1V8_GRAPE 13

46 PP1V8_S2R_SW3 (MAKE_BASE=TRUE)
- =PP1V8_S2R_GYRO 21
- =PP1V8_S2R_ACCEL 21
- =PP1V8_S2R_OSCAR 19
- PP1V8_S2R_SW3_COMP 52 54

54 52 PP1V8_S2R_SW3_COMP (MAKE_BASE=TRUE) — =PP1V8_S2R_COMP 21

PP1V8_S2R_SW3 SHOULD BE ON IN HIBERNATE
CURRENTLY POWERS OSCAR AND 1.8V RAIL ON SENSOR

BUCK4

52 47 46 PP1V2_S2R (MAKE_BASE=TRUE)
- =PP1V2_S2R_DDR 8
- =PP1V2_S2R_DDR_SOC 8
- =PP1V2_S2R_CAM_REAR

BUCK4_SW

52 46 PP1V2_SW1 (MAKE_BASE=TRUE)
- =PP1V2_VDDQ_DDR 8
- =PP1V2_VDDIOD_SOC 8
- =PP1V2_HSIC_SOC 4

52 46 PP1V2_S2R_SW2 (MAKE_BASE=TRUE) — =PP1V2_S2R_OSCAR 19

PP1V2_S2R_SW2 SHOULD BE ON IN HIBERNATE
PROVIDE 1.2V TO OSCAR

BUCK5

52 46 PPVDD_SRAM (MAKE_BASE=TRUE)
- =PPVDD_SRAM_CPU
- =PPVDD_SRAM_SOC 9

BUCK6

52 46 PP3V3_S2R (MAKE_BASE=TRUE)
- =PP3V3_S2R_SWITCH 48
- =PP3V3_S2R_WIFI_PA 44

52 48 PP3V3_SW (MAKE_BASE=TRUE)
- =PP3V3_EDP_PU
- =PP3V3_NAND 12
- =PP3V3_USB_SOC 4

LDO1

52 47 PP3V0_SPARE1 (MAKE_BASE=TRUE) — =PP3V0_SPARE1 49

LDO2

52 47 16 PP1V7_VA_VCP (MAKE_BASE=TRUE) — =PP1V7_VA_VCP 15 16

LDO3

LDO3 SHOULD BE ON IN HIBERNATE
COMPASS, ACCEL, GYRO, PROX ARE ON OSCAR
HALL EFFECT NEEDS TO BE ON IN HIBERNATE

52 47 PP3V0_S2R_SENSOR (MAKE_BASE=TRUE)
- =PP3V0_S2R_HALL 13
- =PP3V0_S2R_GYRO 21
- =PP3V0_S2R_ACCEL 21
- =PP3V0_S2R_COMP 21

LDO4

52 47 PP3V0_ALS (MAKE_BASE=TRUE)
- =PP3V0_ALS 20
- =PP3V0_PROX 22
- =PP3V0_HP_ALS
- =PP3V0_IO_ALS

SHOULD IO ALS POWER HERE?

LDO5

52 47 PP3V0_UVLO (MAKE_BASE=TRUE) — =PP3V0_UVLO 49

LDO6

52 47 PP3V3_ACC (MAKE_BASE=TRUE) — =PP3V3_ACC 11

LDO7

LDO7 SHOULD BE ON IN HIBERNATE

52 47 PP3V0_S2R_TRISTAR (MAKE_BASE=TRUE) — =PP3V0_S2R_TRISTAR 11

LDO8

47 NC_LDO8 (MAKE_BASE=TRUE) NO_TEST=TRUE — =NC_LDO8

LDO9

BACKUP RAIL. CAN BE BOOSTED TO MEET
1.1V MIN ON CAMERA IF NEEDED.

52 47 PP1V3_CAM (MAKE_BASE=TRUE)
- =PP1V3_CAM_FRONT
- =PP1V3_CAM_REAR 23

LDO10

52 47 PP1V0_SOC (MAKE_BASE=TRUE)
- =PP1V0_USB_SOC 4
- =PP1V0_MIPI_SOC 7
- =PP1V0_EDP_PAD_DVDD_SOC 7

LDO11

52 47 PP2V6_CAM_AF (MAKE_BASE=TRUE) — =PP2V6_CAM_REAR_AF 23

LDO13

52 47 PP2V9_CAM (MAKE_BASE=TRUE)
- =PP2V9_CAM_FRONT 20
- =PP2V9_CAM_REAR 23

VLCM1

47 PP5V25_GRAPE (MAKE_BASE=TRUE) — =PP5V25_GRAPE 13

CHARGER MAIN

52 49 48 47 46 PPVCC_MAIN (MAKE_BASE=TRUE)
- =PPVCC_MAIN_AUDIO 15 16
- =PPVCC_MAIN_LED 47
- =PPVCC_MAIN_DOCK 43
- =PPVCC_MAIN_DEV
- =PPVCC_MAIN_CPU 46
- =PPVCC_MAIN_GPU 46
- =PPVCC_MAIN_SOC 46
- =PPVCC_MAIN_GRAPE 13
- =PPVCC_MAIN_LCD 18
- =PPVCC_MAIN_NAVAJO
- =PPVCC_MAIN_VDD_LCM 47
- =PPVCC_MAIN_WLAN 44
- =PPVCC_MAIN_GPS

BATTERY

52 46 PPBATT_VCC (MAKE_BASE=TRUE)
- =PPBATT_POS_CONN 45
- =PPBATT_VCC_BB 24 25 33 34 35 36 37 38
- =PPBATT_AUDIO

USB POWER INPUT

52 46 PPVBUS_USB_DCIN (MAKE_BASE=TRUE) — =PPVBUS_USB_EMI 43

ON_BUF

52 47 PP1V8_ALWAYS (MAKE_BASE=TRUE) — =PP1V8_ALWAYS 5

BACKLIGHT BOOST

52 47 PPLED_OUT_A (MAKE_BASE=TRUE) — =PPLED_REG_A 18

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